SLAS331 – APRIL 2001

DIGITAL AUDIO INTERFACE RECEIVER

FEATURES

- **Standard Digital Audio Interface Receiver (EIAJ1201)**
- **Sampling Rate: 32/44.1/48/88.2/96 kHz**
- **Recover 128 / 256 / 384 / 512 f_S System Clock**
- **Very Low Jitter System Clock Output (80ps Typically)**
- **On-Chip Master Clock Oscillator, Only an External 12.000 MHz or 16.000 MHz Crystal Is Required**
- **Selectable Output PCM Audio Data Format**
- **Output User Bit Data, Flag Signals, and Channel Status Data With Block Start Signal**
- **Single + 3.3-V Power Supply**
- **Package: 28 SSOP**

APPLICATIONS

- **AV Receiver**
- **MD Player**
- **DAC Unit**

DESCRIPTION

The DIR1701 is a digital audio interface receiver (DIR) which receives and decodes audio data up to 96 kHz according to the AES/EBU, IEC958, S/PDIF, and EIAJCP340/1201 consumer and professional format interface standards. The DIR1701 demultiplexes the channel status bit and user bit directly to serial output pins, and has dedicated output pins for the most important channel status bits.

The significant advantages of the DIR1701 are *96 kHz sampling rate capability* and *Low-jitter clock recovery by the Sampling Period Adaptive Controlled Tracking* (SpAct™) *system.* Input signal is reclocked with the patented *Sampling period Adaptive controlled tracking system* for maximum quality. These two features are required for recent consumer and professional audio instruments, in which the DIR has an interface to any kind of delta-sigma type ADC/DAC with 96 kHz sampling rate.

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precaustions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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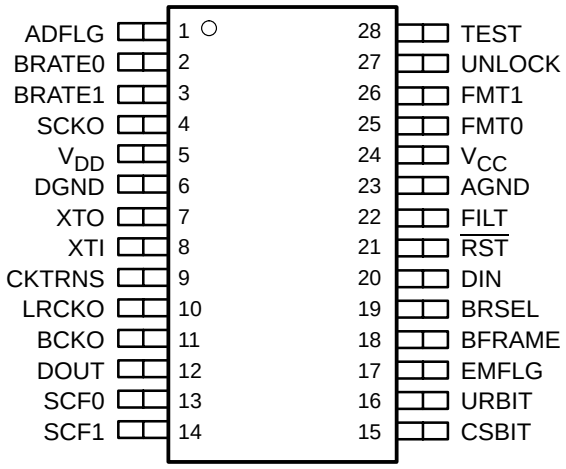
DIR1701
(TOP VIEW)

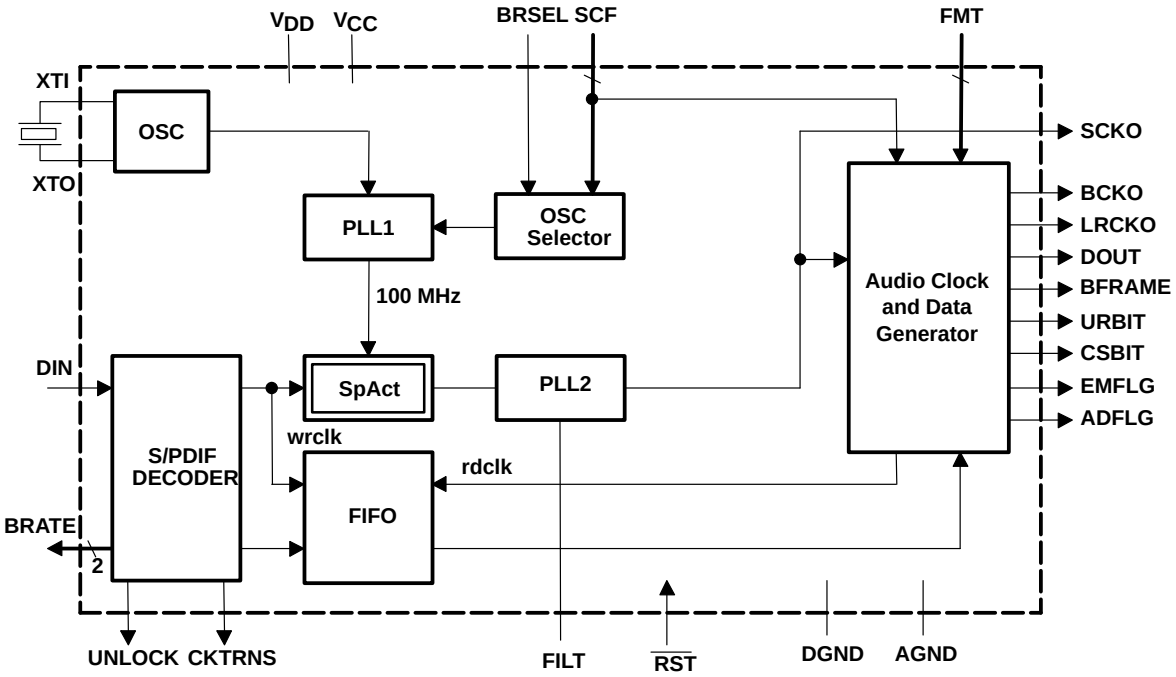


PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER‡	TRANSPORT MEDIA
DIR1701E	SSOP–28	324†	–25°C to +85°C	DIR1701E	DIR1701E	Rails
					DIR1701E/2K	Tape and Reel

† TI equivalent no. 4040065.
‡ Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of DIR1701E/2K will get a single 2000-piece tape and reel.

block diagram



Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
ADFLG	1	O	Audio data or digital data flag
BRATE0	2	O	f_S rate flag 0 (32k, 44.1k, 48k, and 88k / 96k)
BRATE1	3	O	f_S rate flag 1 (32k, 44.1k, 48k, and 88k / 96k)
SCKO	4	O	System clock output
V_{DD}	5	–	Digital power supply, +3.3 V
DGND	6	–	Digital ground
XTO	7	O	Crystal oscillator output
XTI	8	I	Crystal oscillator input, external clock input
CKTRNS	9	O	Clock transition status output
LRCKO	10	O	Audio latch enable (LRCK, f_S) output
BCKO	11	O	Audio bit clock output
DOUT	12	O	Audio serial data output
SCF0	13	I	System clock frequency select (128/256/384/512 f_S) (see Note 1)
SCF1	14	I	System clock frequency select (128/256/384/512 f_S) (see Note 1)
CSBIT	15	O	Channel status bit output (see Note 2)
URBIT	16	O	User bit output (see Note 2)
EMFLG	17	O	Emphasis flag
BFRAME	18	O	Block start clock (B-frame)
BRSEL	19	I	Default bit rate select (32 / 44.1 / 48 / 88.2 / 96k) (see Note 1)
DIN	20	I	S/PDIF data digital input (see Note 4)
$\overline{RST}$	21	I	Reset input, active LOW (see Note 3)
FILT	22	–	External filter
AGND	23	–	Analog ground
V_{CC}	24	–	Analog power supply, +3.3V
FMT0	25	I	Audio data format select (see Note 1)
FMT1	26	I	Audio data format select (see Note 1)
UNLOCK	27	O	PLL unlock or parity error flag
TEST	28	I	Should be connected to DGND (see Note 1)

NOTES: 1. Schmitt trigger input with internal pulldown (TYP 51 kΩ), 5 V tolerant.
2. Serial outputs are utilized for both consumer and professional application.
3. Schmitt trigger input with internal pullup (TYP 51 kΩ), 5 V tolerant.
4. CMOS level input with internal pulldown (TYP 51 kΩ), 5 V tolerant.

absolute maximum ratings†

Supply voltage, V_{CC}, V_{DD}		4.0 V
Supply voltage differences, V_{CC}, V_{DD}		±0.1 V
Ground voltage differences, AGND, DGND		±0.1 V
Digital input voltage:	Digital input pins except XTI	–0.3 V to (6.5 V + 0.3 V)
	XTI	–0.3 V to (V_{DD} + 0.3 V)
Input current (Any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 sec
Package temperature (IR reflow, peak)		235°C, 10 sec

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
V_{IH} (5)	Input logic level		2		5.5	VDC
V_{IL} (5)					0.8	
V_{IH2} (6)			70%V_{DD}			
V_{IL2} (6)					30%V_{DD}	
V_{IH3} (7)			70%V_{DD}		5.5	
V_{IL3} (7)					30%V_{DD}	
V_{OH} (8)	Output logic level	I_O = 1 mA	V_{DD}–0.4			VDC
V_{OL} (8)		I_O = –2 mA			0.5	
V_{OH} (9)		I_O = 2 mA	V_{DD}–0.4			
V_{OL} (9)		I_O = –4 mA			0.5	
I_{IH}(10)	Input leakage current	V_{IN} = V_{DD}		65	100	µA
I_{IL}(10)		V_{IN} = 0 V	–10		10	
I_{IH}(11)		V_{IN} = V_{DD}	–10		10	
I_{IL}(11)		V_{IN} = 0 V	–100	–65		
I_{IH}(6)		V_{IN} = V_{DD}	–10		10	
I_{IL}(6)		V_{IN} = 0 V	–10		10	
f_S(12)	Input sampling frequency		32		96	kHz
SCKO	System clock frequency		4.096	128/256/ 384/512 f_S	49.152	MHz
t_j	SCKO clock jitter			80		ps RMS
	SCKO duty cycle			50%		
	XTI clock accuracy		–500	See Table 3	500	ppm
S/PDIF INPUT						
	Duty cycle	V_{IN} = 1.5 V, f_S = 96 kHz	15%		85%	
	Jitter	V_{IN} = 1.5 V			20	ns p-p
POWER SUPPLY REQUIREMENTS						
V_{DD}, V_{CC}	Voltage range		3	3.3	3.6	VDC
I_{CC} (V_{CC})	Supply current (see Note 13)			3.4	4.7	mA
I_{DD} (V_{DD})				26	36	
P_D	Power dissipation			100		mW
POWER SUPPLY REQUIREMENTS						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

NOTES: 5. TTL compatible, except pins 8, 20: XTI, DIN.
6. Pin 8: XTI (CMOS logic level).
7. Pin 20: DIN (CMOS logic level).
8. Pins 1–3, 9, 17–18, 27: ADFLG, BRATE0, BRATE1, CKTRNS, EMFLG, BFRAME, UNLOCK.
9. Pins 4, 10–12, 15–16: SCKO, LRCKO, BCKO, DOUT, CSBIT, URBIT.
10. Pins 13–14, 19–20, 25–26, 28: SCF0, SCF1, BRSEL, DIN, FMT0, FMT1, CKSEL.
11. Pin 21: $\overline{RST}$
12. f_S is defined as the incoming audio sampling frequency per channel.
13. No load connected to SCKO, LRCKO, BCKO, DOUT, CSBIT, URBIT. Power supply current varies according to the system clock frequency.

basic operation theory

The DIR1701 has two PLLs, PLL1 and PLL2. The SpAct (Sampling Period Adaptive Controlled Tracking) system is a newly developed clock recovery architecture, giving very low jitter clock from S/PDIF data input. The DIR1701 requires a system clock input for operation of SpAct; internal PLL1 provides a 100 MHz execution clock. The system clock can be obtained by either connecting a suitable crystal resonator at the XTI/XTO pins or applying an external clock input at the XTI pin as shown in Figure 1. Internal PLL2 generates the system clock SCKO by using the output signal of the SpAct frequency estimator.

When the S/PDIF input signal ceases, SCKO holds the latest tracked frequency. Also, the DIR1701 indicates the unlocked state by a HIGH level output at the UNLOCK pin. When the S/PDIF signal restarts, the PLL will lock in around 1ms with very low jitter, using the SpAct estimator. Then the DIR1701 indicates the locked status by a LOW level output at the UNLOCK pin. In this status, the BRATE pins indicate the actual bit rate of the incoming S/PDIF signal.

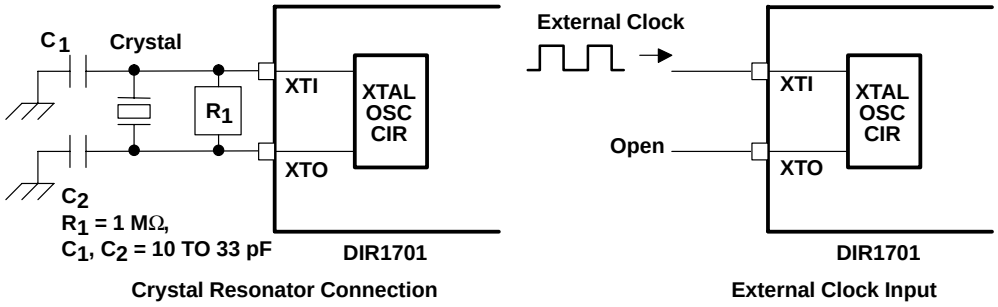


Figure 1. System Clock Connections

system clock output

The primary function of the DIR1701 is to recover audio data and a low jitter clock from a digital audio transmission line. The clocks that can be generated are SCKO (128/256/384/512 f_S, shown in Table 1), BCKO (64 f_S), and LRCKO (1 f_S). SCKO is the output of the voltage controlled oscillator (VCO) in an analog PLL. The PLL function consists of a VCO, phase and frequency detector, and a external second-order loop filter. The closed-loop transfer function, which specifies the PLL jitter attenuation characteristics, is shown in Figure 2.

The crystal frequency should be defined for internal PLL by connecting the BRSEL pin to one of the output pins BFRAME or CSBIT as shown in Table 2. A 12 MHz crystal resonator can be used for 128f_S (CSBIT), 256f_S (OPEN) and 384f_S (BFRAME). And a 16 MHz crystal resonator is used for 512f_S (BFRAME). The system clock frequency can be set by control data at SCF0, SCF1 pin (shown in Table 3); this data must be stable before reset is applied.

Table 4 shows the state of the system and the condition of audio clocks and flags. Required accuracy of system clock by either crystal resonator or external clock input is ±500 ppm.

Table 1. Generated System Clock (SCKO) Frequencies

SAMPLING RATE	128 f_S	256 f_S	384 f_S	512 f_S
32 kHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz
44.1 kHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz
48 kHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz
88.2kHz	11.2896 MHz	22.5792 MHz	33.8688 MHz	45.1584 MHz
96 kHz	12.288 MHz	24.576 MHz	36.864 MHz	49.152 MHz

system clock output (continued)

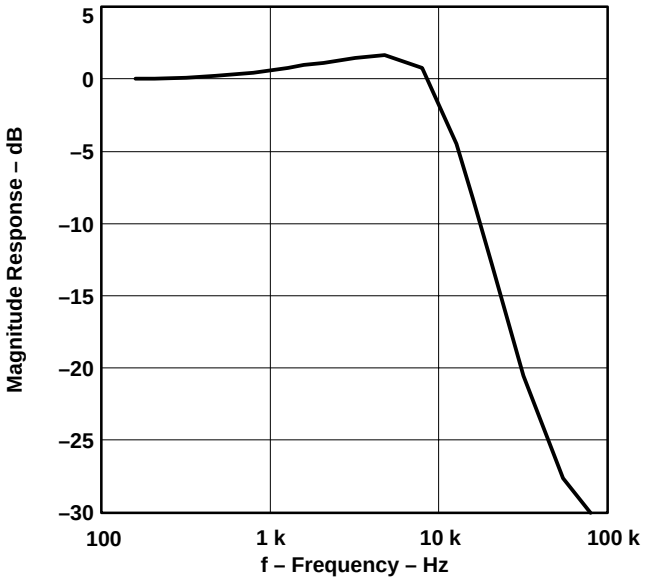


Figure 2. Jitter Attenuator Characteristics With Specified Loop Filter

Table 2. Selectable Crystal Oscillators

SYSTEM CLOCK f_S	CRYSTAL	BRSEL CONNECTED TO
128	12 MHz	CSBIT
256	12 MHz	OPEN or DGND
384	12 MHz	BFRAME
512	16 MHz	BFRAME

Table 3. System Clock Selection

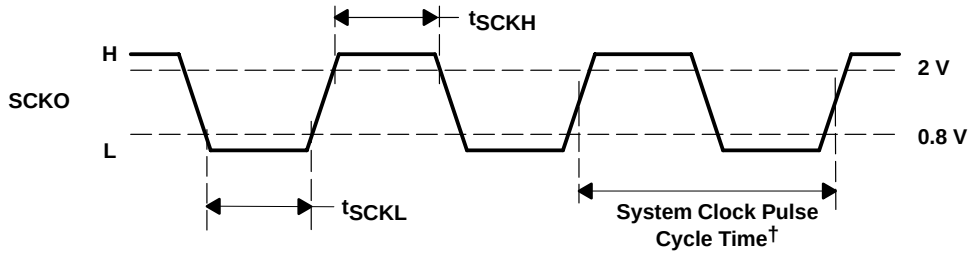
SCF1	SCF0	SYSTEM CLOCK
LOW	LOW	128 f_S
LOW	HIGH	256 f_S
HIGH	LOW	384 f_S
HIGH	HIGH	512 f_S

Table 4. System Clock and Data Output Operation

CONDITIONS	CLOCK AND DATA OUTPUTS							
S/PDIF DATA	SCKO	BCKO	LRCKO	DOUT	BRATE	UNLOCK	CS. UR BIT	AD. EMFLG
After RESET	Unknown (128, 256, 384, 512 f_S)	Unknown (64 f_S)	Unknown (1 f_S)	MUTE	LOW	HIGH	LOW	LOW
YES	PLL (128, 256, 384, 512 f_S)	PLL (64 f_S)	PLL (1 f_S)	DATA	DETECT	LOW	DATA	DATA
NO	HOLD† (128, 256, 384, 512 f_S)	HOLD† (64 f_S)	HOLD† (1 f_S)	MUTE	HOLD†	HIGH	HOLD†	HOLD†

† Holds the latest tracked frequency.

SCKO timing



SCKO Clock Pulse Width High	t_{SCKH}	7 ns (min)
SCKO Clock Pulse Width Low	t_{SCKL}	7 ns (min)

† 1/128 f_S, 1/256 f_S, 1/384 f_S or 1/512 f_S.

bit rate detection

By using the SpAct frequency estimator (not the S/PDIF channel status bit), the DIR1701 detects automatically the sample rate of an incoming S/PDIF signal and indicates the frequency at the BRATE pins.

Table 5 lists the frequency ranges reported. Except for 88.2 and 96 kHz, these sample rates are the same as the channel status bit defined in the S/PDIF specifications. When the bit-rate is 88.2 or 96 kHz the indicator shows the same HL value. This state is not defined in the S/PDIF specifications.

Table 5. Incoming Sample Frequency Bits

SAMPLING RATE	BRATE1	BRATE0
32 kHz	HIGH	HIGH
44.1 kHz	LOW	LOW
48 kHz	LOW	HIGH
88.2 kHz	HIGH	LOW
96 kHz	HIGH	LOW

timing specification for PLL operation

lock-up time

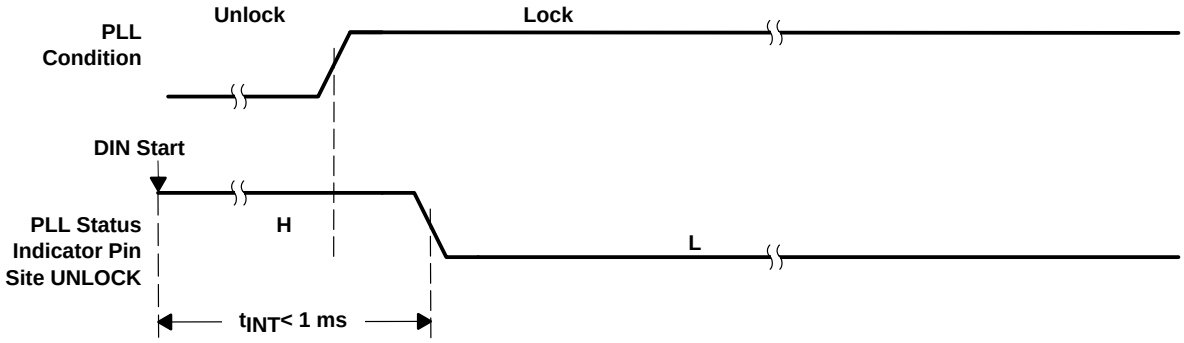


Figure 3. PLL Lock Up Timing

relation between audio-data-output timing and PLL condition indicator timing

When the analog PLL is still unlocked and the S/PDIF signal starts, after at least ten rising edges, the S/PDIF decoder can detect the incoming S/PDIF signal. The DOUT pin becomes LOW (MUTE) until the analog PLL locks. This MUTE period t_{INT} is less than 1 ms (the analog PLL lockup time is less than 0.5 ms). When the decoder detects that incoming S/PDIF signal has stopped, UNLOCK goes HIGH at the next LRCKO transition. SCKO keeps its frequency at the latest tracked bit rate.

When S/PDIF signal is not present after removal of reset, the frequency of the DIR1701 audio clocks (SCKO, BCKO, LRCKO) is not known.

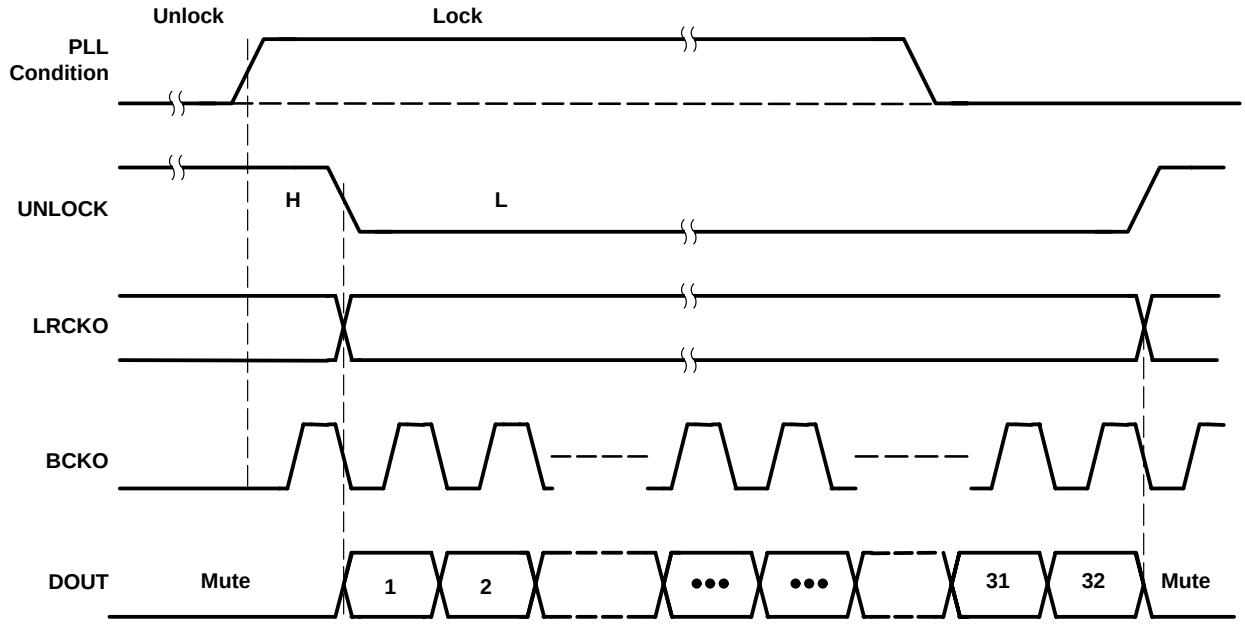


Figure 4. Relation Between Audio Data Output Timing and UNLOCK Flag Timing

unlock flag minimum pulse width time

CASE-A when PLL is unlocked

When the PLL is unlocked, the UNLOCK flag pin is HIGH and the audio data output DOUT becomes LOW (MUTE). The MUTE period, t_{UNL}, is at least 200 ms. In this period, SCKO, BCKO, and LRCKO frequency hold the latest tracked frequency.

If an S/PDIF signal is connected again in this unlock period, the bit rate is changed to the incoming signal frequency, after at least 1 ms (before the UNLOCK flag goes LOW). The CKTRNS pin indicates validity of SCKO. When CKTRNS is HIGH, the frequency of SCKO, BCKO, and LRCKO is in transition between states.

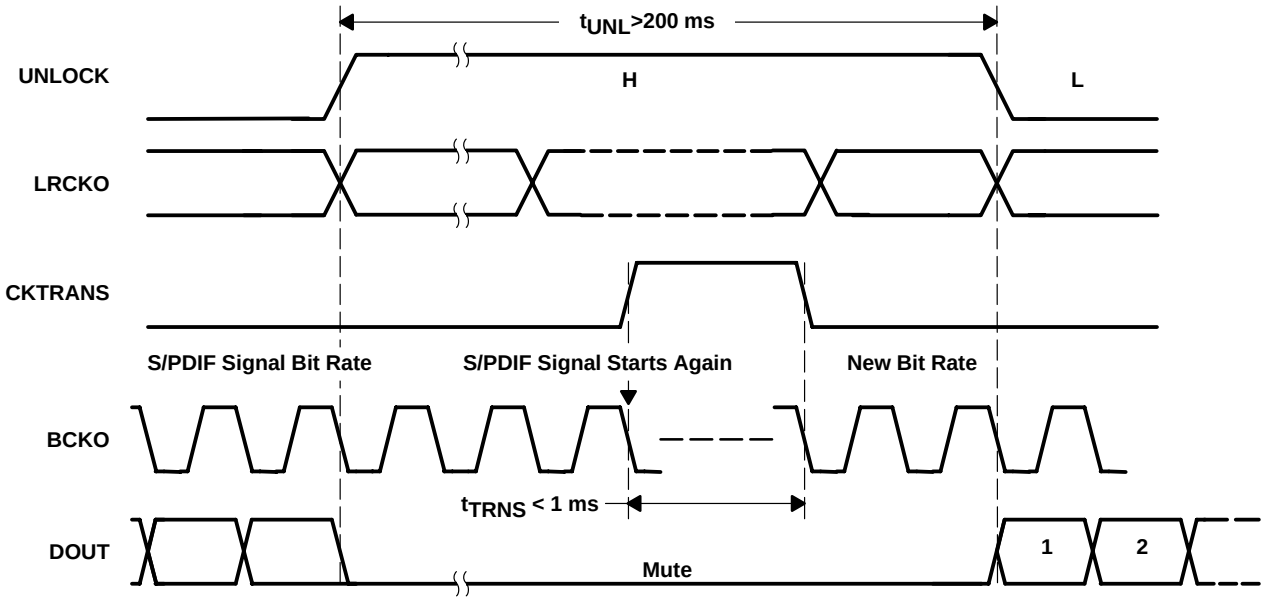


Figure 5. UNLOCK Flag Minimum Pulse Width Time for PLL Unlocked

unlock flag minimum pulse width time (continued)

CASE-B when parity error occurs

When a parity error occurs in one subframe interval, UNLOCK becomes HIGH during this sub-frame then returns LOW at the next arriving subframe.

During this subframe with parity error, the data output will hold the previous data of each channel.

CASE-B When Parity Error Occurs

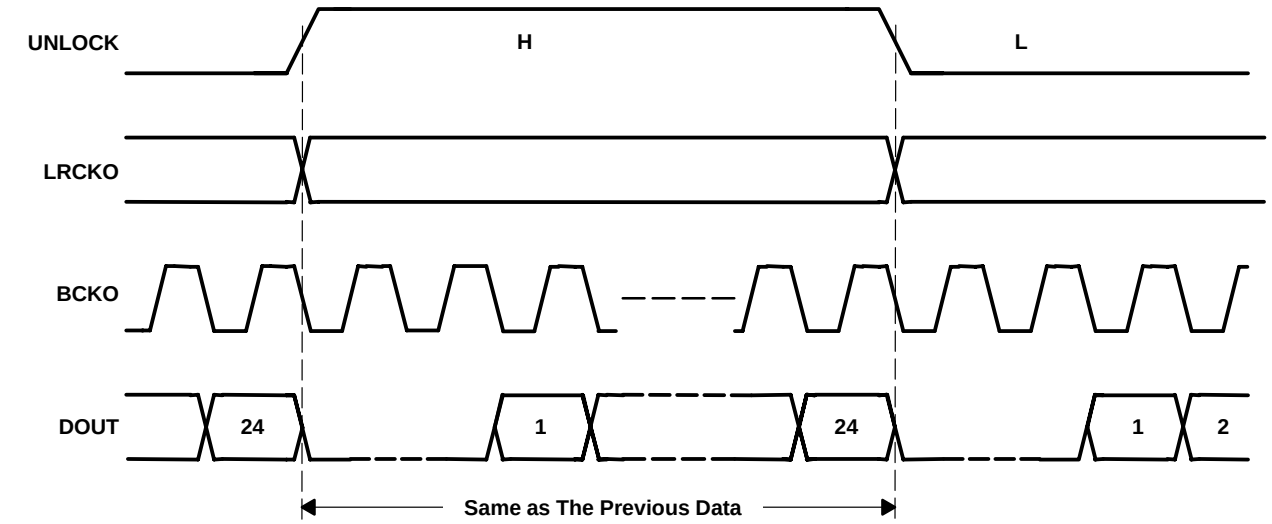


Figure 6. UNLOCK Timing for Parity Error

PCM audio interface

The DIR1701 can produce 16-bit or 24-bit output data in standard format and 24-bit output data in IIS format.

The PCM audio interface format of the DIR1701 is selected using the format pins FMT1, FMT0. Table 6 shows the FMT pin configuration.

Table 6. Audio Output Data Format Select

FMT1	FMT0	AUDIO DATA FORMAT
LOW	LOW	16 bit MSB first, Right justified
LOW	HIGH	24 bit MSB first, Right justified
HIGH	LOW	24 bit MSB first, Left justified
HIGH	HIGH	24 bit IIS

PCM audio interface (continued)

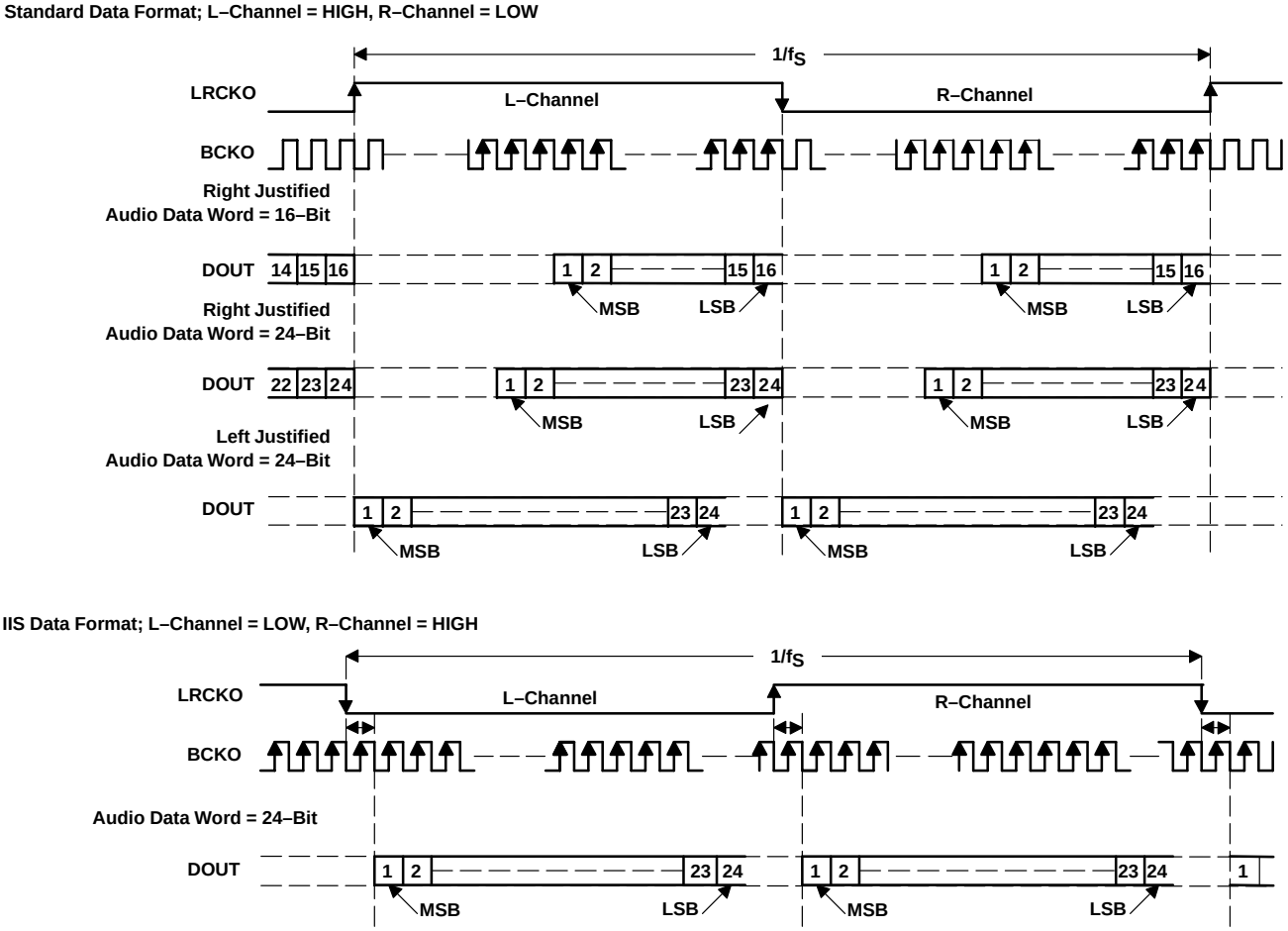
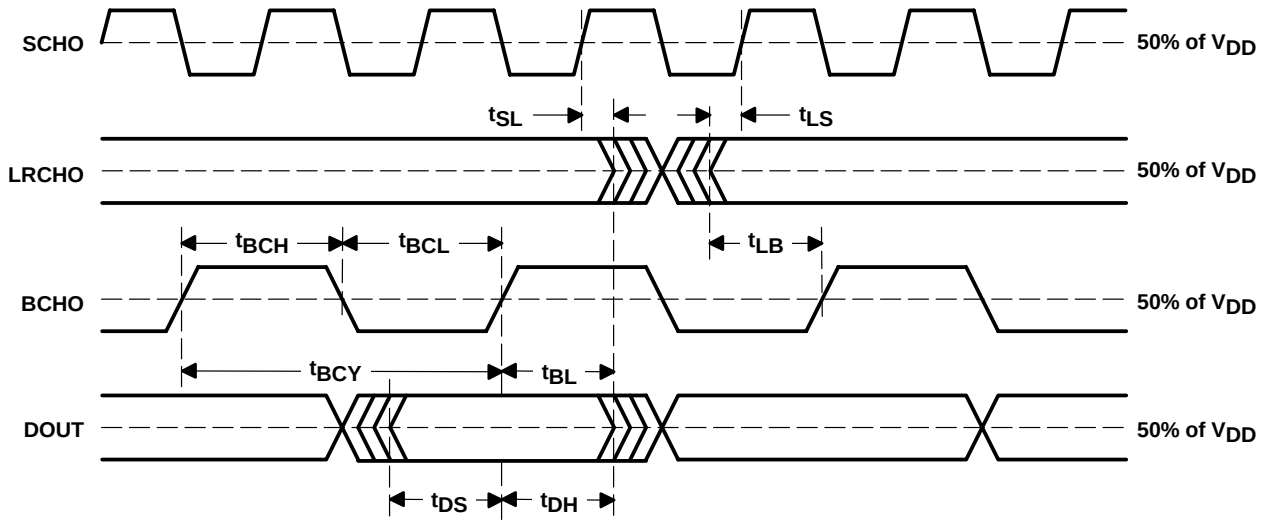


Figure 7. Audio Data Output Format

PCM audio interface (continued)



PARAMETERS		MIN	MAX	UNITS
t_{SL}	SCKO rising edge to LRCKO edge	11		ns
t_{LS}	LRCKO edge to SCKO rising edge	5		ns
t_{BCY}	BCKO pulse cycle time		64 f_S	
t_{BCL}	BCKO pulse width low	78		ns
t_{BCH}	BCKO pulse width high	78		ns
t_{BL}	BCKO rising edge to LRCKO edge	78		ns
t_{LB}	LRCKO edge to BCKO rising edge	78		ns
t_{DS}	DOUT setup time	78		ns
t_{DH}	DOUT hold time	78		ns

Figure 8. Audio Data Output Timing

dedicated output pins for both professional and consumer applications

The DIR1701 has parallel output pins for both professional and consumer applications. In professional mode de-emphasis flag EMFLG indicates a 50/15-µs time constant pre-emphasis. Professional mode is set when Bit 0 of CSBIT Byte 0 is HIGH. When Bits 2 to 4 of CSBIT Byte 0 is 110, the EMFLG becomes HIGH. In other cases, EMFLG is LOW. Audio/non-audio flag ADFLG indicates S/PDIF data mode, i.e., Bit 1 of CSBIT Byte 0. When ADFLG is LOW, S/PDIF data includes PCM audio signal. In other cases, ADFLG is HIGH.

In consumer mode EMFLG indicates 2-channel audio with a 50/15-µs time constant pre-emphasis. Consumer mode is set when Bit 0 of CSBIT Byte 0 is LOW. When Bits 3 to 5 of CSBIT Byte 0 is 100, EMFLG becomes HIGH. In other cases, EMFLG is LOW. The ADFLG signal indicates whether S/PDIF includes digital data, such as AC-3 or not. When Bit 1 of CSBIT Byte 0 is HIGH, the incoming S/PDIF includes non-audio signal. In other cases, ADFLG is LOW.

These dedicated output pins are checked for only L-ch CS information. The DIR1701 does not support CRC check function in professional mode. As for other flags, CS bit and user-bit for professional and consumer applications, are directly supplied by serial mode at CSBIT (pin 15) and URBIT (pin 16). These pins indicate L-ch and R-ch information sequentially.

dedicated output pins for both professional and consumer applications (continued)

Audio data and clock timing are described below. The serial output data starts after 16±8 BCKO clocks from when the corresponding subframe arrives. When B subframe arrives, BFRAME pin becomes HIGH during $1/f_S$ x 32 (s), then BFRAME returns to LOW after 32 frames.

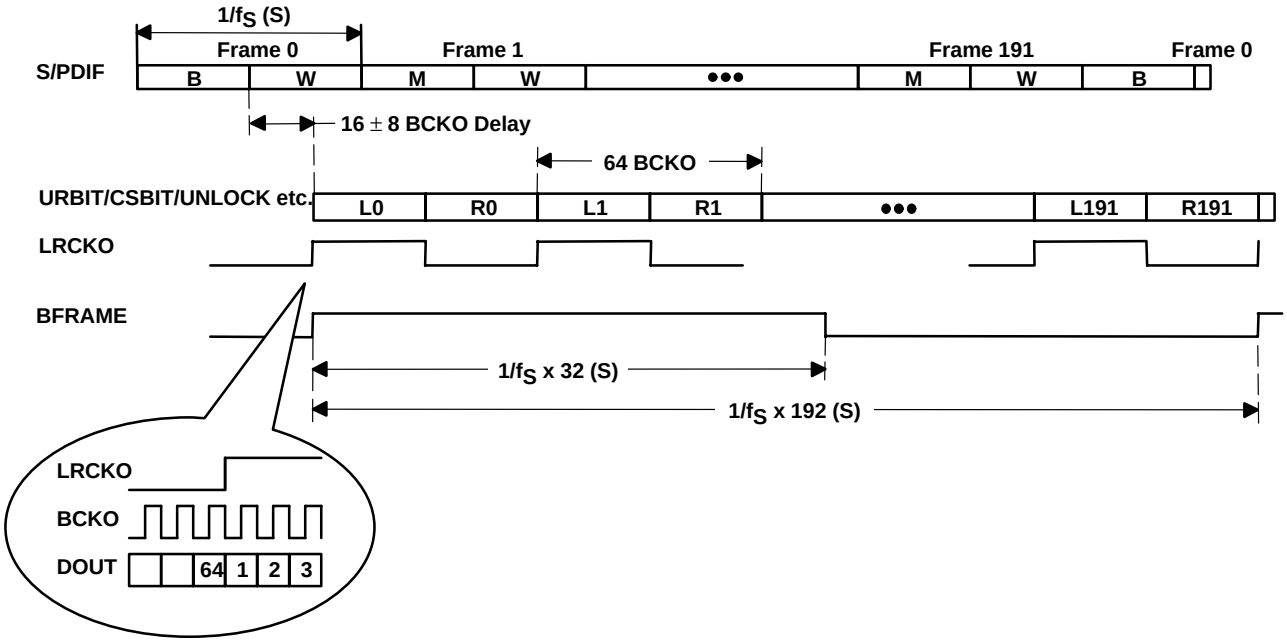
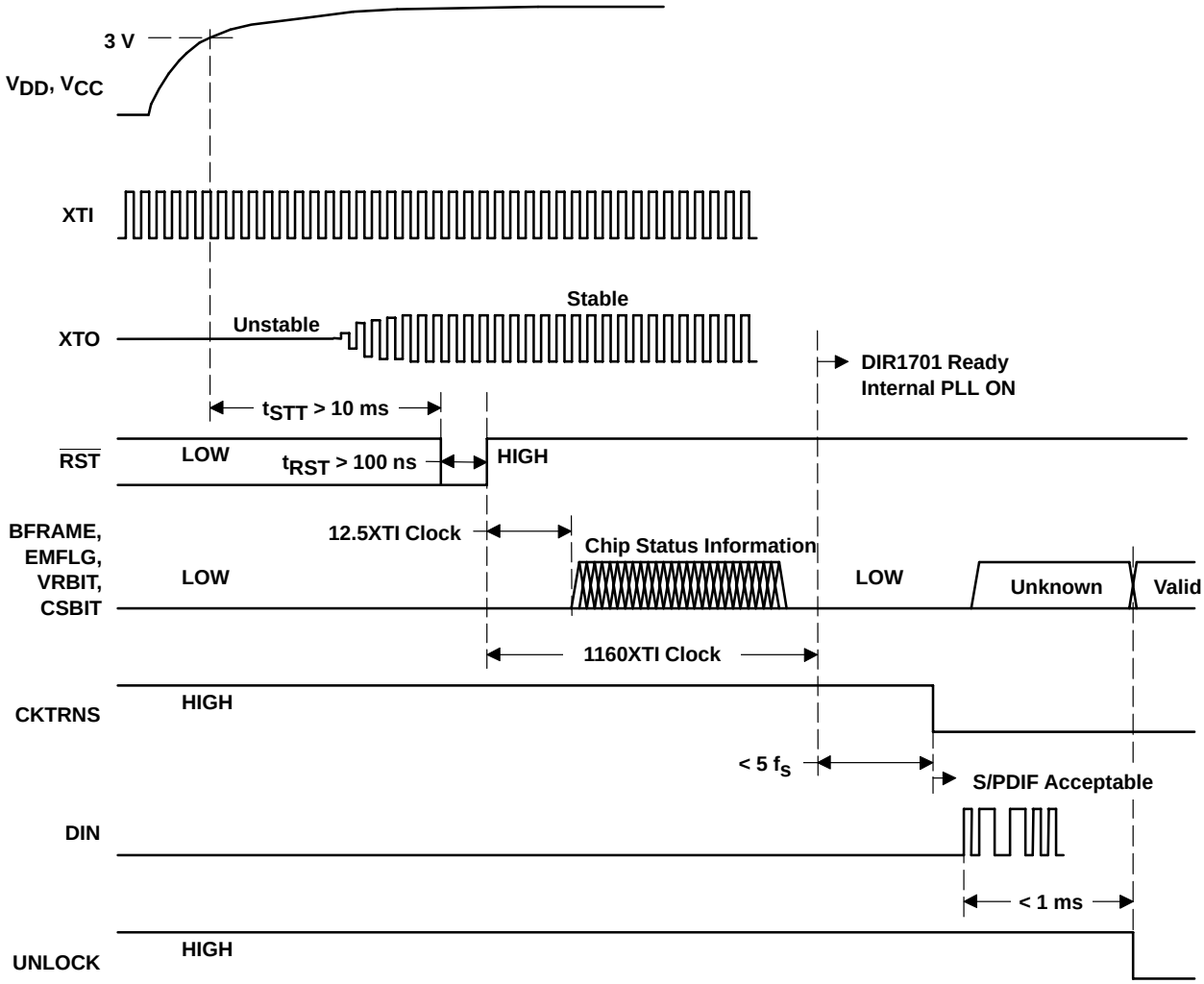


Figure 9. Timing Chart for Audio Data and Channel Status

reset sequence

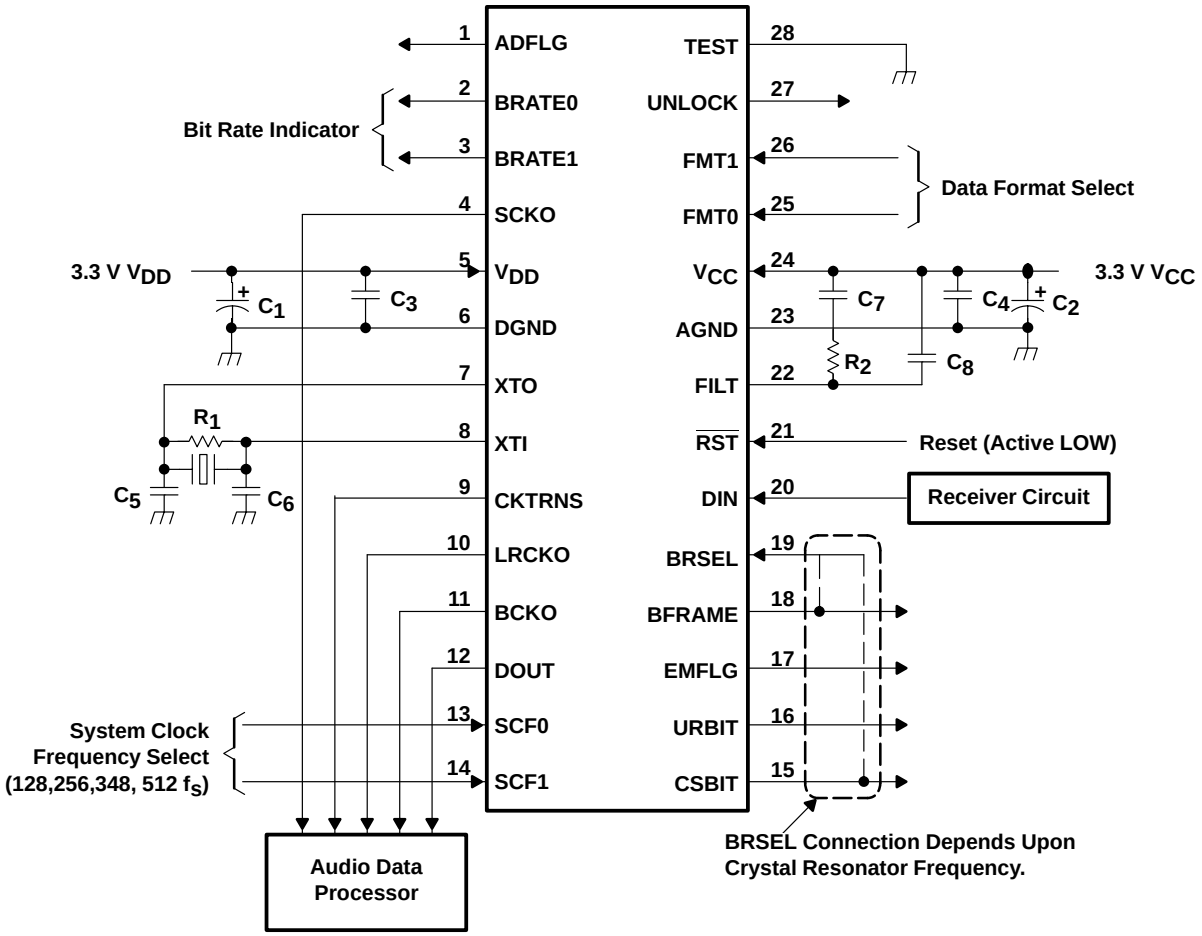
The DIR1701 requires external reset operation after power on. Figure 10 shows the reset sequence after power on. The DIR1701 is ready for receiving S/PDIF signal when the internal reset sequence has finished and CKTRNS goes to LOW. BFRAME, EMFLG, URBIT and CSBIT pins are used for configuration during the period from the rising edge of $\overline{RST}$ to the falling edge of CKTRNS. S/PDIF signal is accepted after CKTRNS goes to LOW. The minimum pulse width of $\overline{RST}$, t_{RST} is 100 ns. The $\overline{RST}$ delay after the power supply reaches 3 V should be at least 10 ms. All of the output pins except CKTRNS and UNLOCK are LOW during $\overline{RST}$ LOW.



NOTE: SCF0 and SCF1 should be settled during $\overline{RST}$ assertion. The change of SCF0 and SCF1 is not permitted during normal operation. When the change is needed, the reset sequence must be started by asserting $\overline{RST}$ again.

Figure 10. After Power ON

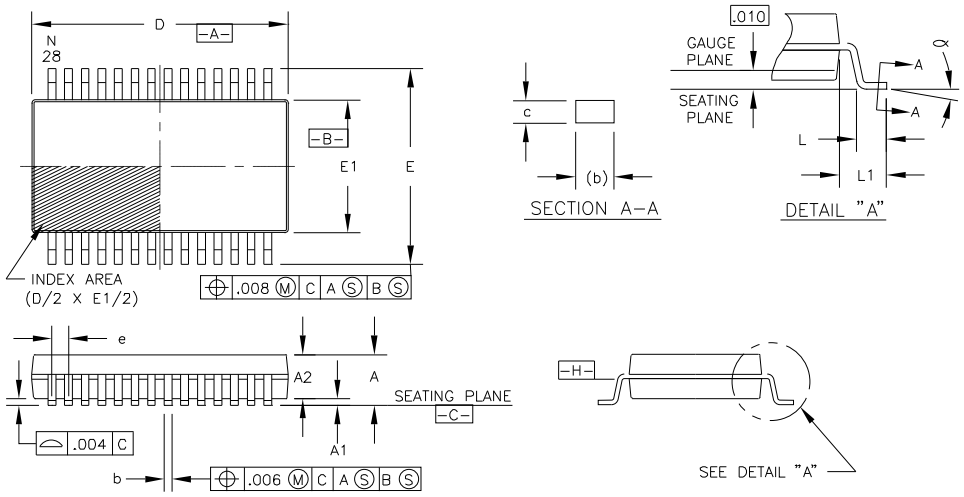
typical circuit connection



C_1 , C_2: Bypass Capacitor, 1 μF to 10 μF
C_3 , C_4: Bypass Capacitor, 0.01 μF to 0.1 μF
C_5 , C_6: OSC Capacitor, 10 to 33 pF
C_7: Loop Filter Capacitor, 0.022 μF
C_8: Ripple Capacitor, 0.0022 μF
R_1: OSC Resistor, 1 MΩ
R_2: Loop Filter Resistor, 6.8 kΩ

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

Package Number 324 - 28-Lead Plastic SSOP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.079	--	2.00	
A1	.002	--	0.05	--	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	3,7
c	.004	.010	0.09	0.25	7
D	.390	.413	9.90	10.50	2
E	.291	.323	7.40	8.20	
E1	.196	.220	5.00	5.60	2
e	.0256 BASIC		0.65 BASIC		
L	.022	.037	0.55	0.95	4
L1	.049 REF		1.25 REF		
N	28		28		5
θ	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ324	REV.: C
JEDEC NUMBER: MO-150	

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