ON THE DESIGN AND EXPERIMENTATION OF A HIGH PERFORMANCE 25A/48V RECTIFIER UNIT

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ABSTRACT

This paper focuses on a 25A/48V rectifier unit, to be applied as a battery charger for telecommunication applications.

The conceived unit is based on a modified version of the Full - Bridge Zero - Voltage Switching Pulse - Width - Modulated (FB-ZVS-PWM) DC/DC converter, which operates with no switching losses from no-load to full-load. This feature is achieved thanks to the employment of commutation auxiliary circuits, along with the dual-thyristor concept.

The input stage is composed of a single-phase AC-to-DC converter with two diodes and two thyristors, which limit the inrush current and is used to disconnect the unit from the line in the case of malfunction.

A 100kHz operational prototype has been designed, fabricated and successfully tested in laboratory.

The overall measured efficiency was 94% at full load.

Design procedure and example, along with experimental results are presented and discussed in the paper.

1.INTRODUCTION

Efforts have been made lately by designer engineers to replace the conventional rectifier units isolated by low frequency transformers and controlled by line commutated thyristors with high frequency switching mode converters. The purpose is to reduce size, cost and weight.

However, the users of such equipments argue that the use of high-frequency converters causes eletromagnetic interference problems, compromises the reliability and reduces the efficiency due to the commutation losses.

This paper discusses the design of a rectifier unit, based on a soft-commutation DC-DC converter, operating at constant frequency, conceived to overcome the above mentioned difficulties.

The block diagram of the conceived unit is represented in Fig.1.

(1) Front end AC/DC converter, composed of two diodes, two thyristors and input capacitor filter.

(2) Control circuit destinated to provide a soft charging of the input capacitor. The phase-angle of the thyristors increases slowly, limiting the inrush current.

(3) High performance DC/DC converter, using a modified version of the Full-Bridge Zero-voltage Switching Pulse-Width Modulated (FB-ZVS-PWM) Converter, operating at 100kHz, utilizing MOSFETs. The soft-commutation there exists from no-load to full-load.

The dual-thyristor concept is used, which prevents a MOSFET from turning-on before its voltage falls to zero. This method intrisically protects the commutation legs against short-circuit, increasing the system reliability.

(4) Output filter formed by high-frequency inductor and capacitor.

(5) This block contains: auxiliary power supply, isolated MOSFET drive circuits, regulation circuits and protection circuits.

(6) Load.

Design methodologies and experimental studies are presented hereafter.

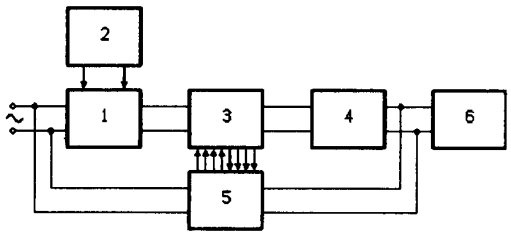


Fig.1: The block diagram of the conceived unit.

2. FRONT END STAGE

The input stage converts the AC line voltage to a DC voltage.

The two thyristors used in this stage provide a soft charging of the input filter capacitors. The phase-angle of the thyristors increases slowly, limiting the inrush current. At steady-state, the thyristors function as diodes.

As the MOSFETs of the DC-DC converter use dual-thyristor circuits, when the converter is turned on, the gate drive voltage must be active before V_{DS} is present. This can be done including a delay time on the trigger circuit of the input rectifier thyristors, which is shown in Fig.2.

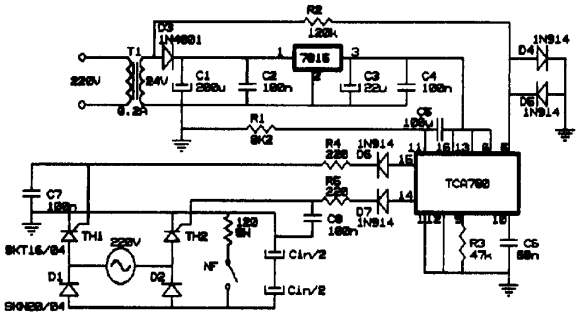


Fig.2: The input AC/DC converter with the thyristor trigger circuit.

At the turning off of the converter a relay provides a fast discharge for the input capacitors.The input filter capacitor voltage and the DC-bus input current experimentally obtained when the converter is turned on, are shown in Fig.3.

3. HIGH PERFORMANCE DC/DC CONVERTER

At power levels high enough and with high switching frequency for an off-line power supply, the FB-ZVS-PWM converter, shown in Fig.4 has been the best choice [1,2,3,4]. This converter presents the desirable output characteristics and low conduction

0-7803-0779-8/92 $3.00 © 1992 IEEE

losses as those of the hard switching PWM converters but with soft-commutation.

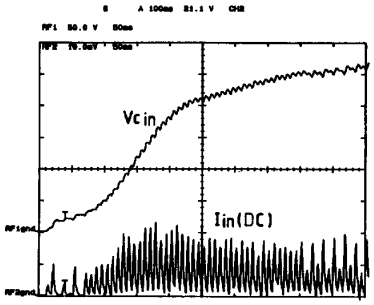


Fig.3: Filter capacitor voltage and DC bus current of the input AC/DC converter during the start transient.

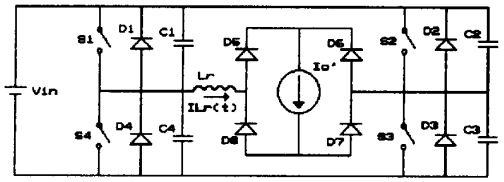


Fig.4: The power stage diagram of the FB-ZVS-PWM.

In spite of the several improvements of the FB-ZVS-PWM, it presents three major problems. The first is related to the switching losses of the output rectifier [2,5,6]. This topic will be discussed further ahead.

The second one, is related to the delay time, which there must be on the gate drive signal of the MOSFETs of the same leg, in order to ensure ZVS.

A fixed delay time has been used for each leg. However, the time interval in which the commutation occurs depends on the input DC voltage and on the output current.

Using a dual-thyristor concept [7], that delay time comes to be defined by the MOSFET drain-source voltage (V_{DS}). Fig.5 shows a gate drive circuit for a MOSFET using a dual-thyristor concept. As can be noticed, because of this circuit, the MOSFETs will be turned on only after Vds is reduced to a low value, defined by V_G, R_1 and R_2.

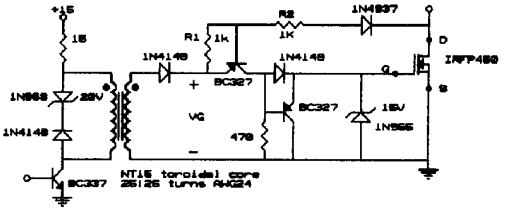


Fig.5: MOSFETS gate drive circuit using a dual thyristor concept.

Therefore, the dual-thyristor circuit adapts the delay time of each leg in order to perform ZVS. Besides that, it prevents leg short-circuit and MOSFETs overcurrent.

The last one, is related to the load range in which ZVS occurs. The transistors of one of the legs can only perform ZVS for a load current above a critical value. To perform ZVS for a wide load range, it is necessary to have great values of leakage inductance. However, to great values of this inductance, the rising and falling of the slope edges of the primary current reduce the duty-cycle available in the transformer secondary [3].

Using a modified version of the FB-ZVS-PWM, a high performance DC-DC converter is obtained. This converter uses MOSFETs operating at 100kHz.

Simply by introducing the commutation auxiliary circuits is achieved soft-commutations (ZVS) from no-load to full-load.

The power stage diagram of the proposed converter is shown in Fig.6, where L_1, L_2, C_{b1}, C_{b2}, R_1 and R_2 form the commutation auxiliary circuits.

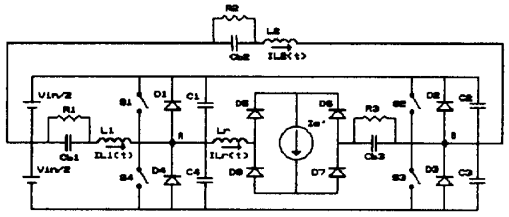


Fig.6: Power stage diagram of the proposed converter.

3.1. PRINCIPLE OF OPERATION

This converter is operated with a phase-shift between the two commutation legs, which provides ZVS for the switches.

The two legs of the bridge operate under different commutation conditions. The switches commutation of the left leg always takes place when the current through the primary of the transformer is equal to the output current reflected to the primary plus the current of the commutation auxiliary inductor L_1. As this inductor is greater than L_r, it can be considered that the charging and the discharging of the intrinsic capacitances occur in a linear fashion.

Yet, the switches commutation of the right leg is achieved with the transformer short-circuited by the output rectifier.

Thus, only the energy stored in the commutation auxiliary inductor L_2 and in the resonant inductor L_r are available to perform the commutation.

The values of the commutation auxiliary inductors are specified so that the ZVS is ensured at no-load.

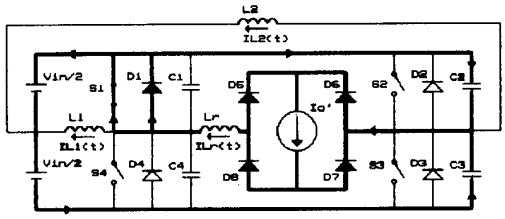
3.2. STAGES OF OPERATION AND WAVEFORMS

A half-cycle of the converter operation is described by six stages. The equivalent circuits of the stages are shown in Fig.7. The following assumptions are made in order to simplify the analysis:

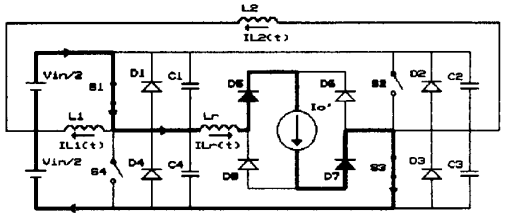
- all switches are ideal;
- blocking capacitors are considered short-circuits in the operation frequency;
- the output filter is represented as a current source;
- the MOSFETs output capacitances are equal and constant;
- the leakage inductance of the transformer is included in the inductance L_r;
- the magnetizing current of the transformer is negligible;
- the auxiliary commutation inductors are considered as current sources, as they are much greater than L_r;

The operation of the converter is described as follows:

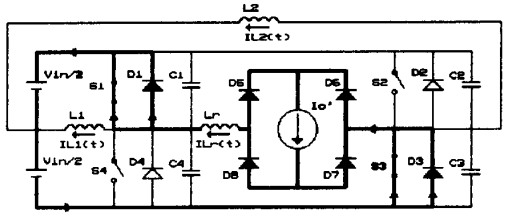
Before the instant t_o, the current I_o' was free-wheeling through diodes D_5-D_8 as well as the current i_{Lr} was free-wheeling through D_1, S_1 and S_2.



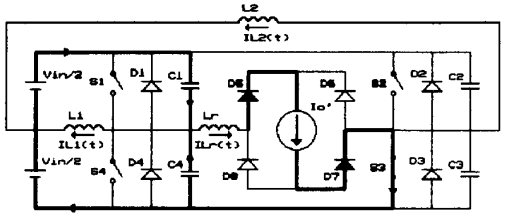
(t_0,t_1)



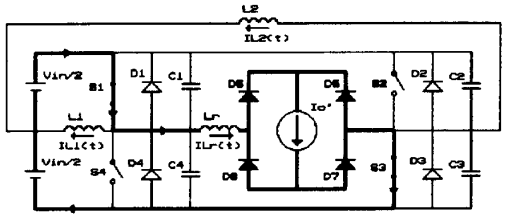
(t_3,t_4)



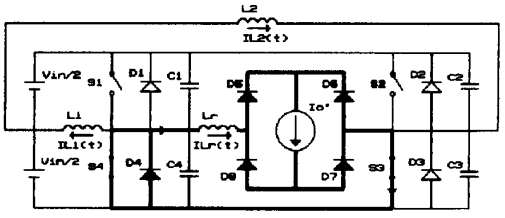
(t_1,t_2)



(t_4,t_5)



(t_2,t_3)



(t_5,t_6)

Fig.7: The stages of operation.

1st. stage - right leg commutation (t_o,t_1): at instant t_o, S_2 is turned off, v_{C2}, v_{C3} and i_{Lr} change in a resonant fashion until instant t_1, when v_{C3} becomes equal to zero. During this stage, L_2 is considered as a current source.

2nd. stage - linear decreasing (t_1,t_2): at the moment t_1, the diode D_3 starts to conduct; just after this, S_3 is turned on. During this stage the current i_{Lr} decreases linearly until t_2, when i_{Lr} reaches zero.

3rd. stage - lineaf increasing (t_2,t_3): during this stage the current i_{Lr} raises linearly through S_1 and S_2 . At the end of this stage, i_{Lr} reaches I_o' .

4th. stage - power transfer (t_3,t_4): during this stage, power is transfered from source V_{in} to the load through S_1, D_5, D_7 and S_3.

5th. stage - left leg commutation (t_4,t_5): at instant t_4, S_1 is turned off, v_{C1}, v_{C4} and i_{Lr} change in a linear fashion until instant t_5, when v_{C4} becomes equal to zero. During this stage, L_1 is considered as a current source.

6th.stage - free-wheeling (t_5,t_6): at instant t_5, diode D_4 starts to conduct and right after this, S_4 is turned on. During this stage the current I_o' keeps free-wheeling through diodes D_5-D_8 as well as the current i_{Lr} keeps free-wheeling through D_4, S_4 and S_3.

The main ideal waveforms, along with the gate drive signal, are shown in Fig.8.

3.3. RELEVANT ANALYSYS

3.3.1. OUTPUT CHARACTERISTICS

The linear variation of the current on the resonant inductor L_r, causes a reduction in the effective duty-cycle on the load, as shows Fig.8. This behavior is given by:

$$V_o = \left[D - \frac{4.f_s.(N_s/N_p).I_o.L_r}{V_{in}} \right] . \frac{N_s}{N_p} . V_{in} \qquad (1)$$

3.3.2. RIGHT LEG COMMUTATION

The right leg commutation always takes place when the load current I_o' free-wheels through output diodes. Thus, only the energy stored in L_r and L_2 are available to perform the commutation.

This commutation process is shown in Fig.9. At first, v_{C2}=0 and v_{C3}=V_{in}. During this process, the voltages v_{C2}, v_{C3} and the current i_{Lr} change in a resonant fashion until v_{C2}=V_{in} and v_{C3}=0. The relevant equations are:

$$L_r(t_o) = I_o' = (N_s/N_p).I_o \qquad (2)$$

$$i_{Lr}(t) = I_{L2p} - (I_{L2p} + I_o'). \cos w_r.t \qquad (3)$$

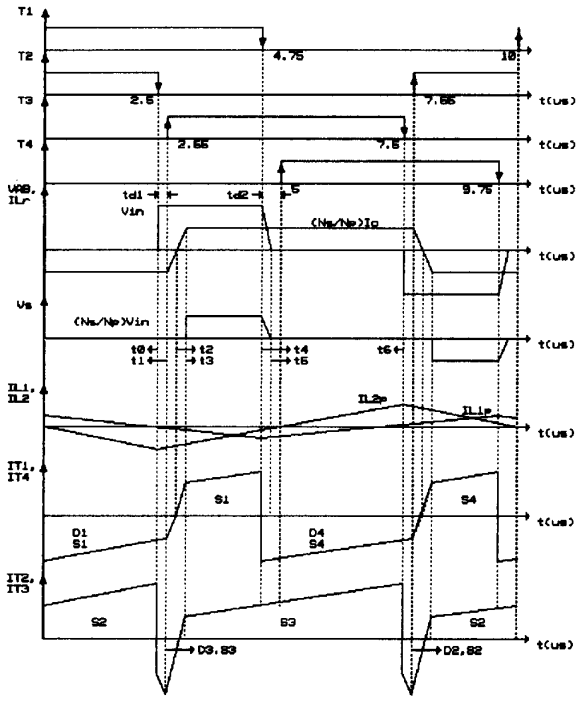


Fig.8: The main ideal wavefomrs and the gate drive signal.

$$v_{C2}(t) = Z_r \cdot (I_{L2p} + I_o').\ \text{sen}\ w_r.t \qquad (4)$$

$$C_2 + C_3 = C_1 + C_4 = C_r \qquad (5)$$

$$w_r = (C_r.L_r)^{-\frac{1}{2}} \qquad (6)$$

$$Z_r = (Lr/C_r)^{\frac{1}{2}} \qquad (7)$$

To ensure ZVS of T_3 for all load conditions, the current I_{L1p}, obtained from equation (4) when $I_o'=0$, must be:

$$I_{L2P} = \frac{V_{in(max)}}{Zr} \qquad (8)$$

With delay time td_1 given by:

$$td_1 \geq \frac{T}{2}(C_r.L_r)^{\frac{1}{2}} \qquad (9)$$

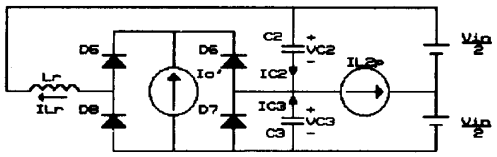


Fig.9: Right leg commutation.

3.3.3. LEFT LEG COMMUTATION

The left leg commutation always occurs when the load current I_o' is active. This commutation process is shown in detail in Fig.10. At the beginning, $v_{C1}=0$ and $v_{C4}=V_{in}$.

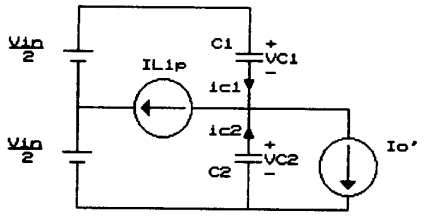


Fig.10: Left leg commutation.

During this process, the voltages v_{C1} and v_{C4} change linearly until $v_{C1}=V_{in}$ and $v_{C4}=0$. The relevant equations are:

$$V_{C1}(t) = \frac{(I_o'+I_{L1p})t_2}{C_r} \qquad (10)$$

$$t_2 = \frac{C_r \cdot V_{in(max)}}{I_o' + I_{L1p}} \qquad (11)$$

To ensure ZVS of T_4 for all load conditions, the delay time td_2, obtained from equation (11) when $I_o'=0$, must be:

$$td_2 \geq \frac{C_r.V_{in}}{I_{L1p}} \qquad (12)$$

As the left leg commutation is less critical than the right one, the current I_{L1p} can be smaller than I_{L2p}. This condition can be obtained by:

$$td_2 \geq td_1 \qquad (13)$$

The td_{2max} is defined at full load, when the duty-cycle is maximum and t_2 is minimum. Then, td_{2max} must be smaller than the time interval of left leg commutation plus the time interval of linear decreasing. This condition is given by:

$$td_{2max} \leq \frac{C_r.V_{in(max)}}{I_o' + I_{L1p}} + \frac{L_r.I_o'}{V_{in}} \qquad (14)$$

3.4. DESIGN PROCEDURE AND EXAMPLE

The conventional full-bridge hard switching design procedure with flux swing limited is employed to design the transformer and the inductors [8]. Using this method, the maximum swing temperature reached by these elements was 40°C. A practical design is given as follows:

a. Transformer:

a.1. The core area product is calculated using this equation:

$$Ae.Aw = \frac{P_{in(max)} \times 10^4}{K_t.K_u.K_p.J_{max}B_{max}.f_s}\ cm^4 \qquad (15)$$

where:

$P_{in(max)} = P_{o(max)}/N = 1600$ W
$N = 0.9$ (efficiency)
$P_{o(max)} = V_{o(max)}.I_o = 57.6 \times 25 = 1440$ W
$K_t = I_{in(dc)}/I_{p(rms)}$ (topology factor)
K_u = window utilization factor
K_p = primary area factor
$K_t = 1$; $K_u = 0.4$ and $K_p = 0.41$ for full bridge
$J_{max} = 300$ A/cm^2 (current density)
$B_{max} = 0.12$ T (flux swing)
$f_s = 100$ kHz (switching frequency).

With these values, Ae.Aw = 27 cm^4. It was chosen a ferrite core E-65/39 IP-6 THORNTON whose parameters are:
Ae = 7.98 cm^2 and Aw = 3.70 cm^2

a.2. The minimum number of primary turns is calculated from the equation below:

$$N_p \geq \frac{V_{in(min)}}{2.AeB.f_s} \qquad (16)$$

Assuming $V_{in(min)}$= 240 V one obtains $N_p \geq 12.5$ turns.

a.3. The turns ratio n is calculated by:

$$n = \frac{N_p}{N_s} = \frac{0.9\ [\ V_{in(min)} - V_F\ ].\ D_{max}}{V_{o(max)} + V_F} \qquad (17)$$

where:
V_F = 1V (rectifier forward drop)
D_{max} = 0.8 (maximum duty-cycle)
So, n = 3.

a.4. Number of turns for the secondary:

N_s = Integer (N_p/n) = 5 turns (26 x AWG 24).
Recalculating the number of turns for the primary:
N_p = n . N_s = 15 turns (13 x AWG 24).
The measured parameters on the primary of the transformer were:
L_m = 400uH (magnetizing inductance)
L_{lk} = 3uH (leakage inductance)

b. Selection of the series inductor L_r

This selection is done considering the duty-cycle reduction from equation (1). However, when selecting L_r, one must consider that the smaller L_r, the greater the current I_{L2p} must be, as shows equations (8).
Assuming the duty-cycle reduction is equal to 0,15.

$$L_r = \frac{0.15.\ V_{in(min)}}{4.f_s.(N_s/N_p).I_o} = \frac{0.15 \times 240}{4.100x10^3.(3/15).25} = 11uH$$

Subtracting the 3uH measured from the leakage inductance, one obtains: L_r = 8uH.

c. Selection of inductor L_2:

Using equations (7) and (8) with C_r=800pF, L_r=11uH and $V_{in(max)}$= 340V, one obtains I_{L2p} = 2.9A. Thus, the inductor L_2 is obtained from the following equation:

$$L_2 = \frac{V_{in(max)}/2}{4.f_s.I_{L2p}} = \frac{340/2}{4.100x10^3.\ 2.9} = 146uH$$

d. Selection of the delay time td_1

Using equation (9), one obtains:
$td_1 \geq 147nS$
thus, td_1 = 150nS

e. Selection of the delay time td_2

From equation (13), it was assumed that:
td_2 = 250nS

f. Selection of the inductor L_1:

Using equation (12), one obtains I_{L1p} = 1 A. Thus, L_1 is obtained from the following equation:

$$L_1 = \frac{V_{in(max)}/2}{4.f_s.I_{L1p}} = \frac{340/2}{4.100x10^3.1} = 425uH$$

The chosen value of td_2 must satisfy equation (14).

Thus, td_2 = 250nS < td_{2max} = 300nS.

g. Output filter inductor

The selection of the filter inductor must be done to prevent discontinuous mode operation upon minimum load current. It can be obtained using the equation below:

$$L_o = \frac{(V_{o(max)} + V_F)\ .\ (1 - D_{min})}{2.f_s.\ \Delta I_{L(max)}} \qquad (18)$$

where:

$$D_{min} = \frac{N_p.(V_{o(min)} + V_F)}{N_s.V_{in(max)}} = 0.475$$

Assuming $\Delta I_{L(max)} = I_o/10$ = 2.5 A, one obtains:
L_o = 61uH

h. Output filter capacitor

The filter capacitor to achieve the output voltage specification of ΔV_o = 0.2 V is :

$$C_o = \frac{\Delta I_{L(max)}}{8.f_s.\ \Delta V_o} = 15uF$$

The maximum equivalent series resistance (ESR) of the capacitor is:

$$ESR = \Delta V_o\ /\ \Delta I_{L(max)} = 0.08\ ohms$$

To obtain the necessary ESR, four 220uF capacitors associated in parallel were used.

i. Blocking capacitor in series with the transformer

This selection is done considering the maximum voltage drop on this capacitor under $V_{in(min)}$. It can be obtained from the following equation:

$$C_b = \frac{(N_s/N_p).\ I_o}{2.f_s.\ \Delta V_{c(max)}} \qquad (19)$$

Assuming $\Delta V_{(max)} = 0.04\ V_{in(min)}$ = 9.6 V, one obtains:
C_b = 5uF

j. Blocking capacitors of the commutation auxiliary circuits

They can be obtained using the equation below:

$$C_{b(aux)} = \frac{I_{Lp}}{4.f_s.\ \Delta V_{c(max)}} \qquad (20)$$

Considering $I_{Lp} = I_{Lp(max)}$ = 2.9 A and $\Delta V_{c(max)}$= 0.04 $V_{in(min)}/2$ = 4.8 V, one obtains:
$C_{b1} = C_{b2}$ = 2uF

k. Damping resistor

A resistor in paralell with the blocking capacitor provides a simple but effective method for preventing both duty-cycle unbalance and low-frequency oscillations between the blocking capacitor and the magnetizing inductance [9].
The damping resistor in series with the transformer can be obtained from the equation below:

$$R_d = \frac{V_{in(min)}}{D_{max}.(N_s/N_p).I_o} = \frac{240}{0.8.(5/15).25} = 33 \text{ ohms}$$

Yet, the damping resistors of the blocking capacitors of the commutation auxiliary circuits are obtained from the following equation:

$$R_{d1} = R_{d2} = \frac{V_{in(min)}/2}{I_{Lp(max)}} = \frac{240/2}{2.9} = 39 \text{ ohms}$$

l. Selection of the switches

The MOSFETs selection to perform ZVS at high frequency must be done considering:

- the maximum drain-source voltage across the switches - $V_{DS(max)}$;
- the rated rms drain current at the operating temperature - I_{Drms} ;
- the peak current - I_{Dpk} ;
- the drain resistance at the operating temperature - R_{DSon} ;
- the input and output intrinsic capacitances of the switches - c_{iss} and c_{oss};
- the turn-on time - t_{on} ;

Considering the following design parameters:

$V_{DS(max)} = V_{in(max)} = 340$ V

$I_{D(rms)} = 6$ A $\quad I_{D(pk)} = 8.4$ A $\quad T = 100°C$

The IRFP450 MOSFET was chosen as it meets the above mentioned requirements and presents the following characteristics:

$V_{DS(max)} = 500$ V $\quad I_{D(100C)} = 8.8$ A $\quad I_{Dpk} = 56A$

$R_{DSon(100°C)} = 0.65\Omega \quad t_{on} = 93uS$

$c_{iss} = 2000pF \quad c_{oss} = 400pF$

m. Calculation the heat sink

m.1 MOSFETs

The heat sink thermal resistance is calculated as follows:

$$R_{\theta JA} = \frac{\Delta T_j}{P_D} - R_{\theta JC} - R_{\theta CS} \qquad (21)$$

where:

$P_D = R_{DSon} \cdot I_D^2(rms) = 25.2$ W

$R_{\theta JC} = 0.7°C/W$ (IRFP450)

$R_{\theta CS} = 0.2°C/W$

Assuming $\Delta T_J = 60°C$, $R_{\theta JA} = 1.7°C/W$

m.2 Output rectifier diodes

Using equation (21) with:

$P_D = V_F \cdot I_F = 1 \cdot 12.5 = 12.5$ W,

$R_{\theta JC} = 1.5°C/W$ (MUR1530) and $R_{\theta CS} = 0.2°C/W$, one obtains:

$R_{\theta JA} = 3.1°C/W$

n. Selection of the output rectifier diodes

To reduce the switching losses on the rectifier diodes, the ultra-fast diodes were selected. The interaction of the reverse-recovery process of the rectifier with the leakage inductance of the tranformer secondary causes voltage overshoot and ringing.

A voltage clamp circuit can be used to limit the maximum voltage across the diodes [2]. This circuit can be selected using the equations below:

$$V_{s(max)} = (Ns / N_p) \cdot V_{in(max)} \qquad (22)$$

$$P_{cp} = f_s.C_d.(2.V_{s(max)})^2 \cdot \frac{(1+u)^2.(1-u)}{u} \qquad (23)$$

$$u = \frac{V_{cp} - 2.V_{s(max)}}{2.V_{s(max)}} \qquad (24)$$

where:

V_s - transformer secondary voltage

V_{cp} - clamping voltage

P_{cp} - power on the clamping circuit

C_d - diode capacitance

Considering $V_{in(max)}$=340 V , C_d = 200pF and assuming V_{cp} = 280V,one obtains:

$P_{cp} = 5.3$ W and $R_{cp} = V_{cp}^2/P_{cp} = 15$k ohms.

As, the voltage across the output rectifier diodes is clamped at V_{cp} = 280 V and the mean current is equal to $I_o/2$, a MUR1530 ultra-fast diode was chosen, which presents the following characteristics: I_F = 15 A, V_R = 300 V and t_{rr} = 60nS.

3.5 CONTROL LOOP

The control circuit is based on the IC 3524, where a control voltage V_C is compared to a sawtooth voltage V_D, establishing a PWM. Another three ICs, (IC4528-Monostable, IC 4013-D Flip-Flop and IC 4001-Nor-Gate) convert the PWM to phase- shift signals to the MOSFETs gate drive circuits.

Two control loops operate in paralell. From no-load to full-load only the voltage loop is active. When an overload occurs, the current loop maintains the output current constant. Another way for the current loop to operate is in fold-back mode.

3.5.1 VOLTAGE LOOP

Considering the DC gain presented by equation (1) along with the duty-cycle provided by the PWM IC equal to $D = V_C/V_D$, the control to output transfer function is given by the following equation:

$$\frac{V_o(s)}{V_c(s)} = \frac{K_1}{1 + K_2/R_o} \cdot \frac{1 + s/w_z}{1 + (s/w_o)/Q + (s/w_o)^2} \qquad (25)$$

where:

$$K_1 = \frac{(N_s/N_p).\ V_{in}}{V_D} \qquad (26)$$

$$K_2 = 4.f_s.L_r.(N_s/N_p)^2 \qquad (27)$$

$$w_o = (L_o.C_o)^{-\frac{1}{2}} \qquad (28)$$

w_o - output filter resonant frequency

$$w_Z = \frac{1}{RSE \cdot C_o} \qquad (29)$$

w_Z - RSE capacitor frequency

$$Q = \frac{1}{w_o.((Lo/R_o) + RSE.C_o)} \qquad (30)$$

Q - Quality factor

The well-known two pole compensation network was used in order to achieve good dynamic response, line and load regulation and stability. The voltage closed-loop can be stablized using the Root-Locus method or Bode plots [8].

The voltage compensation network used is shown in Fig.11.

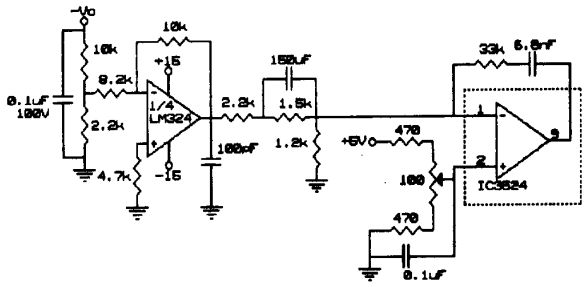


Fig.11: Voltage compensator network.

3.5.2 CURRENT LOOP

The control to output function is obtained from equation (25) being the DC gain divided by R_o. Either a two pole compensation network or a simple PI compensation can be used to obtain the desired performance. The current compensation network used is shown in Fig.12.

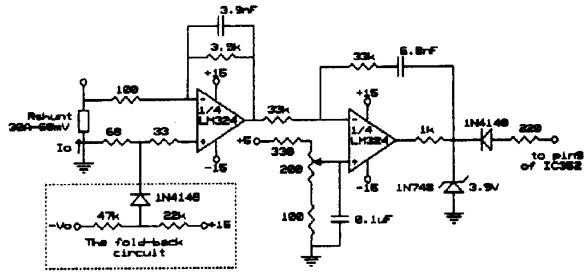


Fig.12: Current compensator network.

4. EXPERIMENTAL RESULTS

A prototype was built as to meet the following basic requirements:

- input voltage: 220 V ± 15%, 60 Hz
- output voltage: 52.8/57.6 V - DC
- rated output current: 25 A
- efficiency: greater than 0.9
- natural convection cooling
- maximum output voltage static error: 1%
- spike noise: < 200mV p-p
- AC ripple: < $48mV_{rms}$
- Psophometric noise: < 2mV

The complete power stage diagram is shown in Fig.13.

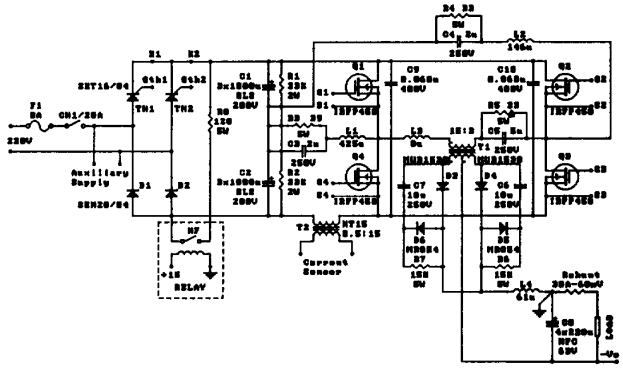


Fig.13: The complete power stage diagram.

The ZVS on switches of the right and left leg are shown in Fig.14 and the voltage V_{AB} and the current I_{Lr} are shown in Fig.15 for: V_{in} = 270 V, I_{in} = 4.8 A, V_o = 57 V and I_o = 20.4 A. Fig.16 shows the output rectifier voltage. The output AC ripple and the spike noise are shown in Fig.17. The open-loop and closed-loop output characteristics are shown in Fig.18. The efficiency at rated AC input voltage and output current is shown in Fig.19.

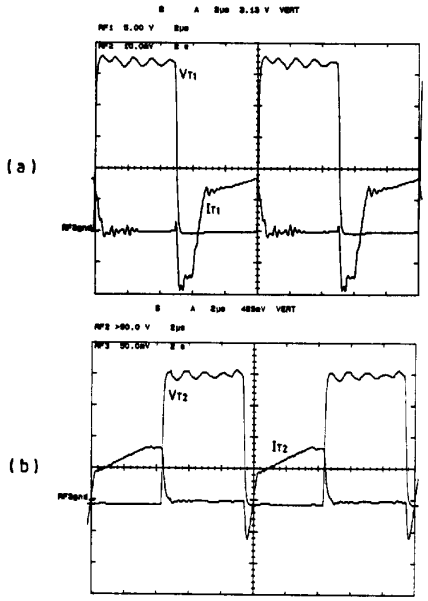


Fig. 14: The commutation of the switches: (a) right leg, V_{T1}(65V/div) and I_{T1}(5A/div); (b) left leg, V_{T2}(50V/div) and I_{T2} (5A/div); time scale: 2us/div.

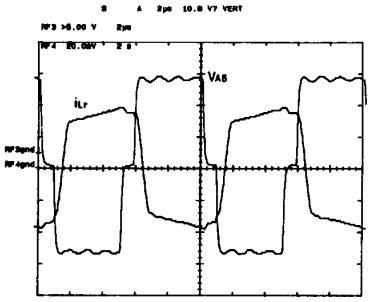


Fig. 15: The voltage V_{AB} (100V/div) and the resonant current i_{Lr} (4A/div), time scale: 2us/div.

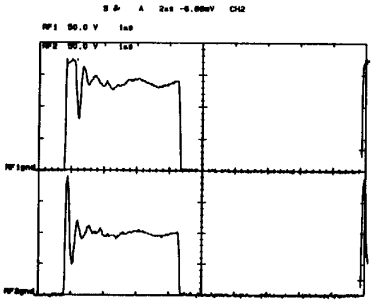


Fig.16: Output diode voltage (50v/div), upper trace : with clamp circuit, lower trace: without clamp circuit.

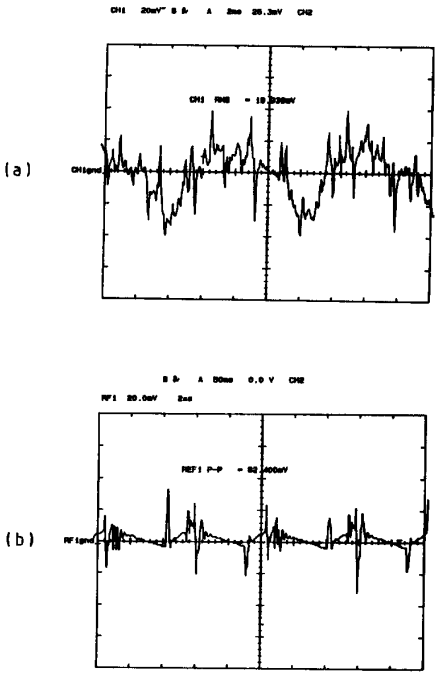


Fig.17: (a) Output AC ripple, (b) Output spike noise.

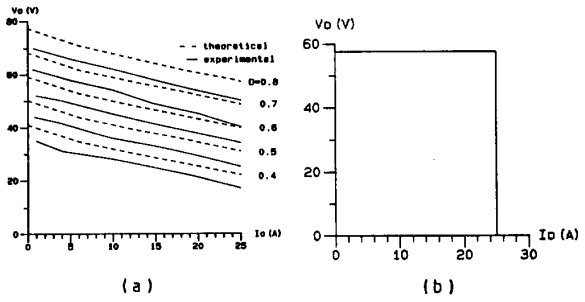


Fig.18: Output characteristics: (a) open-loop, (b) close-loop.

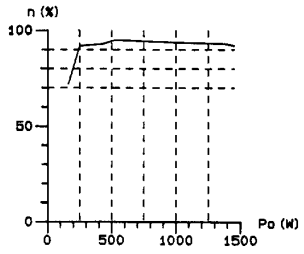


Fig.19: Efficiency.

CONCLUSION

From the studies performed during the development of the 48V/25A rectifier unit presented and discussed in this paper, the authors concluded that it is ready to replace the conventional thyristor based equipments.

Brazilian industries are preparing units to be tested in the field, in telecommunication companies, during 1992.

Currently, the authors are working to improve some characteristics of the unit, such as parallel operation and incorporation of soft commutation active power factor correction.

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