Data Sheet | January 2000 | File Number 4819

Synchronous-Rectified Buck MOSFET Drivers

The HIP6601 and HIP6603 are high frequency, dual MOSFET drivers specifically designed to drive two power N-Channel MOSFETs in a synchronous-rectified buck converter topology. These drivers combined with a HIP630x Multi-Phase Buck PWM controller and Intersil UltraFETs™ form a complete core-voltage regulator solution for advanced microprocessors.

The HIP6601 drives the lower gate in a synchronous-rectifier bridge to 12V, while the upper gate can be independently driven over a range from 5V to 12V. The HIP6603 drives both upper and lower gates over a range of 5V to 12V. This drive-voltage flexibility provides the advantage of optimizing applications involving trade-offs between switching losses and conduction losses.

The output drivers in the HIP6601 and HIP6603 have the capacity to efficiently switch power MOSFETs at frequencies up to 2MHz. Each driver is capable of driving a 3000pF load with a 30ns propagation delay and 50ns transition time. Both products implement bootstrapping on the upper gate with only an external capacitor required. This reduces implementation complexity and allows the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP6601CB	0 to 85	8 Ld SOIC	M8.15
HIP6603CB	0 to 85	8 Ld SOIC	M8.15

Features

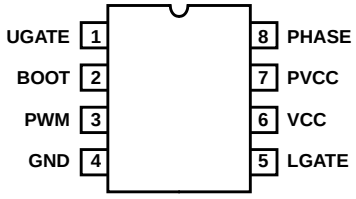
- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- Internal Bootstrap Device
- Supports High Switching Frequency
  - Fast Output Rise Time
  - Propagation Delay 30ns
- Small 8 Lead SOIC Package
- Dual Gate-Drive Voltages for Optimal Efficiency
- Three-State Input for Bridge Shutdown
- Supply Under Voltage Protection

Applications

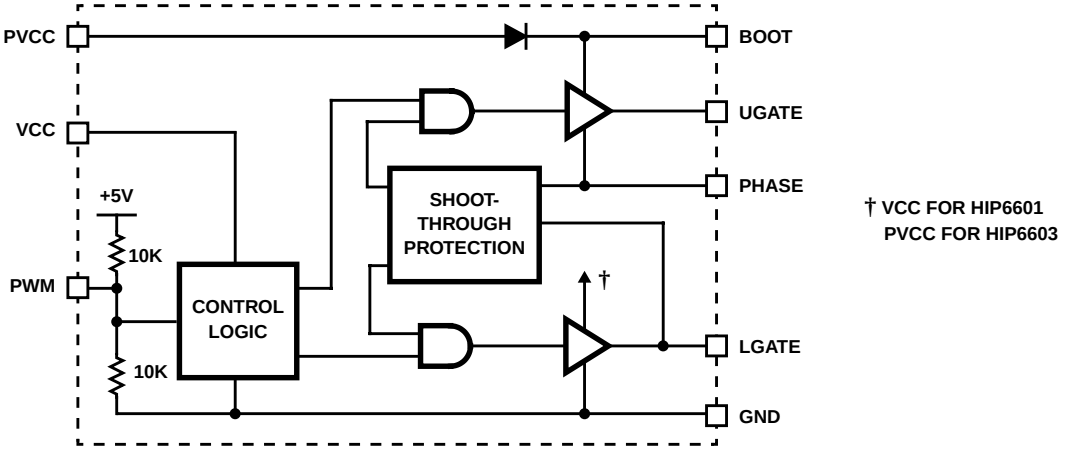
- Core Voltage Supplies for Intel Pentium® III, AMD® Athlon™ Microprocessors
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters

Pinout

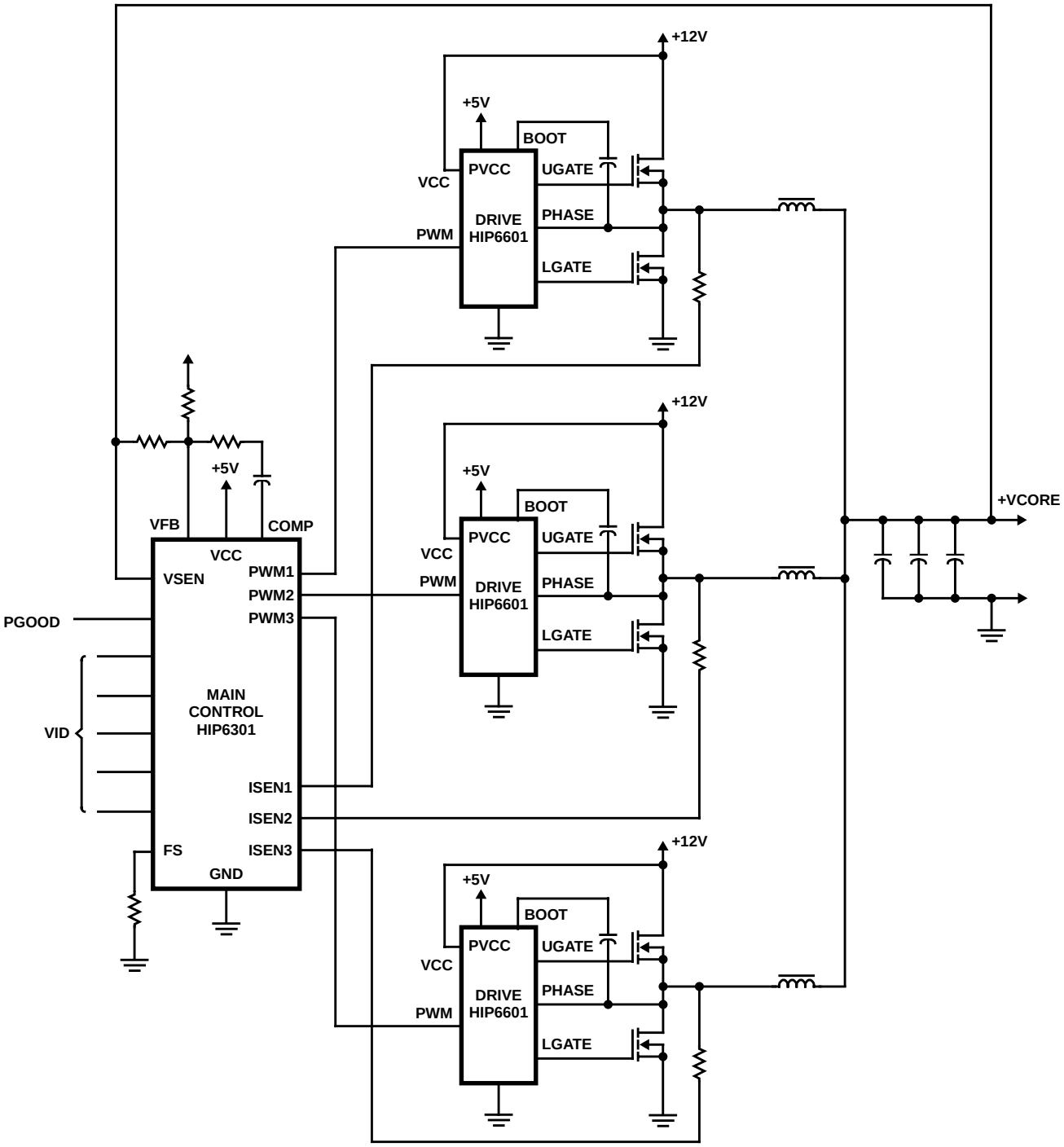
HIP6601CB/HIP6603CB
(SOIC)
TOP VIEW



Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage (VCC) 15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage (V_{BOOT} - V_{PHASE}) 15V
Input Voltage (V_{PWM}) . . . . . .GND - 0.3V to 7V
UGATE . . . . . .V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
LGATE . . . . . .GND - 0.3V to V_{PVCC} + 0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per EIAJ ED-4701 Method C-111). 200V

Operating Conditions

Ambient Temperature Range . . . . . 0^oC to 85^oC
Maximum Operating Junction Temperature . . . . . 125^oC
Supply Voltage, VCC . . . . . 12V ±10%
Supply Voltage Range, PVCC . . . . . .5V to 12V

Thermal Information

Thermal Resistance θ_{JA} ($^oC/W$)
SOIC Package 113
Maximum Junction Temperature (Plastic Package) . . . . . .150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . .300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	HIP6601, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	4.4	6.2	mA
		HIP6603, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	2.5	3.6	mA
Power Supply Current	I_{PVCC}	HIP6601, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	200	430	µA
		HIP6603, f_{PWM} = 1MHz, V_{PVCC} = 12V	-	1.8	3.3	mA
POWER-ON RESET						
VCC Rising Threshold			9.7	9.9	10.0	V
VCC Falling Threshold			9.0	9.1	9.2	V
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 0 or 5V (See Block Diagram)	-	500	-	µA
PWM Rising Threshold			3.6	3.7	-	V
PWM Falling Threshold			-	1.3	1.4	V
UGATE Rise Time	TR_{UGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	-	20	-	ns
LGATE Rise Time	TR_{LGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	-	50	-	ns
UGATE Fall Time	TF_{UGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	-	20	-	ns
LGATE Fall Time	TF_{LGATE}	V_{PVCC} = V_{VCC} = 12V, 3nF load	-	20	-	ns
UGATE Turn-Off Propagation Delay	$TPDL_{UGATE}$	V_{VCC} = V_{PVCC} = 12V, 3nF load	-	30	-	ns
LGATE Turn-Off Propagation Delay	$TPDL_{LGATE}$	V_{VCC} = V_{PVCC} = 12V, 3nF load	-	20	-	ns
Shutdown Window			1.5	-	3.6	V
Shutdown Holdoff Time			-	230	-	ns
OUTPUT						
Upper Drive Source Impedance	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	-	2.5	3.0	Ω
		V_{VCC} = V_{PVCC} = 12V	-	7.0	7.5	Ω
Upper Drive Sink Impedance	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	-	2.3	2.8	Ω
		V_{VCC} = 12V, V_{PVCC} = 12V	-	1.0	1.3	Ω
Lower Drive Source Impedance	R_{LGATE}	V_{VCC} = 12V, V_{PVCC} = 5V	-	4.5	5.0	Ω
		V_{VCC} = 12V, V_{PVCC} = 12V	-	9.0	9.5	Ω
Lower Drive Sink Impedance	R_{LGATE}	V_{VCC} = V_{PVCC} = 12V	-	1.5	2.9	Ω

Functional Pin Description

UGATE (Pin 1)

Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.

BOOT (Pin 2)

Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

PWM (Pin 3)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.

GND (Pin 4)

Bias and reference ground. All signals are referenced to this node.

LGATE (Pin 5)

Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

VCC (Pin 6)

Connect this pin to a +12V bias supply. Place a high quality bypass capacitor from this pin to GND.

PVCC (Pin 7)

For the HIP6601, this pin supplies the upper gate drive bias. Connect this pin from +12V down to +5V.

For the HIP6603, this pin supplies both the upper and lower gate drive bias. Connect this pin to either +12V or +5V.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. The PHASE voltage is monitored for adaptive shoot-through protection. This pin also provides a return path for the upper gate drive.

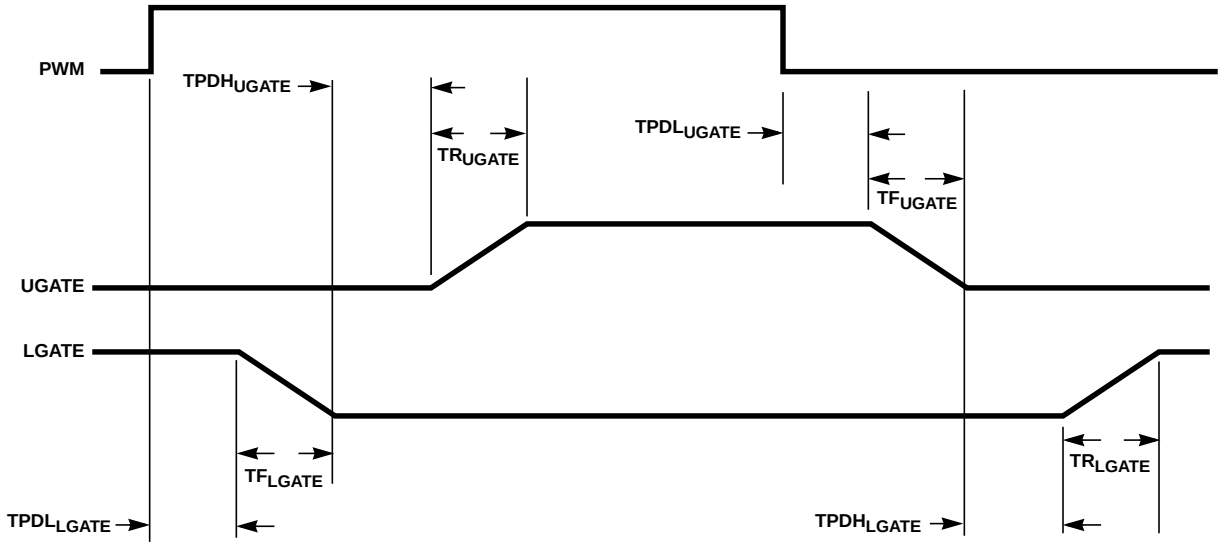
Description

Operation

Designed for versatility and speed, the HIP6601 and HIP6603 dual MOSFET drivers control both high-side and low-side N-Channel FETs from one externally provided PWM signal.

The upper and lower gates are held low until the driver is initialized. Once the VCC voltage surpasses the VCC Rising Threshold (See Electrical Specifications), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [$TPDL_{LGATE}$], the lower gate begins to fall. Typical fall times [TF_{LGATE}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$TPDH_{UGATE}$] based on how quickly the LGATE voltage drops below 1.0V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is complete the upper gate drive begins to rise [TR_{UGATE}] and the upper MOSFET turns on.

Timing Diagram



A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$TPDL_{UGATE}$] is encountered before the upper gate begins to fall [TF_{UGATE}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $TPDH_{LGATE}$. The PHASE voltage is monitored and the lower gate is allowed to rise after PHASE drops below 0.5V. The lower gate then rises [TR_{LGATE}], turning on the lower MOSFET.

Three-State PWM Input

A unique feature of the HIP660X drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1.0V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the PHASE voltage during UGATE turn-off. Once PHASE has dropped below a threshold of 0.5V, the LGATE is allowed to rise. PHASE continues to be monitored during the lower gate rise time. If the PHASE voltage exceeds the 0.5V threshold during this period and remains high for longer than 2µs, the LGATE transitions low. Both upper and lower gates are then held low until the next rising edge of the PWM signal.

Power-On Reset (POR) Function

During initial startup, the VCC voltage rise is monitored and gate drives are held low until a typical VCC rising threshold of 9.9V is reached. Once the rising VCC threshold is exceeded, the PWM input signal takes control of the gate drives. If VCC drops below a typical VCC falling threshold of 9.1V during operation, then both gate drives are again held low. This condition persists until the VCC voltage exceeds the VCC rising threshold.

Internal Bootstrap Device

Both drivers feature an internal bootstrap device. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above VCC + 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

Where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose a HUF76139 is chosen as the upper MOSFET. The gate charge, Q_{GATE}, from the data sheet is 65nC for a 10V upper gate drive. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.325µF is required. The next larger standard value capacitance is 0.33µF.

Gate Drive Voltage Versatility

The HIP6601 and HIP6603 provide the user total flexibility in choosing the gate drive voltage. The HIP6601 lower gate drive is fixed to VCC [+12V], but the upper drive rail can range from 12V down to 5V depending on what voltage is applied to PVCC. The HIP6603 ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC will set both driver rail voltages.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as:

$$P = 1.05 f_{sw}\left(\frac{3}{2} V_U Q_U + V_L Q_L\right) + I_{DDQ} V_{CC}$$

where f_{SW} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The I_{DDQ} V_{CC} product is the quiescent power of the driver and is typically 30mW.

The power dissipation approximation is a result of power transferred to and from the upper and lower gates. But, the internal bootstrap device also dissipates power on-chip during the refresh cycle. Expressing this power in terms of the upper MOSFET total gate charge is explained below.

The bootstrap device conducts when the lower MOSFET or it's body diode conducts and pulls the PHASE node toward GND. While the bootstrap device conducts, a current path is formed that refreshes the bootstrap capacitor. Since the upper gate is driving a MOSFET, the charge removed from the bootstrap capacitor is equivalent to the total gate charge of the MOSFET. Therefore, the refresh power required by the bootstrap capacitor is equivalent to the power used to charge the gate capacitance of the MOSFET.

$$P_{REFRESH} = \frac{1}{2} f_{SW} Q_{LOSS} V_{PVCC} = \frac{1}{2} f_{SW} Q_U V_U$$

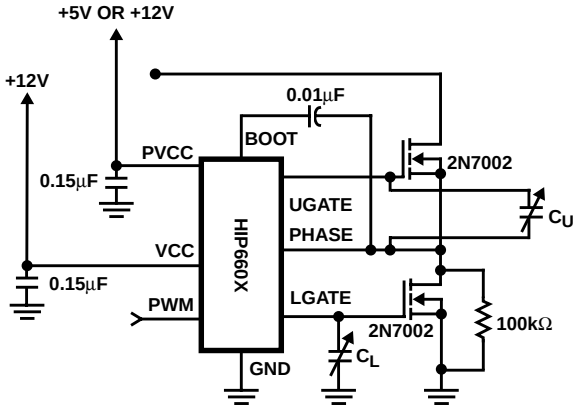
where Q_{LOSS} is the total charge removed from the bootstrap capacitor and provided to the upper gate load.

The 1.05 factor is a correction factor derived from the following characterization. The base circuit for characterizing the drivers for different loading profiles and frequencies is provided. C_U and C_L are the upper and lower gate load capacitors. Decoupling capacitors [0.15µF] are added to the PVCC and VCC pins. The bootstrap capacitor value is 0.01µF.

In Figure 1, C_U and C_L values are the same and frequency is varied from 50kHz to 2MHz. PVCC and VCC are tied together to a +12V supply. Curves do exceed the 800mW cutoff, but continuous operation above this point is not recommended.

Figure 2 shows the dissipation in the driver with 3nF loading on both gates and each individually. Note the higher upper gate power dissipation which is due to the bootstrap device refresh cycle. Again PVCC and VCC are tied together and to a +12V supply.

Test Circuit



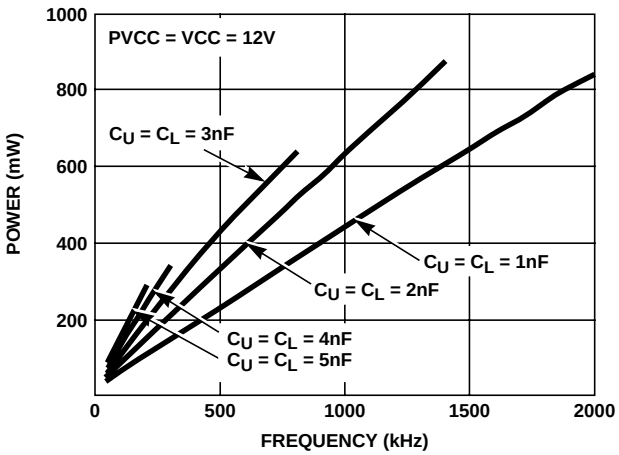


FIGURE 1. POWER DISSIPATION vs FREQUENCY

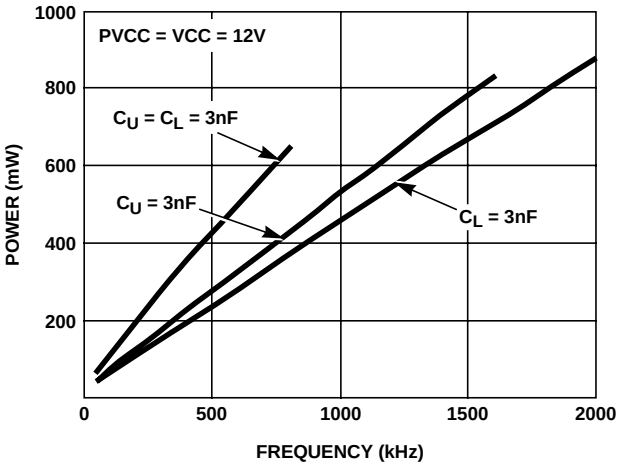


FIGURE 2. 3nF LOADING PROFILE

The impact of loading on power dissipation is shown in Figure 3. Frequency is held constant while the gate capacitors are varied from 1nF to 5nF. VCC and PVCC are tied together and to a +12V supply. Figures 4 through 6 show the same characterization for the HIP6603 with a +5V supply on PVCC and VCC tied to a +12V supply.

Since both upper and lower gate capacitance can vary, Figure 7 shows dissipation curves versus lower gate capacitance with upper gate capacitance held constant at three different values. These curves apply only to the HIP6601 due to power supply configuration.

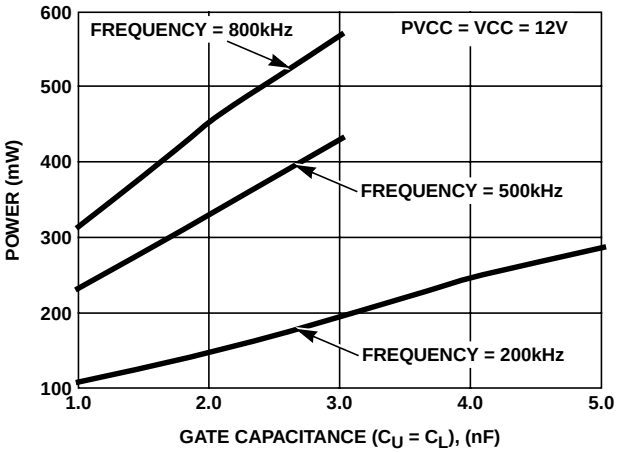


FIGURE 3. POWER DISSIPATION vs LOADING

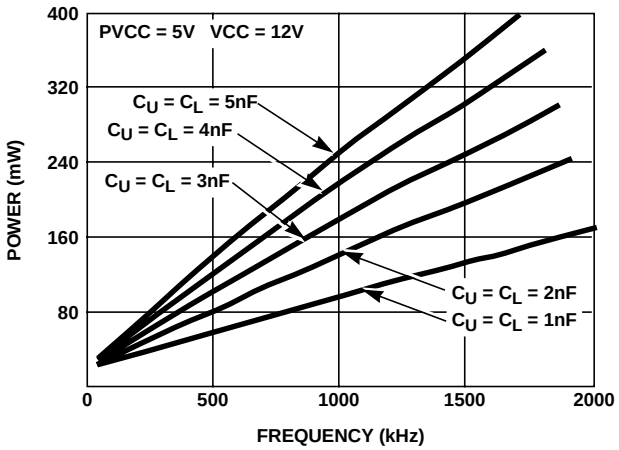


FIGURE 4. POWER DISSIPATION vs FREQUENCY (HIP6603)

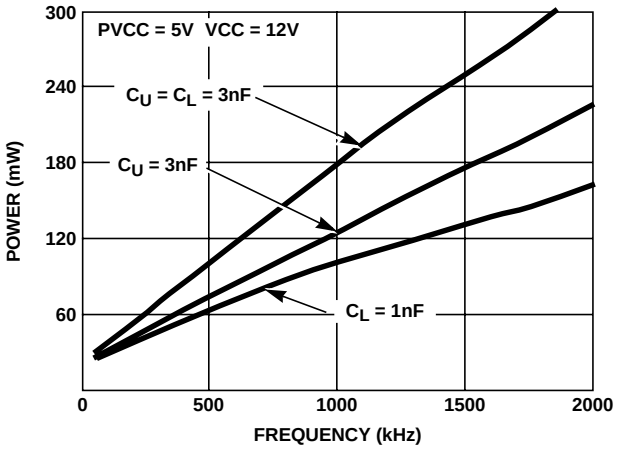


FIGURE 5. 3nF LOADING PROFILE (HIP6603)

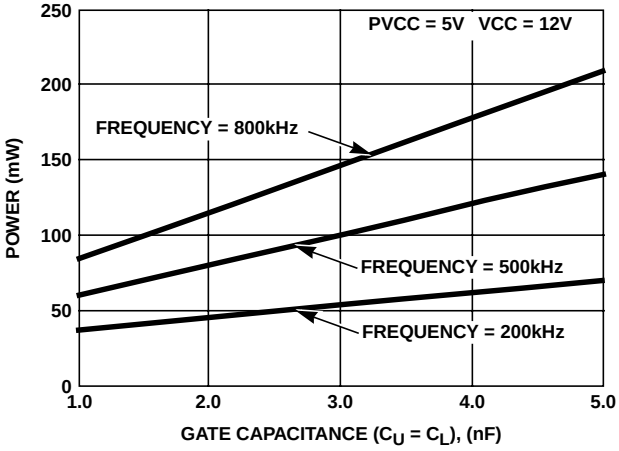


FIGURE 6. VARIABLE LOADING PROFILE (HIP6603)

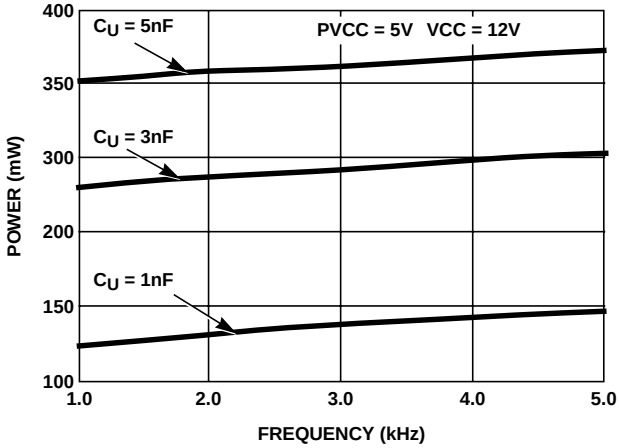
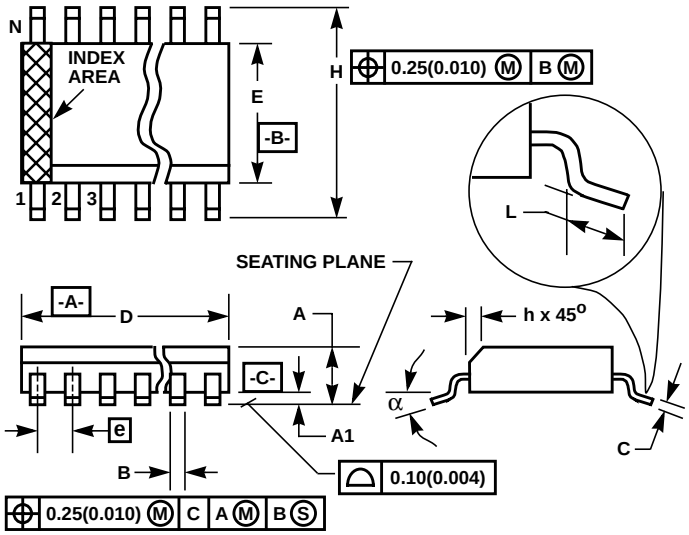


FIGURE 7. POWER DISSIPATION vs LOADING (HIP6601)

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029