ATJ2091H PRODUCT DATA SHEET

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1. Introduction

ATJ2091H is a new generation single-chip highly-integrated digital multimedia SOC for devices such as dedicated audio players, photo viewers, PDAs. It includes audio codec, image and video decoding engine, a high performance 2 core (DSP and MCU) structure with embedded RAM and ROM, digital record capabilities and USB interface for downloading and uploading. ATJ2091H also provides an interface to flash memory, LED/LCD/OLED, button and switch inputs, headphones, microphone while ATJ2091H also can interface to FM input and control. ATJ2091H contains a high performance DSP, which can easily be programmed to support many kinds of digital audio standards such as MP3, WMA, etc. As storage devices ATJ2091H can act as a USB mass storage slave device to personal computer system. ATJ2091H has low power consumption to allow long battery life and an efficient flexible on-chip voltage converter that allows many different battery configurations, including 1xAA, 1xAAA, 2xAA, 2xAAA and Li-Lon. The built-in Sigma-Delta DAC includes a headphone driver to directly drive low impedance headphones. The ADC includes inputs for both Microphone and Analog Audio in to support voice recording. ATJ2091H also has radio integration features. ATJ2091H provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital multimedia players.

2. Features

ATJ2091H Features:

- Digital voice recording at ultra low 8Kbps with Actions speech algorithm
- 24 bits DSP core with on-chip debug support unit (DSU)
- 8 bits MCU which instruction set is compatible with Z80
- Support up to 3 (pcs)* 64M ~4G bytes NAND type/SLC/MLC flash
- Support 24MHz OSC with on-chip PLL for DSP
- 2-channel DMA, 1-channel CTC (Counter/Timer Controller) and interrupt controller for MCU
- Energy saving power management (PMU), supporting 1xAA, 1xAAA, 2xAA,2xAAA and Li-Lon
- USB 2.0 high speed, act as mass storage device
- Build in Stereo Sigma-Delta DAC and its modulator digital out

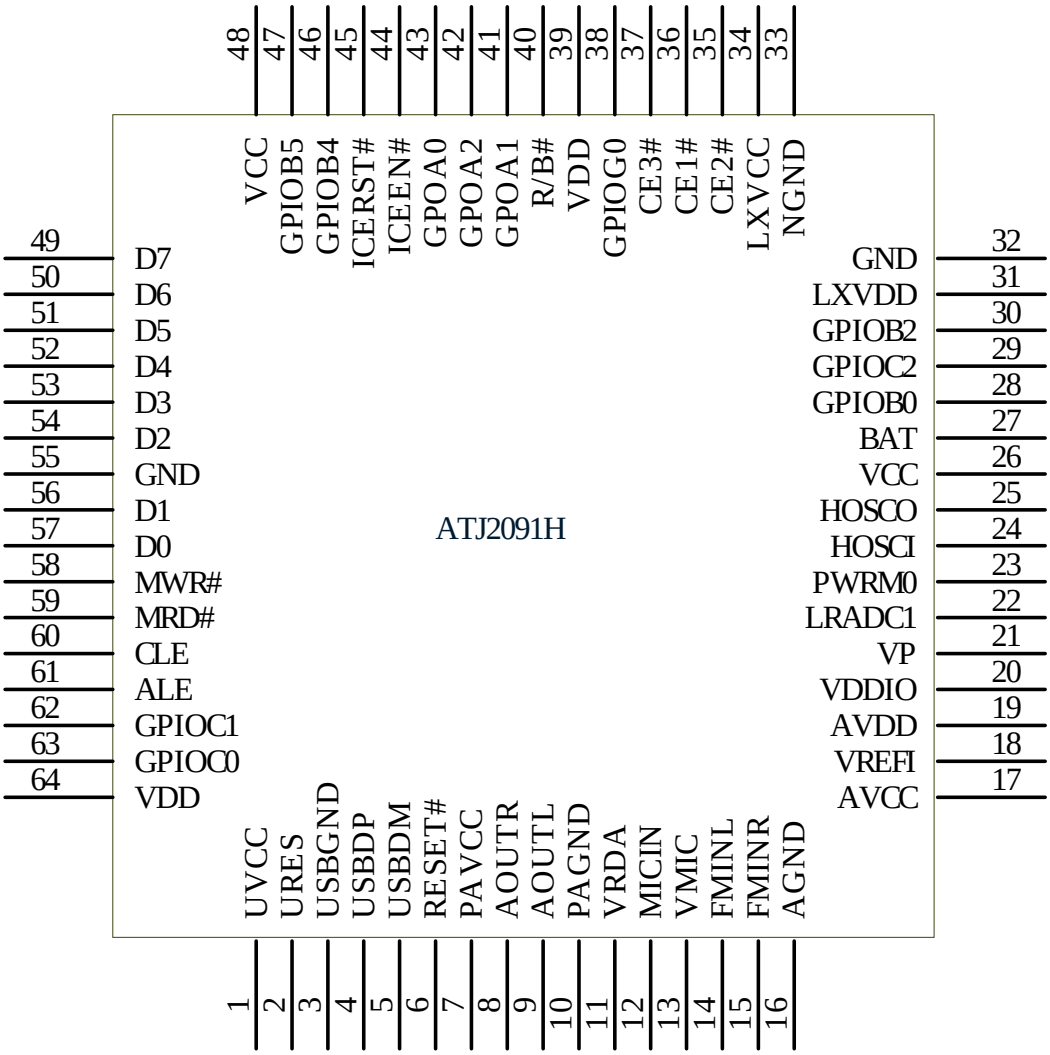
- Support external 80 series LCM driver interface
- Support stereo Sigma-Delta ADC for microphone/ line Input, sample rate at 8/12/16/22/24/32/48KHz
- Support digital audio encoding with sample rate of 8-48KHz
- DSP+PM/DM speed up to 72MIPS
- Headphone driver output 2x11Mw @16ohm
- Package at LQFP-64 (10x10mm)
- FM tuner mixer and controller
- Supports stereo sigma-Delta ADC for FM input, sample rate at 8/12/16/22/24/32/48KHz

3. Pin Description

NOTE:

1: PWR---Power Supply 2: AI---Analog Input
3: AO---Analog Output 4: O---Output
5: I---Input 6: BI---Bi-direction
7: USCU,USCL--- Schmitt Type 8: OD—Open Drain

3.1 Pin Out



3.1.1 Pin Sort by Pin Number

ATJ2091H

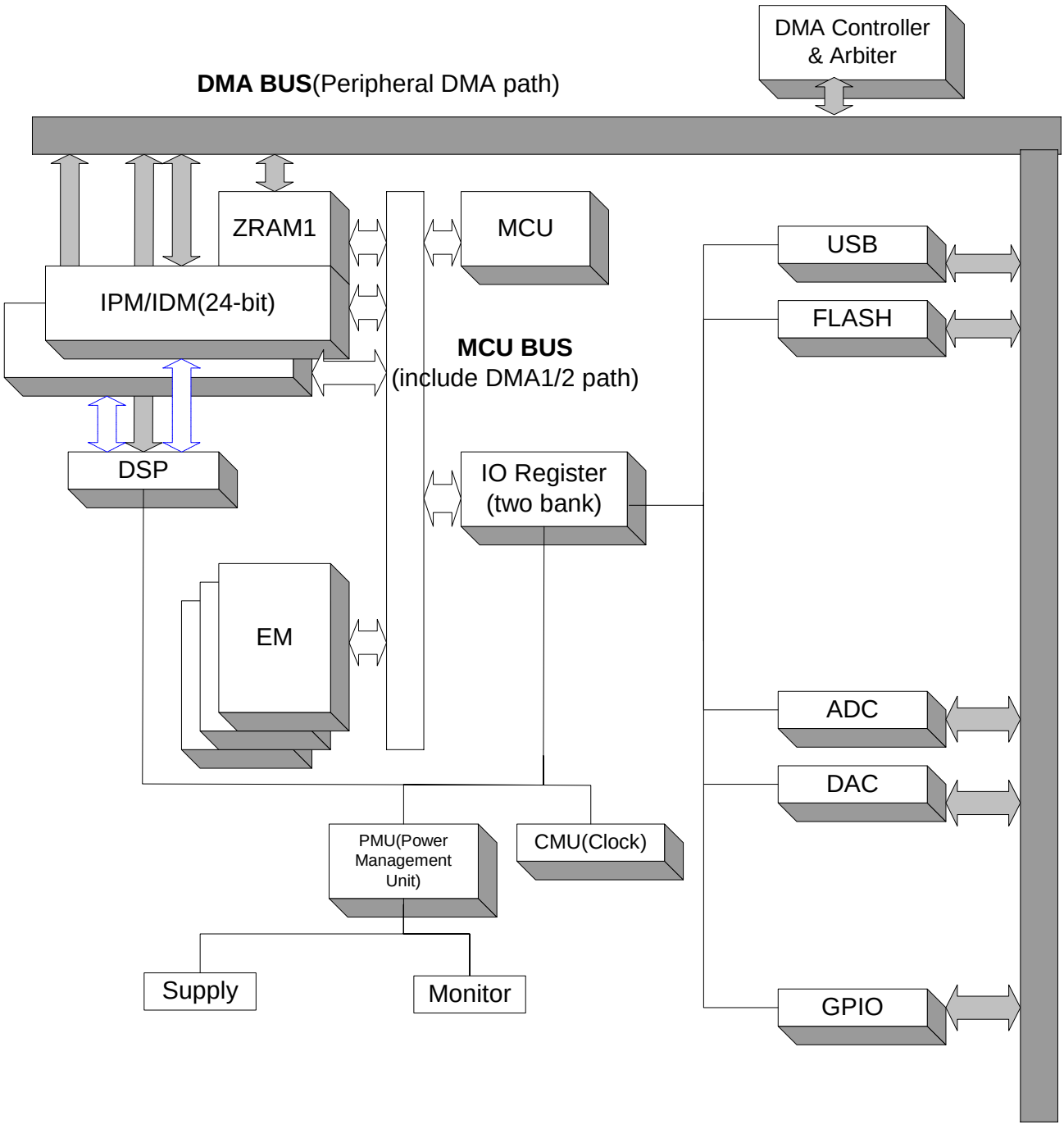
Pin No.	Pin Name	I/O Type	Driver	Reset Default	Short Description
1	UVCC	PWR	/	/	Power supply for USB
2	URES	AO	/	/	USB precision Resistor
3	USBGND	PWR	/	/	USB ground
4	USBDP	A	/	H	USB data minus
5	USBDM	A	/	H	USB data plus
6	RESET-	I	/	H	System reset input (active low)
7	PAVCC	PWR	/	/	Power supply for power amplifier
8	AOUTR	AO	/	/	Int. PA right channel analog output
9	AOUTL	AO	/	/	Int. PA left channel analog output
10	PAGND	PWR	/	/	Power amplifier ground
11	VRDA	AO	/	/	Bypass capacitor connect pin for Int. D/A Reference voltage
12	MICIN	AI	/	/	Microphone pre-amplifier input
13	VMIC	PWR	/	/	Power supply for Microphone
14	FMINL	AI	/	/	Left channel of FM line input
15	FMINR	AI	/	/	Right channel of FM line input
16	AGND	PWR	/	/	Analog ground
17	AVCC	PWR	/	/	power supply of Analog
18	VREFI	AI	/	/	Voltage reference input
19	AVDD	PWR	/	/	Analog Core power pin
20	VDDIO	PWR	/	/	Core power input/output
21	VP	PWR	/	/	Power pin
22	LRADC1	AI	/	/	Low resolution A/D input 1
23	PWRM 0	AI	/	/	POWER mode select 0
24	HOSCI	AI	/	/	High frequency crystal OSC input

25	HOSCO	AO	/	/	High frequency crystal OSC output
26	VCC	PWR	/	/	PAD power pin
27	BAT	I	/	/	Battery monitor pin.
28	GPIO_B0	BI	2mA	Z	Bit0 of General purpose I/O port B
	KEYI0	I		H	Bit0 of key scan circuit input
29	GPIO_C2	BI	4mA	/	Bit2 of General purpose I/O port C
30	GPIO_B2	BI	10mA	Z	Bit2 of General purpose I/O port B
	KEYI2	I		H	Bit2 of key scan circuit input
31	LXVDD	PWR	/	/	Connect to VDD inductance
32	GND	PWR	/	/	Ground
33	NGND	PWR	/	/	NMOS Ground
34	LXVCC	PWR	/	/	Connect to VCC inductance
35	CE2-	O	/	H	Ext. memory chip enable 2
36	CE1-	O	/	H	Ext. memory chip enable 1
37	CE3-	O	4mA	H	Ext. memory chip enable 3
	GPO_A3	O		/	Bit3 of General purpose port A
38	GPIO_G0	BI	2mA	Z	Bit0 of General purpose I/O port G
39	VDD	PWR	/	/	Digital Core power
40	RB-	I	/	OD	Nand Type flash Ready/Busy status input.
41	GPO_A1	O	4mA	L	Bit1 of General purpose Output port A
	ICECK	I		/	Clock input of DSU
42	GPO_A2	O	4mA	L	Bit2 of General purpose Output port A
	ICEDO	O		/	Data output of DSU
43	GPO_A0	O	4mA	0	Bit0 of General purpose Output port A
	ICED1	I		/	Data input of DSU
44	ICEEN-	I	/	/	DSU enable (active low)
45	ICERST-	I	/	/	DSU reset (active low)
46	GPIO_B4	BI	10mA	Z	Bit4 of General purpose I/O port B
	KEYO0	O		/	Bit0 of key scan circuit output
47	GPIO_B5	BI	10mA	Z	Bit5 of General purpose I/O port B

	KEYO1	O		/	Bit1 of key scan circuit output
48	VCC	PWR	/	/	Digital power pad
49	D7	BI	/	L	Bit7 of ext. memory data bus
50	D6	BI	/	L	Bit6 of ext. memory data bus
51	D5	BI	/	L	Bit5 of ext. memory data bus
52	D4	BI	/	L	Bit4 of ext. memory data bus
53	D3	BI	/	L	Bit3 of ext. memory data bus
54	D2	BI	/	L	Bit2 of ext. memory data bus
55	GND	/	/	L	GND
56	D1	BI	/	L	Bit1 of ext. memory data bus
57	D0	BI	/	L	Bit0 of ext. memory data bus
58	MWR-	O	/	H	Ext. memory write strobe
59	MRD-	O	/	H	Ext. memory read strobe
60	CLE	O	/	L	Command latch enable for NAND flash
61	ALE	O	/	L	Address latch enable for NAND flash
62	GPIO_C1	BI	2mA	OD	Bit1 of General purpose I/O port C
	_SDA	O		/	Serial data (Open drain)
	SIRQ-	I		/	Ext. interrupt request input
63	GPIO_C0	BI	2mA	OD	Bit0 of General purpose I/O port C
64	VDD	PWR	/	/	Digital Core power

Function Description

4.1 Functional Block Diagram



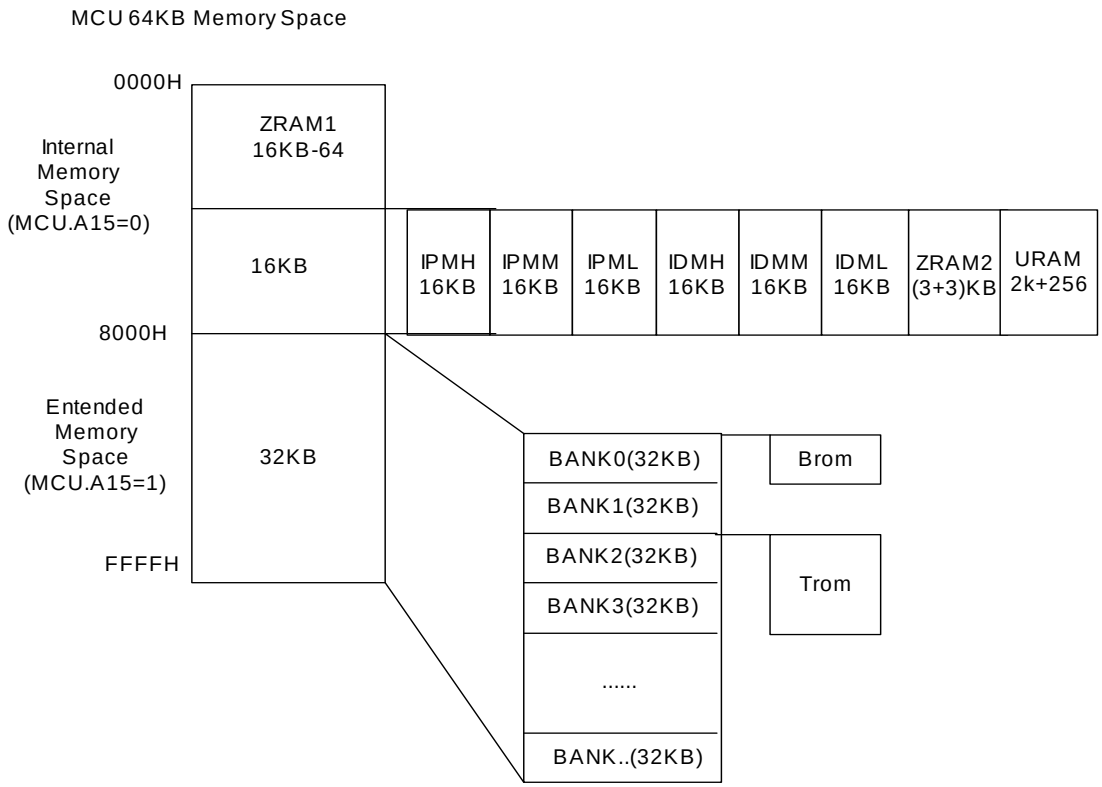
4.2 MCU Core

4.2.1 MCU Memory

ATJ2091H includes120K+192=(16+6+2+16*3+16*3)K+256-64 bytes of on-chip SRAM and 50K=(12+21+17)k bytes on-chip ROM. See the following flag for on chip memory mapping.

- (16K-64) byte ZRAM1(IA15=0,IA14=0) : 0000H-3FBFH
- 6Kbyte ZRAM2 (IA15=0, IA14=1, IOReg05.[2:0]=111) : 4000H-57FFH
- ZRAM2 is make up of B1 and B2, each one is 3k*8 byte SRAM. B1, B2 and ZRAM1(B0) can be operated severally.

4.2.2 MCU 64kb Memory Space



4.3 DSP Core

24-bit Harvard architecture DSP with DSU built in. It works with a memory word length of 24 bits. ATJ2091H has 16KB*24bit program memory (PM) and (16KB)*24bit data memory (DM). Memory-Mapped register includes DAC interface.

4.4 DMA Controller

ATJ2091H supports 4 kinds of DMA channels. DMA1/2 support Data exchange in Memory or IO; DMA5 is for flash controller, DMA6 is USB DMA.

4.5 General Purpose IO Ports

ATJ2091H has GPOA, GPIOB, GPIOC, GPIOD, GPIOE, GPIOF, GPIOG and GPIOK. They have different functions in different modes.

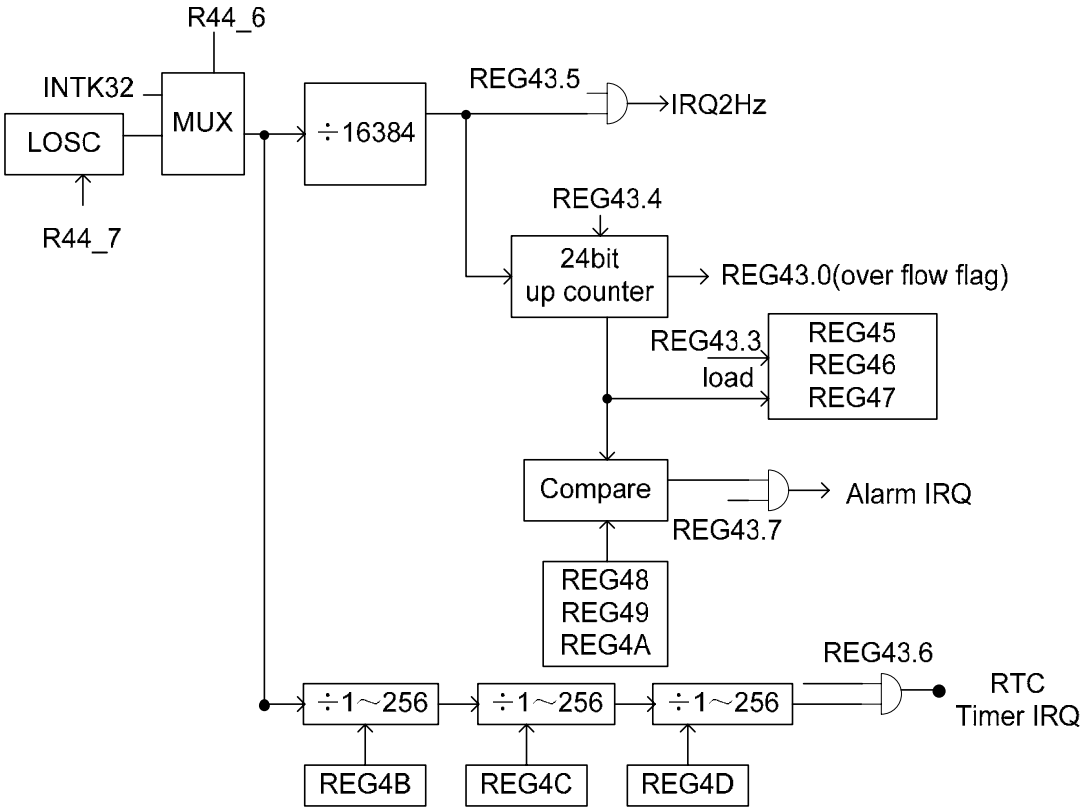
<table>
<tr><th>Function / GPIO</th><th></th><th>F1</th><th>F2</th><th>F3</th><th>F4</th><th>F5</th><th>F6</th><th>F7</th><th>F8</th></tr>
<tr><td rowspan="3">GPOA</td><td>0</td><td colspan="8" rowspan="3">When ICE is used, GPO_A [2~0] Pins are ICEDO, ICECK and ICEDI; Otherwise GPO_A [2~0] is used for output function.</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td rowspan="8">GPIOB</td><td>0</td><td colspan="8" rowspan="8">At function 1（F1）：When choosing keyboard function, GPIOB [3~0] Pins are KEYI [3~0], and GPIOB [7~4] are KEYO [3~0]; when not choosing keyboard function, as GPIOB [7~0]; when keyboard function enables, while some KEYI[3...0] is used as GPIOB, the relative keyin should be masked.GPIOB2/B4/B5 have special large drive capability up to 10mA,it can be used to drive diode.
At Function2－8（F2-F8）：When choosing keyboard function, GPIOB [3~0] Pins are KEYI [3~0], and GPIOB [7~4] are KEYO [3~0]; when not choosing keyboard function, as GPIOB [7~0]; when keyboard function enables, while some KEYI [3...0] is used as GPIOB, the relative keyin should be masked. Especially, when SPI function is enabled, GPIOB2 is used as SPI_SCK and GPIOB5 is used as SPI_MOSI.</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td></tr>
<tr><td>7</td></tr>
<tr><td rowspan="4">GPIOC</td><td>0</td><td>GPIOC0</td><td colspan="7">(F2-F8): When I^{2}C function enables, it is used as _SCL. When as IO, it is GPIO_C0, and then I^{2}C can not be enabled simultaneously.</td></tr>
<tr><td>1</td><td>GPIOC1</td><td colspan="7">(F2-F8): When I^{2}C function enables, it is used as _SDA. When external interrupt enables, it is SIRQ-; and when as IO, it is GPIO_C; multiple functions can not be enabled simultaneously.</td></tr>
<tr><td>2</td><td>GPIOC2/</td><td colspan="7">(F2-F8): GPIO_C2</td></tr>
<tr><td>3</td><td colspan="2">(F1-F3): GPIO_C3 only</td><td colspan="6">(F4-F8) : CE0_</td></tr>
</table>

4.6 RTC/CTC/Watch Dog Timer

4.6.1 RTC

RTC is a 24-bits counter with the following function, the clock source is LOSC (95H only) or INTK32

- Time
- Alarm
- Timer



4.6.2 CTC

CTC is a counter whose clock source is different with RTC. The clock source is HOSC.

4.6.3 Watchdog

Watchdog can be set from 176-milisecond to 180-second with different step.

4.7 Power Management Unit (PMU)

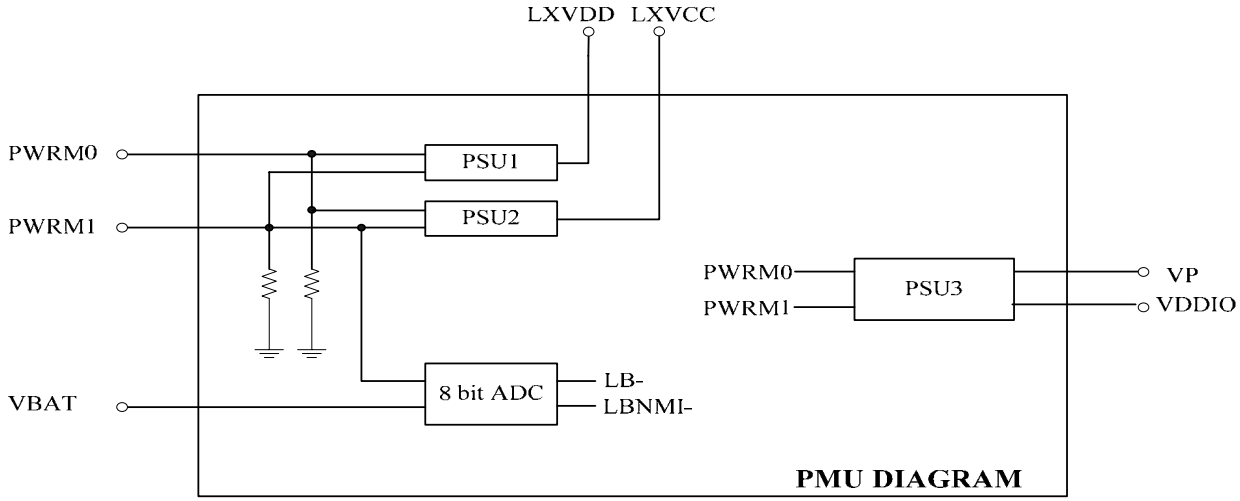
4.7.1 Power Supply Modes

ATJ2091H can support 1xAA/AAA, 2xAA/AAA, Li Battery or USB power supply mode by configuring

two pins PWRM0 and PWRM1.

PWRM1	PWRM0	PSU1(VDD)	PSU2(VCC)	PSU3(VDD)	Mode Descriptions
0	0	On	On	Off	1x AA/AAA with more efficiency
0	1	Off	On	On	1x AA/AAA with less external components
1	0	Off	On	On	Two batteries
1	1	Off	Off	On	USB power or Li battery

The pin “PWRMode1” and “PWRMode0” have been pull down by on-chip resistor.

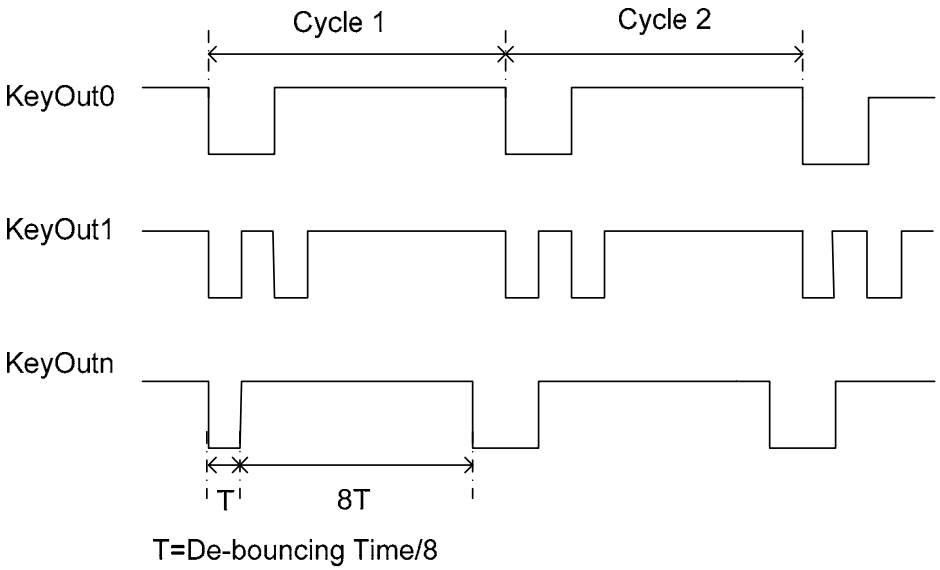


4.8 LCD Interface

ATJ2091H supports high-speed 8-bit parallel bi-directional LCM with 8080-series interface. LCM with 8080-series interface:

- Use GPIO to select data register or command register in LCM.
- CE3- is used as chip select. Pin CS2 of LCM is pulled high to VCC.
- MWR- is write enable signal. ATJ2091H latches D [7:0] at the rising edge.
- MRD- is read enable signal and LCM drives D [7:0] when MRD- is low.

4.9 Key Scan Interface



Key Scan Timing

When key scan circuit is enabled, ATJ2091H will scan the keyboard periodically. It drives pin KEYOUTn [n=2…7] scan pulse in turn. When any key is pressed, the corresponding Keyout N will send out the scan pulse. When a key is pressed, pin Keyin N connecting the key will be found low level.

There are 12 internal 8-bit registers for key value latch per scan. But only another one register (Key Scan Data Register) for MCU may access key value. Those 12 internal registers are mapped into this register, and an internal pointer is used to point to the current register to return scan data when read. Any IO write to this register will clear the internal register, and the pointer will increase by 1 and point to the next register after read is performed.

4.10 External Memory Interface

4.10.1 NAND Flash Interface

ATJ2091H can support NAND type flash from 64M to 4G bytes.

4.11 USB 2.0 SIE

4.11.1General Description

The Actions USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. In high-speed mode this device is capable of transmitting or receiving data up to 480Mbps.This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

4.11.2 Features

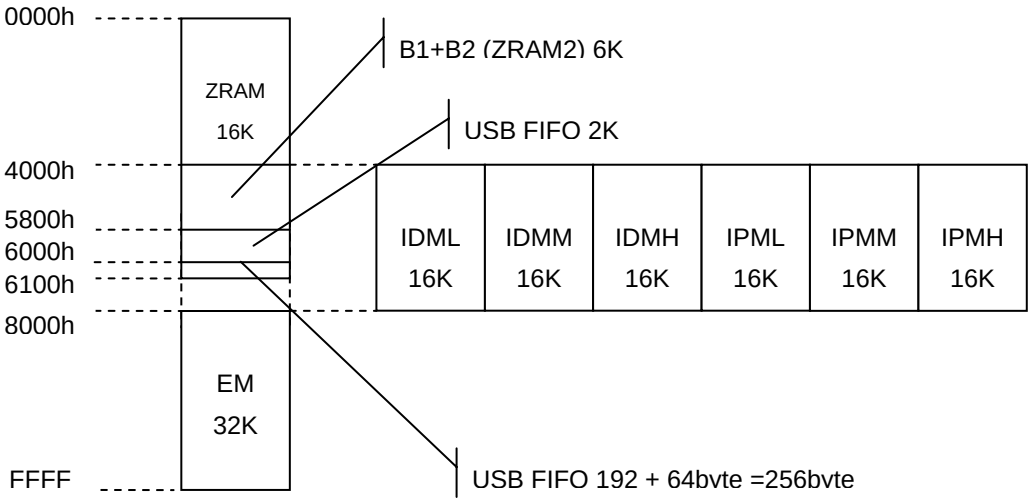
- Fully compliant with USB specification 2.0
- Supports USB high speed (480Mb/s) and full speed (12Mb/s)
- Supports control, bulk, Isochronous and Interrupt transfers
- Embedded USB high-speed transceiver which complies with Inter UTMI
- Supports DMA interface (16-bit)
- 2K bytes configurable FIFO for endpoints and provides double buffer to increase throughput.
- Supports USB remote wake-up feature
- Software controlled connection to USB bus for re-enumeration

4.11.3 Flash Interface

The Flash Interface circuit is a programmable high performance HW State Machine which supports a lot features in the following text.

- Command and address control state machine
- Reading and writing timing generator
- ECC accelerator (Reed-Solomon & Hamming)
- Sense R/B# status
- Comply with “SmartMedia Software Algorithm Guidelines”
- Bad block detection and replacement
- MLC flash supported

4.11.4 USB Using Memory



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	2.0	±10%	V
	VCC	3.3	±10%	V
Input voltage	V_{IH}	2.4	±10%	V
	V_{IL}	1.0	±10%	V
Storage temperature	T_{stg}		-65~150	℃

Note:

1. T_O = 25℃（Operating Temperature）
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

5.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

5.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.6VCC		VCC+0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			±10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			±5	uA
GPIO Drive	I_{drive1}	GPOA0,GPOA1,GPOA2		4		mA
	I_{drive2}	GPIO_B2, GPIO_B4, GPIO_B5		10		mA
	I_{drive3}	Other GPIO		2		mA
Supply Current （One battery mode）	I_{VDD}	In Full speed mode (MCU run 24MHz in internal SRAM, DSP run 36MIPS)		21	25	mA
		In Standby mode		50	70	uA
	I_{VCC}	In Full speed mode (MCU run 24MHz in internal SRAM, DSP run 36MIPS)		1.28	1.5	mA
		In Standby mode		18	40	uA

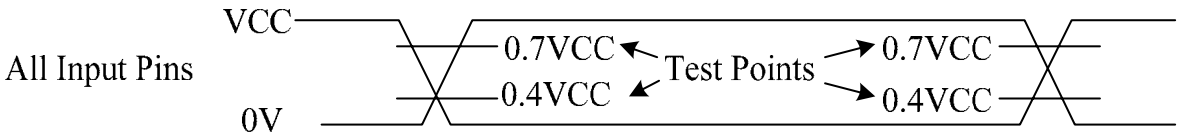
NOTES:

1. T_o = -10 to +70°C, VDD = 2.0 V, VCC = 3.3 V
2. I_{VDD} is a total power supply current for the 2.5 V power supply. I_{VDD} is applied to the LOGIC and PLL and OSC block.
3. I_{VCC} is a total power supply current for the 3.3 V power supply. I_{VCC} is applied to the USB, IO, TP, and AD block.

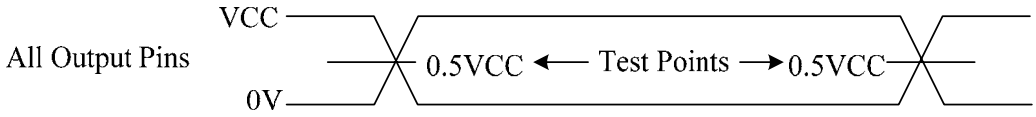
5.4 AC Characteristics

T_o = -10 to +70℃

5.4.1 AC Test Input Waveform

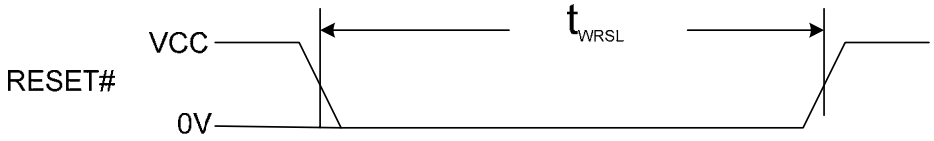


5.4.2 AC Test Output Measuring Points



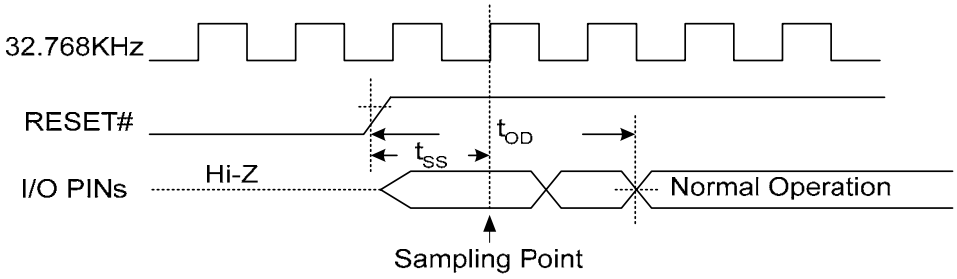
5.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	160		us



5.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}			61.04	us
Output delay time (from RESET#)	t_{OD}		61.04		us

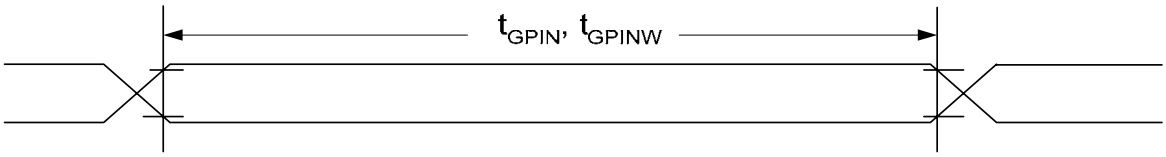


5.4.5 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$11/f_{mcuclk}$		s
GPIO input rise time	t_{GPRISE}			200	ns
GPIO input fall time	t_{GPFALL}			200	ns
Output level width	t_{GPOUT}		$11/ f_{mcuclk}$		s

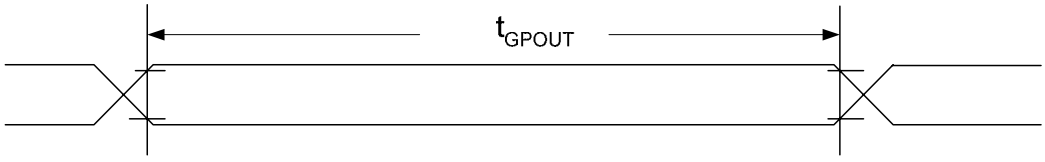
Note: 1. f_{MCUCLK} is the frequency upon which MCU is running.

Input Level Width



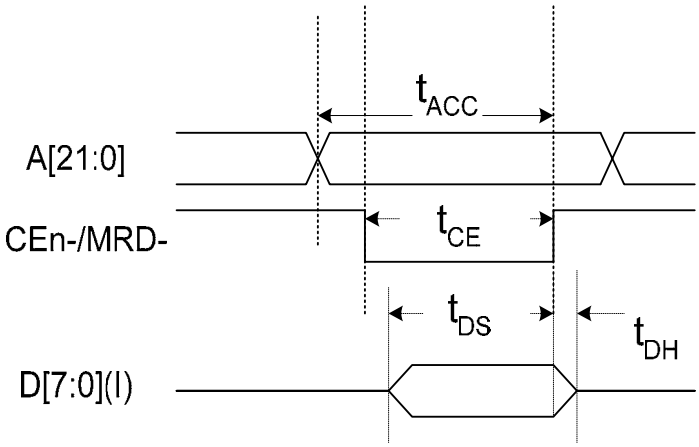
Input Rise/Fall Time

Output Level Width

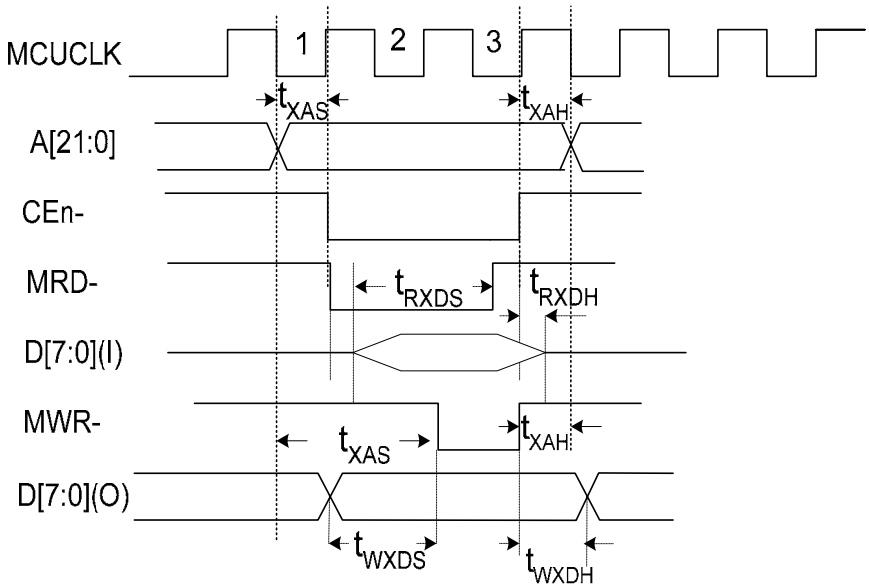


5.4.6 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}	HOSC=24MHz	102		ns
Data access time (from CEx#)[Note]	t_{CE}	HOSC=24MHz	82		ns
Data input setup time	t_{DS}	HOSC=24MHz	0		ns
Data input hold time	t_{DH}	HOSC=24MHz	0		ns



5.4.7 External System Bus Parameter



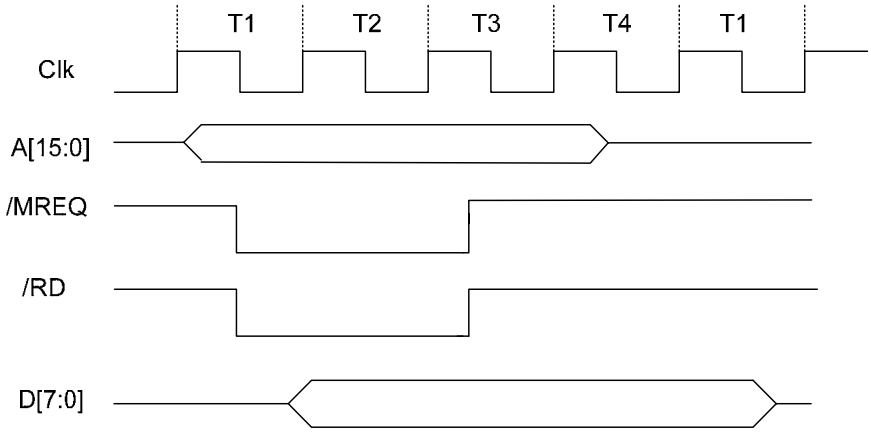
Parameter	Symbol	Condition	Min.	Max.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	25		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

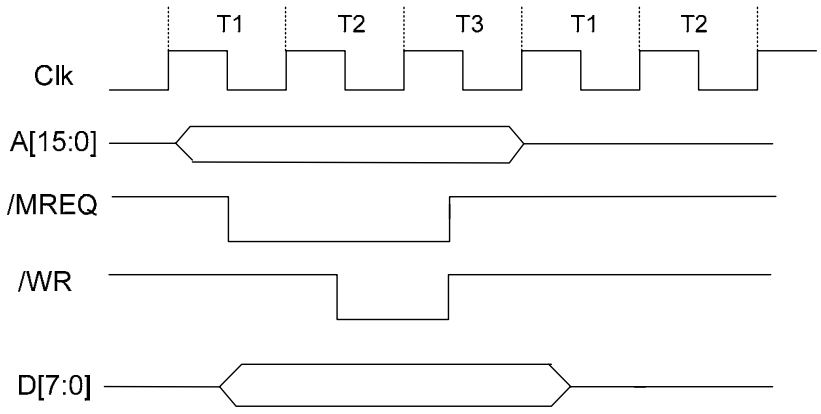
5.4.8 Bus Operation

Memory Read Timing



Memory Read Timing

Memory Write Timing



Memory Write Timing

5.4.9 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 2.0 V, VCC = 3.3V, Sample Rate=32KHz)

Characteristics	Min.	Typ.	Max.	Unit
Dynamic range		78		dB
Total Harmonic Distortion + Noise		73		dB
Frequency Response (20-13KHz)			±5%	dB
Full Scale Input Voltage(Gain=0dB)		2		mVpp

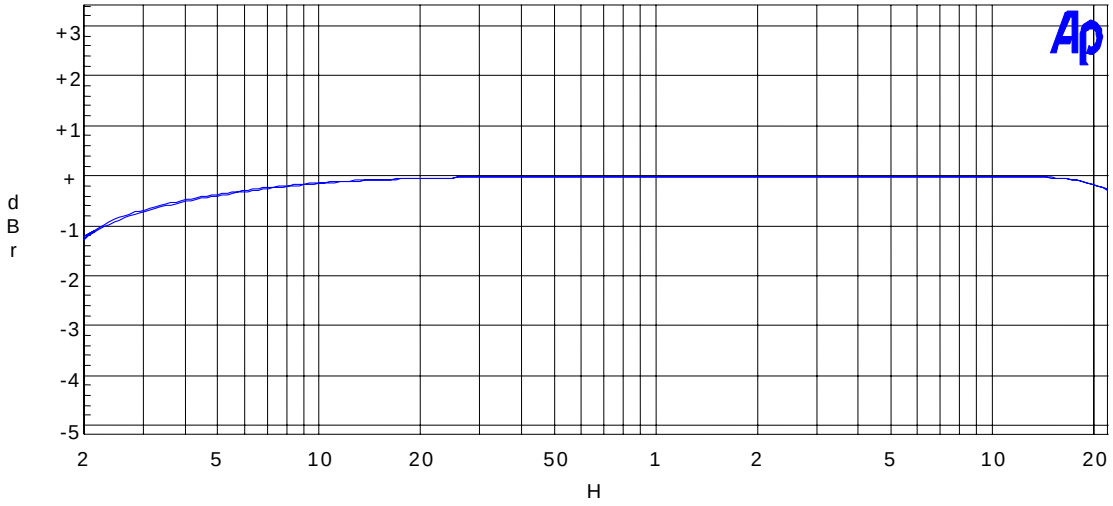
5.4.10 Headphone Driver Characteristics Table

(T_o =-10 - +70℃, VDD = 2.0 V, VCC = 3.3 V, Sample Rate=32KHz, Volume Level=0x1F)

Characteristics	Min.	Typ.	Max.	Unit
Dynamic Range –60 dBFS Input		86		dB
Total Harmonic Distortion + Noise		80		dB
Frequency Response 20-20KHz			±1	dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.2		Vpp
Inter channel Gain Mismatch(1KHz)		11		dB

Frequency Response Diagram of Headphone Driver

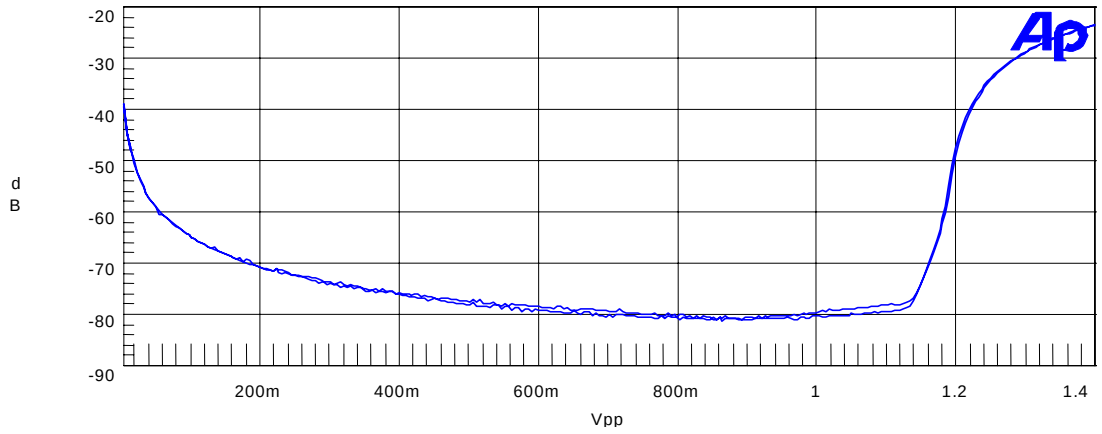
Audio ATJ2091 PA Frequency Response @1Vpp



Swe	Trac	Col	Line	Thic	Dat	Axi	Comm
1	1	Blu	Soli	1	Anlr.A	Lef	Left
1	2	Blu	Soli	1	Anlr.A	Lef	Right

THD + N Amplitude Diagram of Headphone Driver

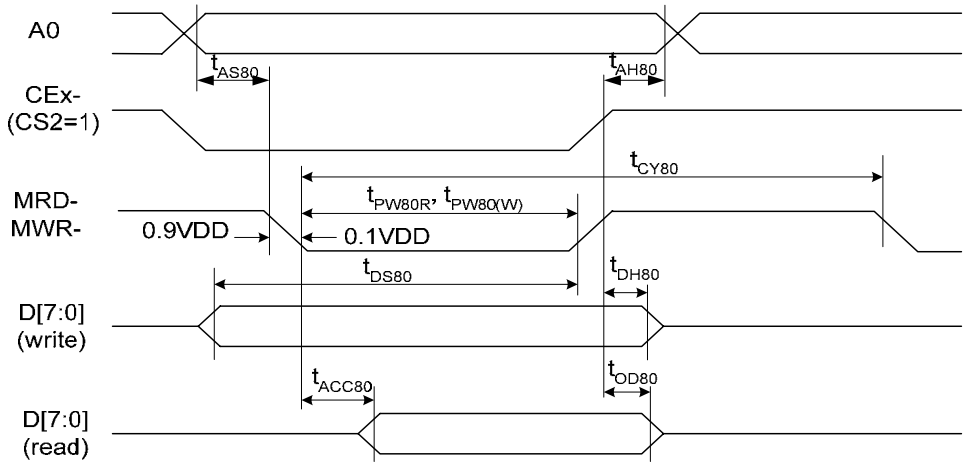
Audio Precision ATJ2091 PA THD+N vs Amplitude
@1KHZ 16ohm*220uF



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	Left Channel
1	2	Blue	Solid	1	Anlr.THD+N Ratio	Left	Right Channel

5.4.11 LCM Driver Parameter

LCM Interface Timing



Parameter	Symbol	Condition	Type	Unit
Data access time(write)	$t_{PW80(W)}$	HOSC=24MHZ	29	ns
Data access time (Read)	$t_{PW80(R)}$	HOSC=24MHZ	67	ns
Write cycle time	$t_{CY80(W)}$	HOSC=24MHZ	407	ns
Read cycle time	$t_{CY80(R)}$	HOSC=24MHZ	284	ns
Data setup time	t_{DS80}	HOSC=24MHZ	79	ns
Data hold time	t_{DH80}	HOSC=24MHZ	8	ns
Address setup time	t_{AS80}	HOSC=24MHZ	11	ns
Address hold time	t_{AH80}	HOSC=24MHZ	11	ns
Read access time	t_{ACC80}	HOSC=24MHZ	13	ns
Data input hold time	t_{OD80}	HOSC=24MHZ	8	ns

6. Ordering Information

6.1 Soldering Conditions

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 235℃(Lead) or 260℃(Lead Free)
	Reflow time: 30 seconds or less (210℃or more)----(Lead) or 60 seconds or less (217℃or more)---- (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%,Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

Maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

6.2 Precaution Against ESD For Semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work

bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

6.3 Handling of Unused Input Pins For CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

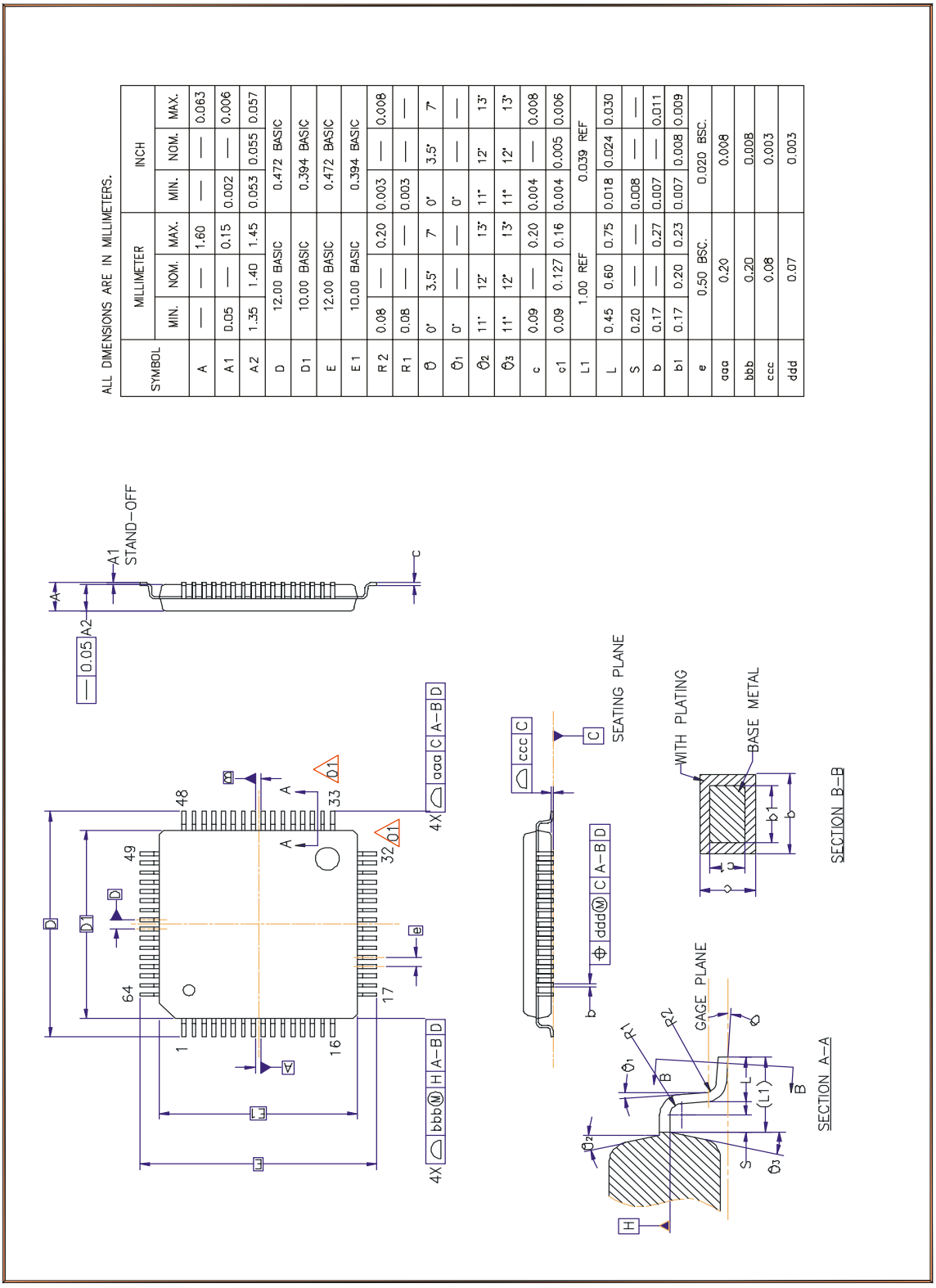
6.4 Status Before Initialization of MOS Devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on .

7. ATJ 2091H Package Drawing

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D		12.00 BASIC			0.472 BASIC	
D1		10.00 BASIC			0.394 BASIC	
E		12.00 BASIC			0.472 BASIC	
E1		10.00 BASIC			0.394 BASIC	
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1		1.00 REF			0.039 REF	
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e		0.50 BSC.			0.020 BSC.	
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.07			0.003	



Actions Semiconductor Co., Ltd.

Address: 15-1, NO.1, HIT Road, Tangjia, Zhuhai, Guangdong, China

Tel: +86-756-3392353

Fax: +86-756-3392251

Post code: 519085

http:// www.actions-semi.com

Business Email: mp-sales@actions-semi.com

Technical Service Email: mp-cs@actions-semi.com