Low Power Analog Front End

■FEATURES

- ●Supply Voltage +2.4 to +3.6V
- ●Low Current Consumption 4µA (OPA,OPB), 150µA (ADC)
- ●Low Noise Amplifier 1.3µVpp typ. (0.1 to 10Hz)
- ●Low Offset Voltage Amplifier 300µV max.
- ●RF immunity Amplifier
- ●Programmable Cell Bias Voltage
  - OPA: 0.3V to 1.7V (7 steps)
  - OPB: 0.25V to 1.75V (50mV step)
- ●Programmable Gain Pre-Amplifier 1V/V to 8V/V
- ●High resolution Programmable Gain ADC
  - 1V/V to 8V/V, 16-Bit (NFB), 32sps to 2k sps
- ●System Calibration for offset & gain drift
- ●Control external EEPROM as a Master device
- ●Ambient Operating Temperature -40°C to +85°C
- ●Interface I^2C (3-Bit selectable slave address)
- ●Package EQFN-24-LE (4mm x 4mm)

■GENERAL DESCRIPTION

NJU9101 is a Low Power Analog Front End IC for use in micro-power sensing applications, especially electrochemical sensors. It provides a complete signal processing solution between sensor and micro-processor as smart-sensor module.

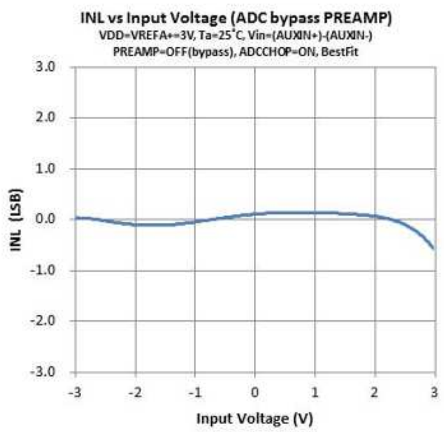
NJU9101 has 2 channel low power operational amplifiers. These amplifiers provide potentiostat and trans-impedance-amplifiers to constitute gas sensor systems. The NJU9101 has calibration circuit by using output data of built-in high precision ADC. It is suitable for temperature variation of sensor.

NJU9101 operates over voltage range of 2.4V to 3.6V. Total average current consumption can be less than 5µA.

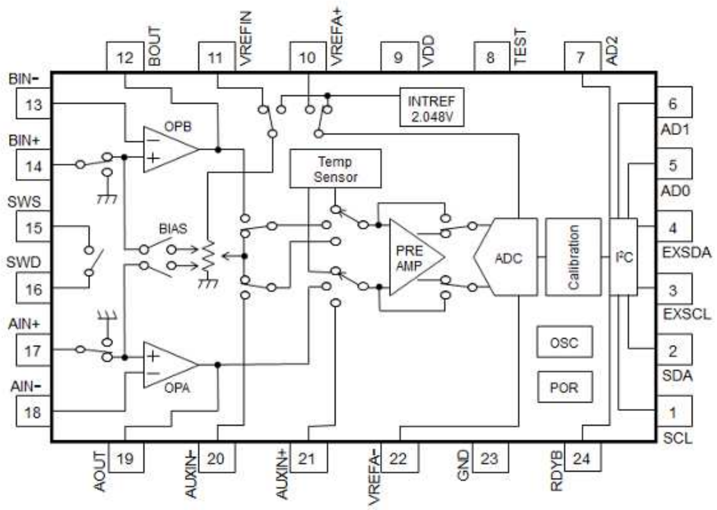
■APPLICATION

- ●Gas Monitor
- ●Blood Glucose Meter
- ●Current Sensing Systems
- ●Low Power Systems
- ●Photodiode Sensing Systems
- ●Portable equipment

■INL vs Input Voltage (ADC)

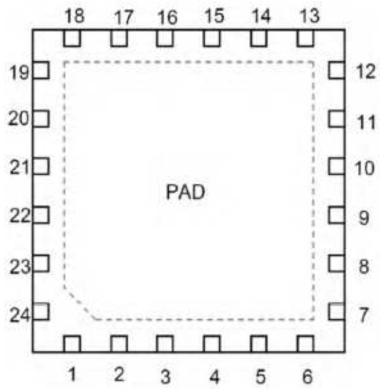


■EQUIVALENT CIRCUIT・BLOCK DIAGRAM



■PIN CONFIGURATION

EQFN-24-LE



<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th colspan="2">DESCRIPTION</th><th>Pin Type</th></tr>
<tr><td>1</td><td>SCL</td><td colspan="2">I^{2}C serial clock input</td><td>Digital Input</td></tr>
<tr><td>2</td><td>SDA</td><td colspan="2">I^{2}C serial data input / output
(which requires an pull-up resistor)</td><td>Digital Input / Output</td></tr>
<tr><td>3</td><td>EXSCL</td><td colspan="2">I^{2}C serial clock output for external EEPROM
(which requires an pull-up register)</td><td>Digital Output</td></tr>
<tr><td>4</td><td>EXSDA</td><td colspan="2">I^{2}C serial data input / output for external EEPROM
(which requires an pull-up resister)</td><td>Digital Input / Output</td></tr>
<tr><td>5</td><td>AD0</td><td>Chip address selection input 0</td><td rowspan="3">Select 7 chip address from “000” to “110”. Do not select address “111”, which address is for production test purpose</td><td>Digital Input</td></tr>
<tr><td>6</td><td>AD1</td><td>Chip address selection input 1</td><td>Digital Input</td></tr>
<tr><td>7</td><td>AD2</td><td>Chip address selection input 2</td><td>Digital Input</td></tr>
<tr><td>8</td><td>TEST</td><td colspan="2">TEST terminal (This terminal is used for production test. Connect to VDD)</td><td>Analog Input</td></tr>
<tr><td>9</td><td>VDD</td><td colspan="2">Voltage Supply</td><td>Power Supply</td></tr>
<tr><td>10</td><td>VREFA+</td><td colspan="2">Positive voltage reference input for ADC</td><td>Analog Input</td></tr>
<tr><td>11</td><td>VREFIN</td><td colspan="2">Voltage reference input for Bias Registor</td><td>Analog Input</td></tr>
<tr><td>12</td><td>BOUT</td><td colspan="2">Voltage output for Bch. OpAmp</td><td>Analog Output</td></tr>
<tr><td>13</td><td>BIN-</td><td colspan="2">Negative voltage input for Bch. OpAmp</td><td>Analog Input</td></tr>
<tr><td>14</td><td>BIN+</td><td colspan="2">Positive voltage input for Bch. OpAmp</td><td>Analog Input</td></tr>
<tr><td>15</td><td>SWS</td><td colspan="2">Switch Source Input</td><td>Swtich</td></tr>
<tr><td>16</td><td>SWD</td><td colspan="2">Switch Drain Input</td><td>Swtich</td></tr>
<tr><td>17</td><td>AIN+</td><td colspan="2">Positive voltage input for Ach. OpAmp</td><td>Analog Input</td></tr>
<tr><td>18</td><td>AIN-</td><td colspan="2">Negative voltage input for Ach. OpAmp</td><td>Analog Input</td></tr>
<tr><td>19</td><td>AOUT</td><td colspan="2">Voltage output for Ach. OpAmp</td><td>Analog Output</td></tr>
<tr><td>20</td><td>AUXIN-</td><td colspan="2">Auxiliary positive input</td><td>Analog Input</td></tr>
<tr><td>21</td><td>AUXIN+</td><td colspan="2">Auxiliary negative input</td><td>Analog Input</td></tr>
<tr><td>22</td><td>VREFA-</td><td colspan="2">Negative voltage reference input for ADC
(connect to GND, is recommended)</td><td>Analog Input</td></tr>
<tr><td>23</td><td>GND</td><td colspan="2">GND</td><td>GND</td></tr>
<tr><td>24</td><td>RDYB</td><td colspan="2">RDYB output / GPIO</td><td>Digital Input / Output</td></tr>
<tr><td>PAD</td><td>EXPPAD</td><td colspan="2">Exposed PAD on backside (connect to GND)</td><td>GND</td></tr>
</table>

■MARK INFORMATION

NJU9101 MLE (TE1)

Part Number / Package / Taping Form

■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJU9101MLE	EQFN-24-LE	O	O	Sn-2Bi	9101	31	1,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	5	V
Analog Input Voltage(1)	V_{IA}	-0.3 to V_{DD}+0.3 not exceeding 5	V
Digital Input Voltage	V_{ID}	-0.3 to 6	V
Switch Input Voltage(1)	V_{IS}	-0.3 to V_{DD}+0.3 not exceeding 5	V
On State Switch Current	I_{SO}	-40 to +40(3)	mA
Power Dissipation(T_a=25°C)(2)	P_D	830(4) / 2100(5) (2-layer / 4-layer)	mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(1): The input pins have clamp diodes to the power supply pins. Limit the input current to 10mA or less whenever input signals exceed the power supply rail by 0.3V.

(2): Power dissipation is the power that can be consumed by the IC at T_a=25°C, and is the typical measured value based on JEDEC condition. When using the IC over T_a=25°C subtract the value [mW/°C] = P_D / T_{st} max.- 25) per temperature.

(3): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(4): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	+2.4 to +3.6	V
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

■ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OPA, OPB						
Input Offset Voltage	V_{IO}	$V_{ICM} = V_{DD}/2$, $R_s = 50\Omega$	-	-	±300	µV
Input Offset Voltage Drift	$\Delta V_{IO} / \Delta T$		-	±1	-	µV/°C
Input Bias Current	I_B		-	10	-	pA
Open Loop Gain	A_V		-	100	-	dB
Common Mode Rejection Ratio	CMR	V_{ICM} = GND to 2V	65	80	-	dB
Common Mode Input Voltage Range	V_{ICM}	CMR ≥ 65dB	GND	-	2	V
Maximum Output Voltage	V_{OH}	$I_{SOUECE} = 1mA$	2.8	2.85	-	V
	V_{OL}	$I_{SINK} = 1mA$	-	0.15	0.2	V
Gain Band Width	GBW		-	30	-	kHz
Slew Rate	SR		-	0.01	-	V/µs
Equivalent Input Noise Voltage	e_n	f = 100Hz, $R_S = 50\Omega$	-	50	-	nV/√Hz
		f = 0.1Hz to 10Hz	-	1.3	-	μV_{pp}

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$, ADC reference Voltage = External

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OPA, OPB with BIASRES (Potentiostat)						
OPA referred to OPB Input Offset Voltage 1	$V_{IO1A\text{-}B}$	OPA BIAS = 1V OPB BIAS = 1V	-	-	±0.6	mV
OPA referred to OPB Input Offset Drift 1	$\Delta V_{IO1A\text{-}B} / \Delta T$	OPA BIAS = 1V OPB BIAS = 1V	-	±2	-	µV/°C
OPA referred to OPB Input Offset Voltage 2	$V_{IO2A\text{-}B}$	OPA BIAS = 1V OPB BIAS = 0.7V	295	300	305	mV
OPA referred to OPB Input Offset Drift 2	$\Delta V_{IO2A\text{-}B} / \Delta T$	OPA BIAS = 1V OPB BIAS = 0.7V	-	±5	-	µV/°C
OPA referred to OPB Input Offset Voltage 3	$V_{IO3A\text{-}B}$	OPA BIAS = 1V OPB BIAS = 1.6V	-605	-600	-595	mV
OPA referred to OPB Input Offset Drift 3	$\Delta V_{IO3A\text{-}B} / \Delta T$	OPA BIAS = 1V OPB BIAS = 1.6V	-	±8	-	µV/°C

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Switch (ANASW)						
On State Resistance	R_{ON}	Analog Switch = ON $I_{DS} = -10mA$		10	30	Ω
Off Leakage Current	I_{LOFFD}	Analog Switch = OFF V_{SWS}=2V/1V, V_{SWD}=1V/2V	-	±1	-	nA

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$, Temperature Input Mode

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature Sensor						
Temperature Accuracy (Error) 1	T_{ACC1}	$T_a = 25°C$	-	±1	±5	°C
Temperature Accuracy (Error) 2	T_{ACC2}	$T_a = -40°C$ to $+85°C$	-	±3	-	°C
Temperature Resolution	T_{RES}		-	0.25	-	°C

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = 3V$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Internal Reference						
Internal Reference Voltage	V_{IREF}	±1%	2.028	2.048	2.068	V
Internal Reference Drift	$\Delta V_{IREF} / \Delta T$	$T_a = -40°C$ to $+85°C$	-	30	-	ppm/°C

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$, Auxiliary Differential Input Mode

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PREAMP						
PREAMP Gain Error	G_{ACCP}	PREAMP Gain = 1V/1V to 8V/V	-	±0.1	-	%
PREAMP Common Mode Rejection	CMR_{PRE}	PREAMP Gain = 1V/V AUXIN+ = AUXIN- = GND+0.05 to V_{DD}-1	70	90	-	dB
PREAMP Common Mode Input Voltage	V_{ICMP}	PREAMP Gain = 1V/V $CMR_{PRE} \geq 70dB$	GND +0.05	-	V_{CC}-1	V

Unless otherwise specified, all limits ensured for $T_a = 25°C$, $V_{DD} = V_{REFIN} = V_{REFA+} = 3V$, Auxiliary Input Mode
ADC Chopping = ON, ADC Reference Voltage = External, ADC Gain = 1V/V, ADC Decimation Ratio = "320"

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ADC						
Resolution	N	No missing code(6)	16	-	-	Bit
Noise Free Bit	NFB		-	16	-	Bit
Conversion Time	DR	See p.22 "ADC Conversion Time"	-	-	-	SPS
Output Noise	V_{nADC}	VREFA+ = 3V	-	13.9	-	µVrms
Integral Non Linearity	INL		-	±1	-	LSB
Gain Error		ADC Gain = 1V/1V to 8V/1V	-	±0.1	-	%
Offset Error		AUXIN+ = AUXIN- = V_{DD}/2	-	±1	-	LSB
Differential Input Voltage Range	V_{IDADC}	V_{REF} = |(VREFA+)-(VREFA-)|	-	$\pm V_{REF}$	-	V
ADC Common Mode Rejection	CMR_{ADC}	AUXIN+ = AUXIN- = GND to V_{DD}	80	90	-	dB
ADC Common Mode Input Voltage Range	V_{ICADC}	$CMR_{ADC} \geq 80dB$	GND	-	V_{DD}	V

(6) This Parameter is not production tested, please refer Typical Characteristics.

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply / OSC						
Voltage Range	V_{DD}		2.4	-	3.6	V
Bias Resistance	R_{BIAS}		-	1.5	-	MΩ
Supply Current 1	I_{DD1}	All Circuit Block Off	-	0.5	1	µA
Supply Current 2	I_{DD2}	OPA、OPB	-	4	5.5	µA
Supply Current 3	I_{DD3}	Internal Reference Voltage (2.048V)	-	31	40	µA
Supply Current 4	I_{DD4}	PREAMP	-	55	75	µA
Supply Current 5	I_{DD5}	ADC	-	150	200	µA
OSC Frequency	f_{OSC}	±10%	276	307	338	kHz

■CHARACTERISTICS OF I/O STAGES FOR I²C-BUS Compatible (SDA, SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 200pF (Connected to GND)

FASE MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard Mode			Fast Mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	$0.3V_{DD}$	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	$0.7V_{DD}$	-	5.5	2.7	-	5.5	V
Low Level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DD}$ max.	I_i	-10	-	10	-10	-	10	µA

■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C-BUS Compatible Devices

I²C BUS Load Conditions

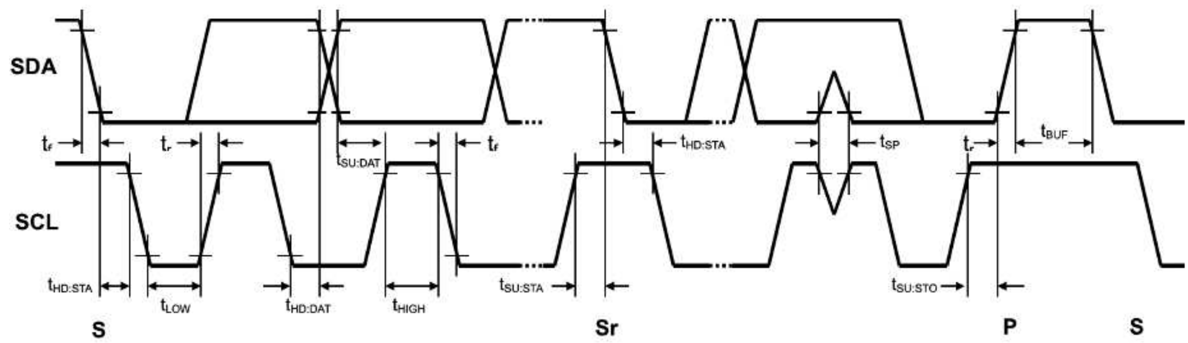
STANDARD MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 200pF (Connected to GND)

FASE MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard Mode			Fast Mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	10	-	100	10	-	400	kHz
Hold time (repeated) START condition	$t_{HD:STA}$	4.0	-	-	0.6	-	-	µs
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	µs
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	µs
Data hold time	$t_{HD:DAT}$	0	-	-	0	-	-	µs
Data set-up time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	µs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low Level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High Level	V_{nH}	1	-	-	1	-	-	V

C_b: Total capacitance of one bus line in pF.

■TIMING ON THE I²C BUS (SDA, SCL)



■CHARACTERISTICS OF I/O STAGES FOR EEPROM I^2C-BUS (EXSDA, EXSCL)

I^2C BUS Load Conditions

Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL}	0.0	-	$0.3V_{DD}$	V
High Level Input Voltage	V_{IH}	$0.7V_{DD}$	-	-	V
Low Level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DD}$ max.	I_i	-10	-	10	µA

■CHARACTERISTICS OF BUS LINES (EXSDA, EXSCL)

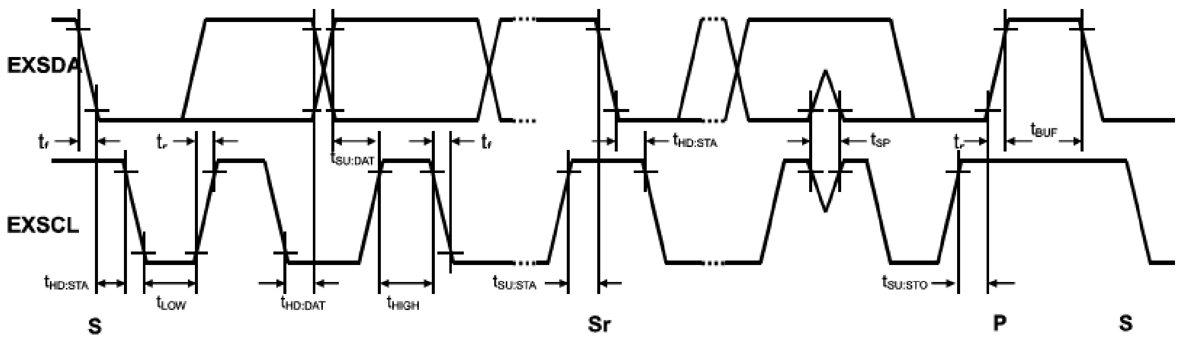
I^2C BUS Load Conditions

Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
EXSCL clock frequency	f_{SCL}	92	102.3	112.7	kHz
Hold time (repeat) START condition	$t_{HD:STA}$	7.2	6.5	5.9	µs
Low period of the EXSCL clock	t_{LOW}	7.2	6.5	5.9	µs
High period of the EXSCL clock	t_{HIGH}	3.6	3.3	3.0	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	7.2	6.5	5.9	µs
Data hold time (EXSDA input)	$t_{HD:DAT}$	0	-	-	µs
Data hold time (EXSDA output)	$t_{HD:DAT}$	7.2	6.5	5.9	µs
Data Set-up time (EXSDA input)	$t_{SU:DAT}$	0	-	-	µs
Data Set-up time (EXSDA output)	$t_{SU:DAT}$	7.2	6.5	5.9	µs
Rise time of both SDA and SCL signals	t_r	-	-	300	ns
Fall time of SDA and SCL signals	t_f	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	7.2	6.5	5.9	µs
Bus free time between a STOP and START condition	t_{BUF}	7.2	6.5	5.9	µs
Capacitive load for each bus line	C_b	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	V

C_b: total capacitance of one bus line in pF.

■TIMING ON THE EEPROM I2C BUS (EXSDA, EXSCL)



■REGISTER DESCRIPTION

NJU9101 has register (list shown below) which can access it through I^{2}C bus.
It can control the external EEPROM address corresponding to each register address from NJU9101.

REGISTER ADDRESS	EEPROM ADDRESS	REGISTER NAME	BIT							
			D7	D6	D5	D4	D3	D2	D1	D0
0x00	-	CTRL	-	RST	SENSCK [1:0]		MEAS	MEAS_SEL [1:0]		MEAS_SC
0x01	-	STATUS	-	-	BOOT	CLKRUN	RDYB	OV	CERR	OFOV
0x02	-	AMPDATA0	AMPDATA [15:8]							
0x03	-	AMPDATA1	AMPDATA [7:0]							
0x04	-	AUXDATA0	AUXDATA [15:8]							
0x05	-	AUXDATA1	AUXDATA [7:0]							
0x06	-	TMPDATA0	TMPDATA [9:2]							
0x07	-	TMPDATA1	TMPDATA [1:0]		-	-	-	-	-	-
0x08	-	ID	ID [7:0]							
0x09	-	ROMADR0	-	-	-	-	-	ROMADR [10:8]		
0x0A	-	ROMADR1	ROMADR [7:0]							
0x0B	-	ROMDATA	ROMDATA [7:0]							
0x0C	-	ROMCTRL	-	-	ROMERR	ROMBUSY	ROMSTOP	ROMACT	ROMMODE [1:0]	
0x0D	-	TEST	TEST [7:0]							
0x0E	0x000	ANAGAIN	-	-	-	-	PRE_GAIN [1:0]		ADC_GAIN [1:0]	
0x0F	0x001	BLKCONN0	-	-	BIASSWA	BIASSWB	PRE_BIAS [3:0]			
0x10	0x002	BLKCONN1	OPA_BIAS [2:0]			OPB_BIAS [4:0]				
0x11	0x003	BLKCONN2	PREMODE	INPSWA	INPSWB	ANASW	BIASSWN	PAMPSEL	BIASSEL	VREFSEL
0x12	0x004	BLKCTRL	BLKCTRL [7:0]							
0x13	0x005	ADCCONV	-	ADCCHOP	CLKDIV [1:0]		REJ [1:0]		OSR [1:0]	
0x14	0x006	SYSPRESET	RDYBOE	RDYBDAT	RDYBMODE [1:0]		-	-	-	AMPAUX
0x15	0x007	SCAL1A0	-	-	-	-	-	-	-	SCAL1A [8]
0x16	0x008	SCAL1A1	SCAL1A [7:0]							
0x17	0x009	SCAL2A0	-	-	-	-	-	-	-	SCAL2A [8]
0x18	0x00A	SCAL2A1	SCAL2A [7:0]							
0x19	0x00B	SCAL3A0	-	-	-	-	-	-	-	SCAL3A [8]
0x1A	0x00C	SCAL3A1	SCAL3A [7:0]							
0x1B	0x00D	SCAL4A0	-	-	-	-	-	-	-	SCAL4A [8]
0x1C	0x00E	SCAL4A1	SCAL4A [7:0]							
0x1D	0x00F	SCAL1B0	SCAL1B [15:8]							
0x1E	0x010	SCAL1B1	SCAL1B [7:0]							
0x1F	0x011	SCAL2B0	SCAL2B [15:8]							
0x20	0x012	SCAL2B1	SCAL2B [7:0]							
0x21	0x013	SCAL3B0	SCAL3B [15:8]							
0x22	0x014	SCAL3B1	SCAL3B [7:0]							
0x23	0x015	SCAL4B0	SCAL4B [15:8]							
0x24	0x016	SCAL4B1	SCAL4B [7:0]							
0x25	0x017	OCAL1A0	-	-	-	-	-	-	OCAL1A [9:8]	
0x26	0x018	OCAL1A1	OCAL1A [7:0]							

0x27	0x019	OCAL2A0	-	-	-	-	-	-	OCAL2A [9:8]
0x28	0x01A	OCAL2A1	OCAL2A [7:0]						
0x29	0x01B	OCAL3A0	-	-	-	-	-	-	OCAL3A [9:8]
0x2A	0x01C	OCAL3A1	OCAL3A [7:0]						
0x2B	0x01D	OCAL4A0	-	-	-	-	-	-	OCAL4A [9:8]
0x2C	0x01E	OCAL4A1	OCAL4A [7:0]						
0x2D	0x01F	OCAL1B0	-	OCAL1B [14:8]					
0x2E	0x020	OCAL1B1	OCAL1B [7:0]						
0x2F	0x021	OCAL2B0	-	OCAL2B [14:8]					
0x30	0x022	OCAL2B1	OCAL2B [7:0]						
0x31	0x023	OCAL3B0	-	OCAL3B [14:8]					
0x32	0x024	OCAL3B1	OCAL3B [7:0]						
0x33	0x025	OCAL4B0	-	OCAL4B [14:8]					
0x34	0x026	OCAL4B1	OCAL4B [7:0]						
0x35	0x027	SCAL1	SCAL1 [7:0]						
0x36	0x028	SCAL2	SCAL2 [7:0]						
0x37	0x029	SCAL3	SCAL3 [7:0]						
0x38	0x02A	OCAL1	OCAL1 [7:0]						
0x39	0x02B	OCAL2	OCAL2 [7:0]						
0x3A	0x02C	OCAL3	OCAL3 [7:0]						
0x3B	0x02D	AUXSCAL0	AUX_SCAL [15:8]						
0x3C	0x02E	AUXSCAL1	AUX_SCAL [7:0]						
0x3D	0x02F	AUXOCAL0	AUX_OCAL [15:8]						
0x3E	0x030	AUXOCAL1	AUX_OCAL [7:0]						
0x3F	-	CHKSUM	CHKSUM [7:0]						

■EVERY REGISTER DESCRIPTION

CTRL Register Register Address: 0x00, EEPROM Address: -

CTRL								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	RST	SENSCK [1:0]		MEAS	MEAS_SEL [1:0]		MEAS_SC
R / W	-	WS	RW		RW	RW		RW
RESET	-	-	0x0		0	0x0		0

BIT	BIT NAME	FUNCTION
[6]	RST	Write Software Reset. When read this bit, always return “0”. 0: No effect 1: Reset
[5:4]	SENSCK	Change offset voltage of OPB to check sensor diagnostic. 00: OFF (No change) 01: Plus Offset (Change Offset Voltage ≈ +5.0mV) 10: Minus Offset (Change Offset Voltage ≈ -5.0mV) 11: Reserve
[3]	MEAS	Measurement Switch When write “1”, ADC conversion starts. When read this bit, returns “1” in case of under conversion, “0” in case of idle condition. When select “Single Conversion” mode, this bit is set to “0” automatically after conversion completion. When select “Continuous Conversion” mode and write “0”, ADC conversion stop and return to an idol state. 0: Measurement OFF (Operating condition of this chip follows “BLKCTRL” condition) 1: Measurement ON
[2:1]	MEAS_SEL	Measurement Mode Selection. 00: Temperature sensor input mode 01: Amplifier input mode 10: Auxiliary input mode 11: Reserve
[0]	MEAS_SC	Measurement Mode for ADC 0: Single Conversion 1: Continuous Conversion

STATUS Register Register Address: 0x01, EEPROM Address: -

STATUS								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	BOOT	CLKRUN	RDYB	OV	CERR	OFOV
R / W	-	-	R	R	R	R	R	R
RESET	-	-	1	-	1	0	0	0

BIT	BIT NAME	FUNCTION
[5]	BOOT	Booting flag for IC. NJU9101 reads initial register value from external EEPROM as booting. This bit returns “1” until the reading of the initial register value is completed from start. 0: Completion of booting 1: Under booting
[4]	CLKRUN	System Clock Condition. 0: System Clock is sleeping 1: System Clock is operating
[3]	RDYB	Data Ready Flag. When conversion data is updated, this bit is cleared to “0”. When either “AMPDATA0”, “AUXDATA0”, or “TMPDATA” is read, this bit is set to “1”. 0: New ADC data is ready 1: New ADC data is not ready
[2]	OV	Overflow flag in sensitivity calibration of ADC output data. When over flow is occurred in sensitivity calibration of ADC conversion data, this bit is set to “1”. When this bit is “1”, ADC output data (“AMPDATA” or “AUXDATA”) is set to 0x7FFF (positive over flow) or 0x8000 (negative over flow). When either “AMPDATA0”, “AUXDATA0”, or “TMPDATA” is read, this bit is cleared to “0”. 0: ADC conversion data is valid 1: ADC conversion data is over flow (set 0x7FFF or 0x8000)
[1]	CERR	Overflow flag in calibration coefficient data. When over flow is occurred in setting of calibration coefficient data, this bit is set to “1”. In case of “1”, ADC output data is invalid value. When either “AMPDATA0”, “AUXDATA0” or “TMPDATA” is read, this bit is cleared to “0”. 0: No overflow in calibration coefficient calculation 1: Overflow in calibration coefficient calculation (Output data is invalid)
[0]	OFOV	Overflow flag in offset calibration of ADC output data. When over flow is occurred in offset calibration of ADC conversion data, this bit is set to “1”. In case of “1”, ADC output data is invalid value. When either “AMPDATA0”, “AUXDATA0” or “TMPDATA” is read, this bit is cleared to “0”. 0: No overflow in offset calibration data 1: Overflow in offset calibration data (Output data is invalid)

AMPDATA0 / AMPDATA1 Register Register Address: 0x02 / 0x03, EEPROM Address: -

	AMPDATA0 Register Address: 0x02								AMPDATA1 Register Address: 0x03							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AMPDATA [15:0]															
R / W	R															
RESET	-															

BIT	BIT NAME	FUNCTION
AMPDATA0 [7:0] + AMPDATA1 [7:0]	AMPDATA[15:0]	ADC output data register for amplifier input mode. Singed 16-Bit data.

AUXDATA0 / AUXDATA1 Register Register Address: 0x04 / 0x05, EEPROM Address: -

	AUXDATA0 Register Address: 0x04								AUXDATA1 Register Address: 0x05							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AUXDATA [15:0]															
R / W	R															
RESET	-															

BIT	BIT NAME	FUNCTION
AUXDATA0 [7:0] + AUXDATA1 [7:0]	AUXDATA[15:0]	ADC output data register for Auxiliary input mode. Signed 16-Bit data.

TMPDATA0 / TMPDATA1 Register Register Address: 0x06 / 0x07, EEPROM Address: -

	TMPDATA0 Register Address: 0x06								TMPDATA1 Register Address: 0x07							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	TMPDATA [9:0]										-	-	-	-	-	-
R / W	R/W										-	-	-	-	-	-
RESET	-										-	-	-	-	-	-

ビット	ビット名	機能
TMPDATA0 [7:0] + TMPDATA1 [7:6]	TMPDATA[9:0]	ADC output data register for Temperature sensor input mode. Signed 8.2 fixed point format. (-45°C to +127.75°C) Temperature calibration calculation is executed by value of TEMPDATA. When calibration is executed by using external temperature sensor, write data which getting from external temperature sensor to this register.

ID Register Register Address: 0x08, EEPROM Address: -

	ID							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ID [7:0]							
R / W	R							
RESET	0x55							

BIT	BIT NAME	FUNCTION
[7:0]	ID	Fixed value “0x55” is stored as a chip identification code in this register.

ROMADR0 / ROMADR1 Register Register Address: 0x09 / 0x0A, EEPROM Address: -

	ROMADR0								ROMADR1							
	Register Address: 0x09								Register Address: 0x0A							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	ROMADR [10:0]										
R / W	-	-	-	-	-	RW										
RESET	-	-	-	-	-	0x0										

ビット	ビット名	機能
ROMADR0 [2:0] + ROMADR1 [7:0]	ROMADR[10:0]	This is EEPROM address selection register that read/write from/to EEPROM.

*Be sure to set ROMADR0[4:3] = “00” to control EEPROM.

ROMDATA Register Register Address: 0x0B, EEPROM Address: -

	ROMDATA							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ROMDATA [7:0]							
R / W	RW							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[7:0]	ROMDATA	In read mode, return a reading data from EEPROM. In write mode, set a writing data to EEPROM.

*Be sure to set ROMADR0[4:3] = “00” to control EEPROM.

ROMCCTL Register Register Address: 0x0C, EEPROM Address: -

ROMCCTL								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	ROMERR	ROMBUSY	ROMSTOP	ROMACT	ROMMODE [1:0]	
R / W	-	-	RC	R	WS	WS	W	
RESET	-	-	-	-	0x0	0x0	0x0	

BIT	BIT NAME	FUNCTION
[5]	ROMERR	When I^2C bus communication error occurs during accessing to external EEPROM, this bit is set to "1". It is communication error in the following cases, 1) When NJU9101 outputs address, data, acknowledge data, it receives the EXSDA data different from the EXSDA data which outputs. 2) NJU9101 receives NACK response in the timing which it is expected to receive ACK response. And, It is cleared to "0" when this bit is written in "1". 0: I2C communication is not error 1: I2C communication is error
[4]	ROMBUSY	This bit shows accessing status to external EEOPROM. 0: Completion of the access 1: Under accsessing
[3]	ROMSTOP	When write "1" to "ROMSTOP" bit, stop accessing to external EEPROM. "ROMBUSY" bit is cleared to "0" immediately. When it stops accessing during writing to external EEPROM, ROM data is not guaranteed. In the read mode, this bit always returns "0". 1: stop accessing to external EEPROM
[2]	ROMACT	When write "1" to ROMACT bit, start accessing to external EEPROM with following "ROMMODE[1:0]" data. In write "0" case, it is not started accessing. And, to start accessing to external EEPROM, it is necessary that it is not accessing timing to external EEPROM ("ROMBUSY" bit = "0"), and system clock is during operation ("CLKRUN" bit = "1"). In the read mode, this bit always returns "0". 1: start accessing to external EEPROM
[1:0]	ROMMODE	Write operation for external EEPROM. In the read mode, this bit returns "0". 00: Read one byte data from external EEPROM (address ROMADR[10:0]), and, store this one byte data to ROMDATA[7:0] bit register in NJU9101. 01: Write ROMDATA[7:0] bit data to register in external EEPROM which is assigned by ROMADR[10:0] address. 10: Load external EEPROM data to Host-register (ex. MPU) 11: Store Host-register setting (ex. MPU) into external EEPROM data.

*Be sure to set ROMADR0[4:3] = "00" to control EEPROM.

TEST Register Register Address: 0x0D, EEPROM Address: –

TEST								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	TEST [7:0]							
R / W	RW							
RESET	0x00							

*This register if for production test purpose. Do not write data to this register.

ANAGAIN Register Register Address: 0x0E, EEPROM Address: 0x000

ANAGAIN								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	PRE_GAIN [1:0]		ADC_GAIN [1:0]	
R / W	-	-	-	-	RW		RW	
RESET	-	-	-	-	0x0		0x0	

BIT	BIT NAME	FUNCTION
[3:2]	PRE_GAIN	Pre-amplifier gain selection 00: 1 V/V 01: 2 V/V 10: 4 V/V 11: 8 V/V
[1:0]	ADC_GAIN	Programmable-gain-amplifier in ADC selection 00: 1 V/V 01: 2 V/V 10: 4 V/V 11: 8 V/V

BLKCONN0 Register Register Address: 0x0F, EEPROM Address: 0x001

BLKCONN0								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	BIASSWA	BIASSWB	PRE_BIAS [3:0]			
R / W	-	-	RW	RW	RW			
RESET	-	-	0x0	0x0	0x0			

BIT	BIT NAME	FUNCTION
[5]	BIASSWA	This is Switch for connecting “BIASRES” and “OPA positive input” 00: Open “BIASRES” and “OPA positive input” 01: Connect “BIASRES” and “OPA positive input”
[4]	BIASSWB	This is Switch for connecting “BIASRES” and “OPB positive input” 00: Open “BIASRES” and “OPB positive input” 01: Connect “BIASRES” and “OPB positive input”
[3:0]	PRE_BIAS	Negative input bias level for PREAMP (From 0.3V to 1.7V are 100mV steps) This bias level is set by “BIASRES” Circuit Block. V_{REFIN} = 3V or at INTVREF(2.048V) as follows 0000: GND 0001: 0.3V 0010: 0.4V 0011: 0.5V : : 1101: 1.5V 1110: 1.6V 1111: 1.7V

BLKCONN1 Register Register Address: 0x10, EEPROM Address: 0x002

BLKCONN1								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OPA_BIAS [2:0]			OPB_BIAS [4:0]				
R / W	RW			RW				
RESET	0x0			0x0				

BIT	BIT NAME	FUNCTION
[7:5]	OPA_BIAS	Bias Level for OPA, This bias level is set by “BIASRES” Block. V_{REFIN} = 3V or at INTVREF(2.048V) as follows 000: GND 001: 0.3V 010: 0.5V 011: 0.7V 100: 1.0V 101: 1.3V 110: 1.5V 111: 1.7V
[4:0]	OPB_BIAS	Bias Level for OPB (From 0.25V to 1.75V are 50mV steps). V_{REFIN} = 3V or at INTVREF(2.048V) as follows 00000: GND 00001: 0.25V 00010: 0.3V 00011: 0.35V : 11101: 1.65V 11110: 1.7V 11111: 1.75V

BLKCONN2 Register Register Address: 0x11, EEPROM Address: 0x003

BLKCONN2								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	PREMODE	INPSWA	INPSWB	ANASW	BIASSWN	PAMPSEL	BIASSEL	VREFSEL
R / W	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

BIT	BIT NAME	FUNCTION
[7]	PREMODE	Select PREAMP mode 0: Non-Inverted Amplifier mode 1: Instrumentation Amplifier mode
[6]	INPSWA	OPA positive input connection 0: GND Positive input is connected to GND. 1: AINP Positive input is connected to AINP Pin.
[5]	INPSWB	OPB positive input connection 0: GND Positive input is connected to GND. 1: BINP Positive input is connected to BINP Pin.
[4]	ANASW	Build in Analog Switch Status 0: Switch OFF 1: Switch ON On Resistance is 10Ω typ. Absolute Maximum Input Current is ±50mA.
[3]	BIASSWN	Select switch for PREAMP / ADC Negative Input at AMP / AUX input mode. 0: OPB Output / AUXIN- 1: BIASRES This is selectable bias level set by “PRE-BIAS”.
[2]	PAMPSEL	Enable / Disable PREAMP for signal path. 0: Disable (Bypass PREAMP) 1: Enable
[1]	BIASSEL	Reference Voltage selection for Bias Register 0: Internal Reference (2.048V) 1: External Reference
[0]	VREFSEL	Reference Voltage selection for ADC 0: Internal Reference (2.048V) 1: External Reference

BLKCTRL Register Register Address: 0x12, EEPROM Address: 0x004

BLKCNT								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	BLKCTRL [7:0]							
R / W	RW							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[7:0]	BLKCTRL	Circuit Block Powered down selection. When ADC is in the idle state, circuit block which this bit is set to “0” is automatically powered down. The circuit block which this bit is set to “1” is kept powered on state even in case of ADC idle state. When all bits are “0”, NJU9101 goes “power down mode” except for Digital block. [7]: BIASRES block [6]: OPB block [5]: OPA block [4]: OSC block [3]: PREAMP block [2]: INTVREF(2.048V) block [1]: ADC block [0]: Temperature Sensor block

ADCCONV Register Register Address: 0x13, EEPROM Address: 0x005

ADCCONV								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	ADCCHOP	CLKDIV [1:0]		REJ [1:0]		OSR [1:0]	
R / W	-	RW	RW		RW		RW	
RESET	-	0x0	0x0		0x0		0x0	

BIT	BIT NAME	FUNCTION
[6]	ADCCHOP	ADC CHOP Switch. It's effective in reducing offset Voltage of PREAMP and ADC. Reduce offset voltage by chopping input signal. When this bit is “1”, conversion time becomes long. (ex. 16.2ms(ADCCHOP=”0”) -> 31.1ms(ADCCHOP=”1”)) 0: CHOP OFF 1: CHOP ON
[5:4]	CLKDIV	Select operation clock frequency for sigma-delta modulator. f_{OSC}=307.2kHz typ. 00: f_{mod}=(1/2) x f_{OSC} 01: f_{mod}=(1/4) x f_{OSC} 10: f_{mod}=(1/8) x f_{OSC} 11: f_{mod}=(1/16) x f_{OSC}
[3:2]	REJ	Select rejection mode for Sinc3 filter 00: 50/60Hz Rejection 01: 50Hz Rejection 10: 60Hz Rejection 11: Reserved
[1:0]	OSR	Select Decimation ratio for Sinc3 filter. Total Decimation Ratio is decided by REJ / OSC bits combination.

ADC Decimation Ratio

OSR [1:0]	REJ [1:0] 00	01	10	11
00	768	768	640	-
01	384	384	320	-
10	192	192	160	-
11	96	96	80	-

ADC Conversion Time [ms]

OSR [1:0]	REJ [1:0] 00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
00	16.2	16.2	13.7	-	31.3	31.3	26.3	-	5	5	4.2	-	15.3	15.3	12.8	-
01	8.7	8.7	7.5	-	16.3	16.3	13.8	-	2.5	2.5	2.1	-	7.8	7.8	6.5	-
10	5.0	5.0	4.3	-	8.8	8.8	7.6	-	1.3	1.3	1.0	-	4.0	4.0	3.4	-
11	3.1	3.1	2.8	-	5.1	5.1	4.5	-	0.6	0.6	0.5	-	2.1	2.1	1.8	-
State	Single Conversion								Continuous Conversion							
	CHOP: OFF				CHOP: ON				CHOP: OFF				CHOP: ON			

Conversion Time vs Resolution (ADC)

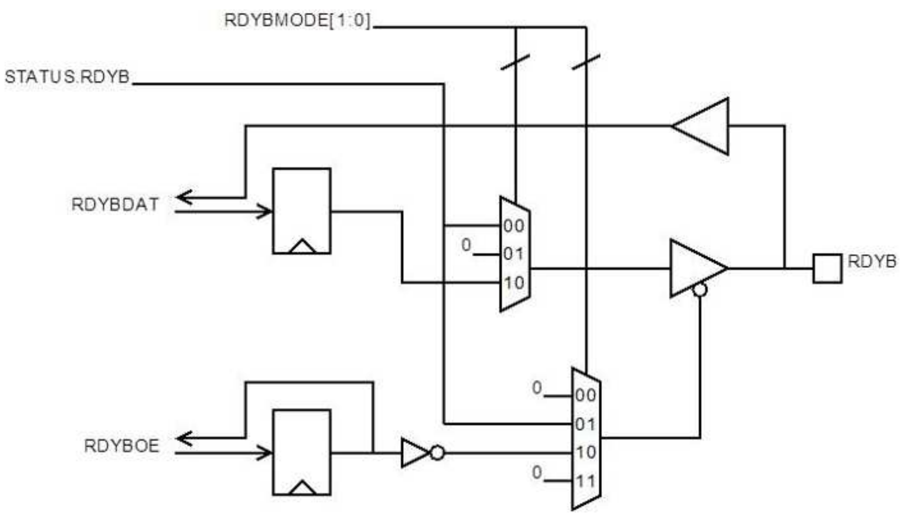
ADC Conversion Time	CHOP: ON				CHOP: OFF			
	ADC Gain				ADC Gain			
	1V/V	2V/V	4 V/V	8 V/V	1 V/V	2 V/V	4 V/V	8 V/V
26.3ms	16 / (16)	16 / (16)	16 / (16)	16 / (16)	16 / (16)	16 / (16)	15.6 / (16)	15.3 / (16)
13.8ms	16 / (16)	16 / (16)	15.2 / (16)	16 / (16)	16 / (16)	16 / (16)	15 / (16)	14.8 / (16)
7.6ms	15 / (16)	14.7 / (16)	14.5 / (16)	14 / (16)	15 / (16)	14.7 / (16)	14.1 / (16)	13.5 / (16)
4.5ms	14 / (16)	14 / (16)	13.5 / (16)	12 / (14.7)	14 / (16)	14 / (16)	13.6 / (16)	12 / (14.7)

Noise Free Bit / (Effective Number of Bits), Unit: bit

SYSPRESET Register Register Address: 0x14, EEPROM Address: 0x006

SYSPRESET								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	RDYBOE	RDYBDAT	RDYBMODE [1:0]		-	-	-	AMPAUX
R / W	RW	RW	RW		-	-	-	RW
RESET	0x0	-	0x1		-	-	-	0x0

BIT	BIT NAME	FUNCTION
[7]	RDYBOE	RDYB terminal direction of GPIO mode 0: RDYB terminal is input mode 1: RDYB terminal is Output mode
[6]	RDYBDAT	Return RDYB terminal level in input mode. Store RDYB terminal level in Output mode.
[5:4]	RDYBMODE	Select function of RDYB terminal 00: RDYB terminal outputs “RDYB” bit in STATUS register. 01: RDYB terminal outputs “RDYB” bit in STATUS register. with open-drain circuit style. 10: RDYB terminal is used as GPIO. Output condition is set by “RDYBDAT” and “RDYBOE”. 11: Reserved
[0]	AMPAUX	Select Calibration channel coefficient assignment. 0: AMPDATA uses SCAL/OCAL calibration coefficient. AUXDATA uses AUX_SCAL / AUX_OCAL calibration coefficient. 1: AMPDATA uses AUX_SCAL / AUX_OCAL calibration coefficient. AUXDATA uses SCAL/OCAL calibration coefficient.



SCALxA0 / SCALxA1 Register Register Address: 0x15 to 0x1C, EEPROM Address: 0x007 to 0x00E

	SCALxA0 (x=1 to 4) Register Address: 0x15, 0x17, 0x19, 0x1B EEPROM Address: 0x007, 0x009, 0x00B, 0x00D								SCALxA1 (x=1 to 4) Register Address: 0x16, 0x18, 0x1A, 0x1C EEPROM Address: 0x008, 0x00A, 0x00C, 0x00E							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	-	-	SCALxA [8:0]								
R / W	-	-	-	-	-	-	-	RW								
RESET	-	-	-	-	-	-	-	-								

BIT	BIT NAME	FUNCTION
SCALxA0 [0] + SCALxA1 [7:0]	SCALxA [8:0] (x=1 to 4)	1^{ST} order Gain Calibration parameter for AMPDATA. This parameter is signal 9-Bit data.

SCALxB0 / SCALxB1 Register Register Address: 0x1D to 0x24, EEPROM Address: 0x00F to 0x016

	SCALxB0 (x=1 to 4) Register Address: 0x1D, 0x1F, 0x21, 0x23 EEPROM Address: 0x00F, 0x011, 0x013, 0x15								SCALxB1 (x=1 to 4) Register Address: 0x1E, 0x20, 0x22, 0x24 EEPROM Address: 0x010, 0x012, 0x014, 0x016							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	SCALxB [15:0]															
R / W	RW															
RESET	-															

BIT	BIT NAME	FUNCTION
SCALxB0 [7:0] + SCALxB1 [7:0]	SCALxB [15:0] (x=1 to 4)	Zero-order Gain Calibration parameter for AMPDATA. This parameter is unsigned 16-Bit data.

OCALxA0 / OCALxA1 Register Register Address: 0x25 to 0x2C, EEPROM Address: 0x017 to 0x01E

	OCALxA0 (x=1 to 4) Register Address: 0x25 to 0x28 EEPROM Address: 0x017 to 0x01A								OCALxA1 (x=1 to 4) Register Address: 0x29 to 0x2C EEPROM Address: 0x01B to 0x01E							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	-	OCALxA [9:0]									
R / W	-	-	-	-	-	-	RW									
RESET	-	-	-	-	-	-	-									

BIT	BIT NAME	FUNCTION
OCALxA0 [1:0] + OCALxA1 [7:0]	OCALxA [9:0] (x=1 to 4)	1ST order Offset Calibration parameter for AMPDATA. This parameter is signed 10-Bit data.

OCALxB0 / OCALxB1 Register Register Address: 0x2D to 0x34, EEPROM Address: 0x01F to 0x026

	OCALxB0 (x=1 to 4) Register Address: 0x2D, 0x2F, 0x31, 0x33 EEPROM Address: 0x01F, 0x021, 0x023, 0x025								OCALxB1 (x=1 to 4) Register Address: 0x2E, 0x30, 0x32, 0x34 EEPROM Address: 0x020, 0x022, 0x024, 0x026							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	OCALxB [14:0]														
R / W	-	RW														
RESET	-	-														

BIT	BIT NAME	FUNCTION
OCALxB0 [6:0] + OCALxB1 [7:0]	OCALxB [14:0] (x=1 to 4)	Zero-order Offset Calibration parameter for AMPDATA. This parameter is signed 15-Bit data.

SCALx Register Register Address: 0x35 to 0x37, EEPROM Address: 0x027 to 0x029

	SCALx (x=1 to 3)							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	SCALx [7:0]							
R / W	RW							
RESET	-							

BIT	BIT NAME	FUNCTION
[7:0]	SCALx (x=1 to 3)	Threshold Temperature for AMPDATA Sensitivity Calibration. Signed 8.0 fixed point format. (-45°C to +127°C) -45°C ≤ SCAL1 < SCAL2 < SCAL3 ≤ +127°C

OCALx Register Register Address: 0x38 to 0x3A, EEPROM Address: 0x02A to 0x02C

OCALx (x=1 to 3)								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OCALx [7:0]							
R / W	RW							
RESET	-							

BIT	BIT NAME	FUNCTION
[7:0]	OCALx (x=1 to 3)	Threshold Temperature for AMPDATA Offset Calibration. Signed 8.0 fixed point format. (-45°C to +127°C) -45°C ≤ OCAL1 < OCAL2 < OCAL3 ≤ +127°C

AUX_SCAL0 / AUX_SCAL1 Register Register Address: 0x3B / 0x3C, EEPROM Address: 0x02D / 0x02E

	AUX_SCAL0 Register Address: 0x3B EEPROM Address: 0x02D								AUX_SCAL1 Register Address: 0x3C EEPROM Address: 0x02E							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AUXSCAL [15:0]															
R / W	RW															
RESET	-															

BIT	BIT NAME	FUNCTION
AUX_SCAL0 [7:0] + AUX_SCAL1 [7:0]	AUXSCAL [15:0]	Sensitivity Calibration for AUXDATA. (Auxiliary calibration does not have temperature coefficient).

AUX_OCAL0 / AUX_OCAL1 Register Register Address: 0x3D / 0x3E, EEPROM Address: 0x02F / 0x030

	AUX_OCAL0 Register Address: 0x3D EEPROM Address: 0x02F								AUX_OCAL1 Register Address: 0x3E EEPROM Address: 0x030							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AUXOCAL [15:0]															
R / W	RW															
RESET	-															

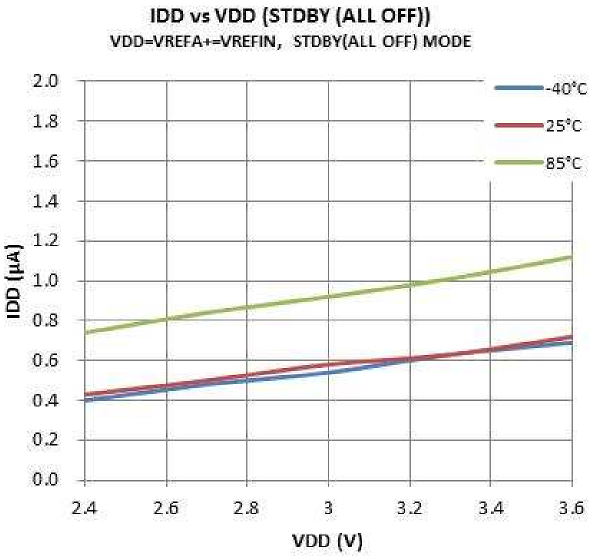
BIT	BIT NAME	FUNCTION
AUX_OCAL0 [7:0] + AUX_OCAL1 [7:0]	AUXOCAL [15:0]	Offset Calibration for AUXDATA. (Auxiliary calibration does not have temperature coefficient.)

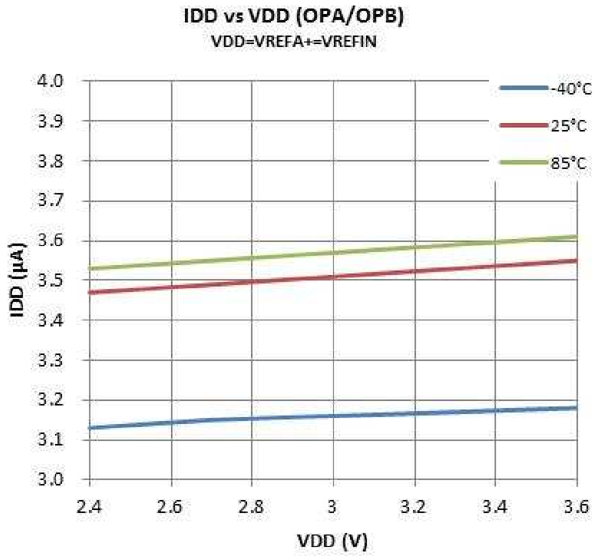
CHKSUM Register Register Address: 0x3F, EEPROM Address: -

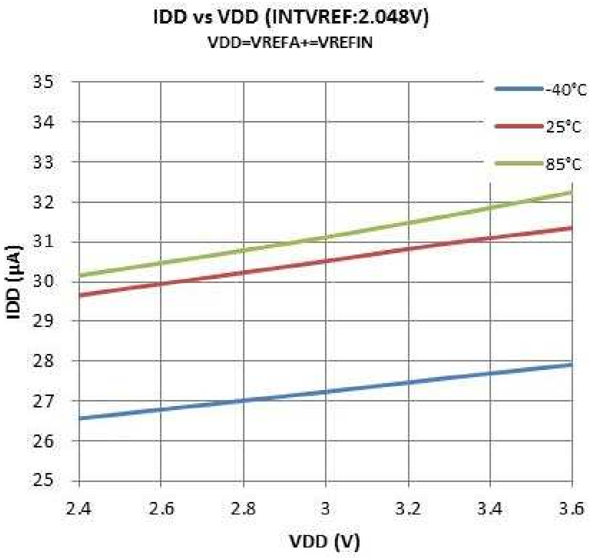
CHKSUM								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	CHKSUM [7:0]							
R / W	R							
RESET	-							

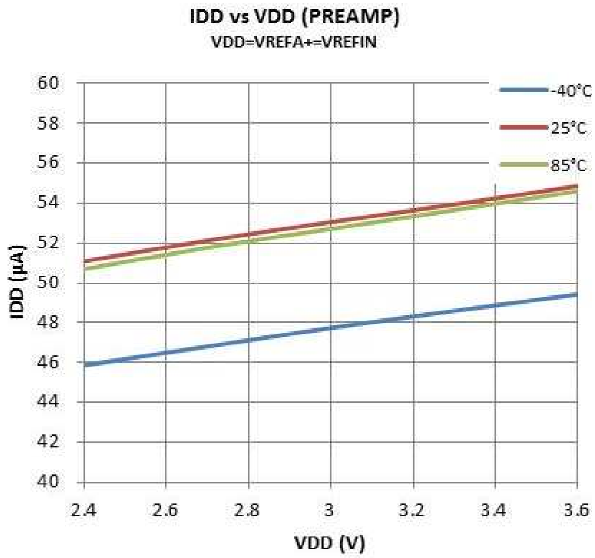
BIT	BIT NAME	FUNCTION
[7:0]	CHKSUM	Check Sum value of register set value is showed which is read from external EEPROM. Check Sum value is updated in following cases, when start up, when finish reading saved data from in external EEPROM, and when finish roading setting data to host-register from external EEPROM. Check Sum result value is finally showed as 1's complement. This result is summed unsigned data of each address byte (0x000 to 0x030) in external EEPROM.

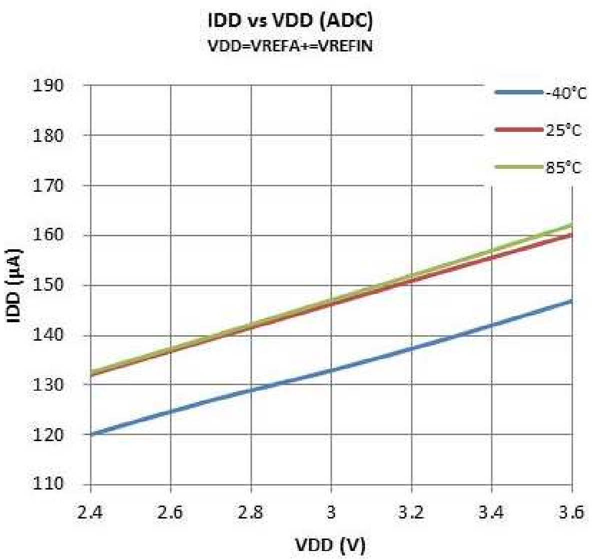
■TYPICAL CHARACTERISTICS

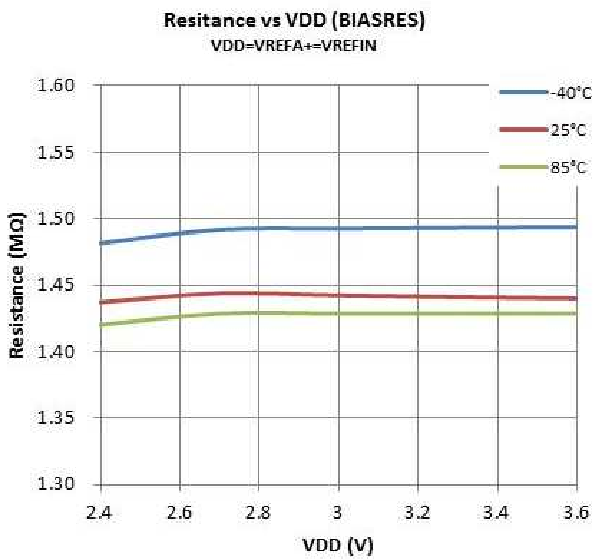


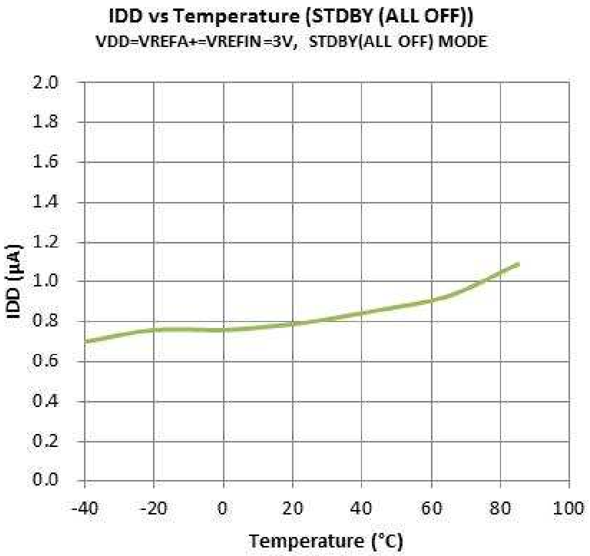


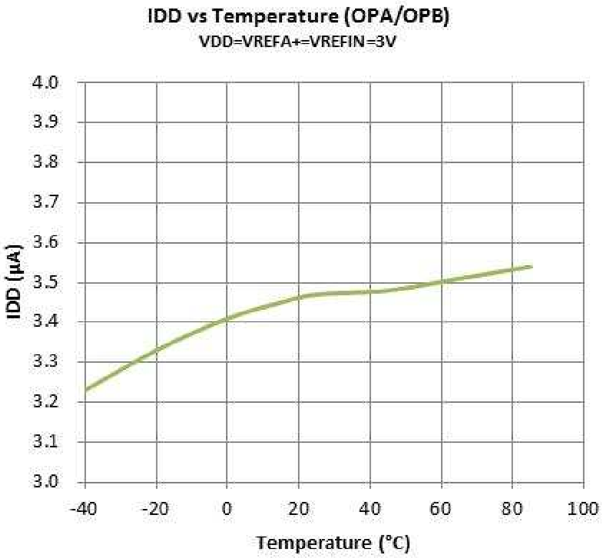


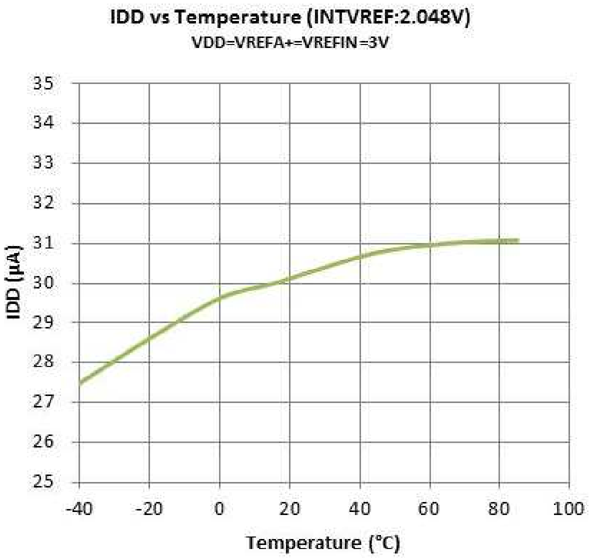


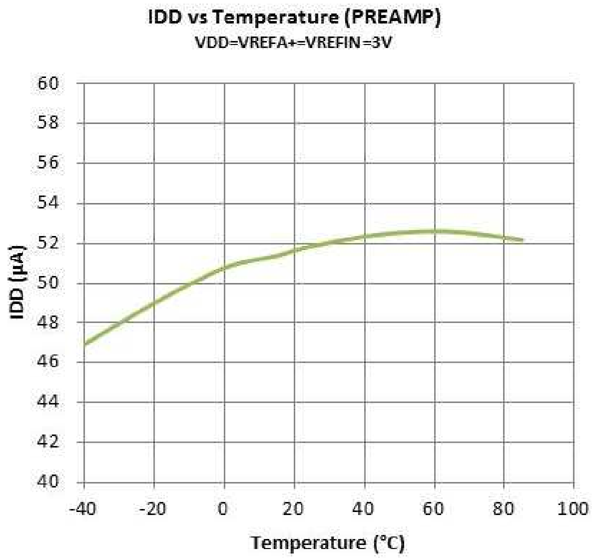


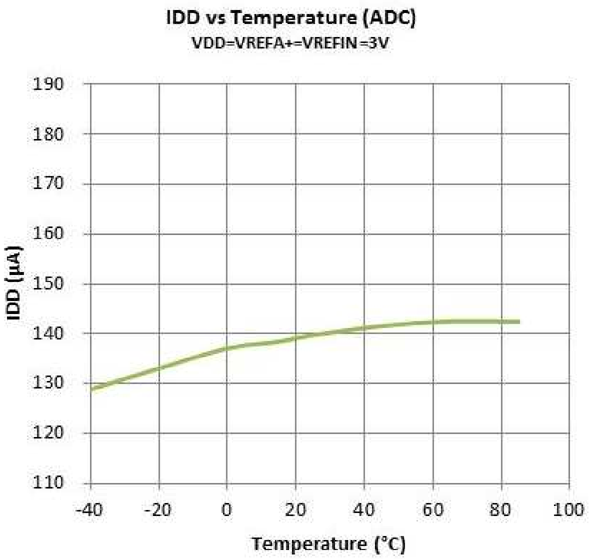


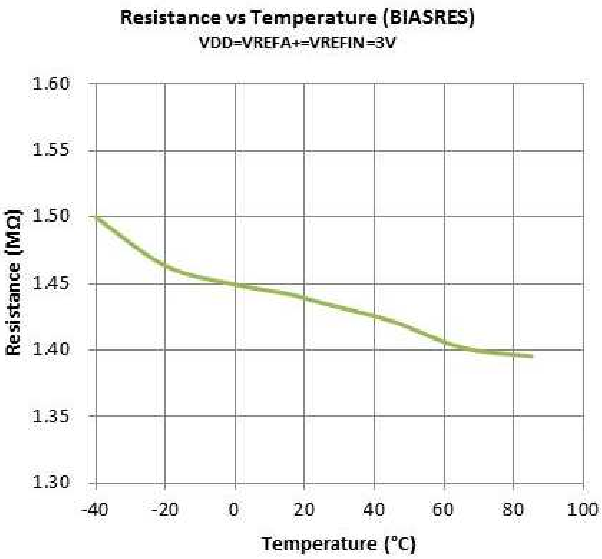

IDD vs Temperature (STDBY (ALL OFF))
VDD=VREFA+=VREFIN=3V, STDBY(ALL OFF) MODE
IDD (μA)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-40
-20
0
20
40
60
80
100
Temperature (°C)


IDD vs Temperature (OPA/OPB)
VDD=VREFA+=VREFIN=3V
IDD (μA)
4.0
3.9
3.8
3.7
3.6
3.5
3.4
3.3
3.2
3.1
3.0
-40
-20
0
20
40
60
80
100
Temperature (°C)

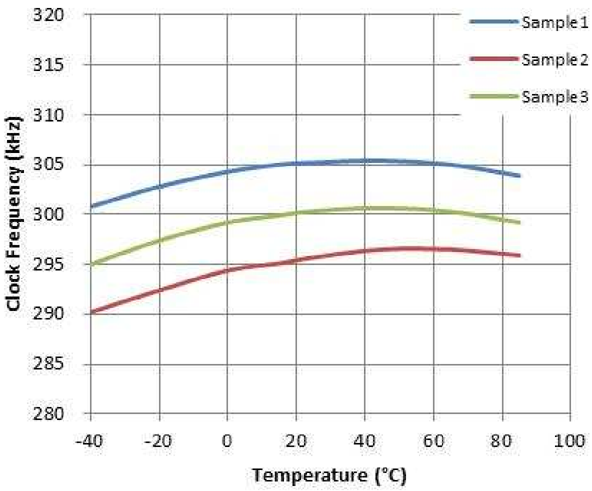

IDD vs Temperature (INTVREF:2.048V)
VDD=VREFA+=VREFIN=3V
IDD (μA)
35
34
33
32
31
30
29
28
27
26
25
-40
-20
0
20
40
60
80
100
Temperature (°C)


IDD vs Temperature (PREAMP)
VDD=VREFA+=VREFIN=3V
IDD (μA)
60
58
56
54
52
50
48
46
44
42
40
-40
-20
0
20
40
60
80
100
Temperature (°C)

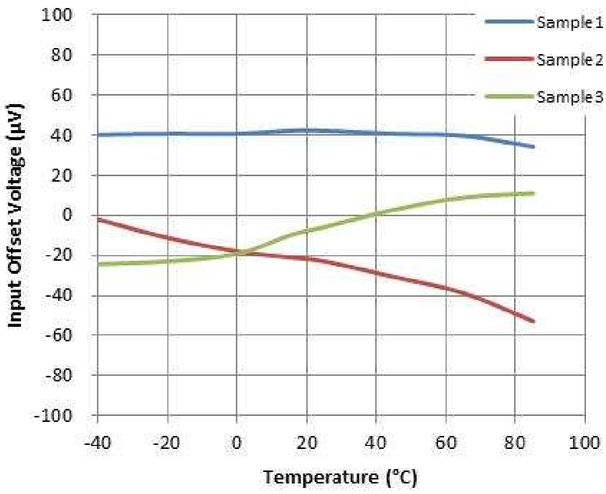

IDD vs Temperature (ADC)
VDD=VREFA+=VREFIN=3V
IDD (μA)
190
180
170
160
150
140
130
120
110
-40
-20
0
20
40
60
80
100
Temperature (°C)


Resistance vs Temperature (BIASRES)
VDD=VREFA+=VREFIN=3V
Resistance (MΩ)
1.60
1.55
1.50
1.45
1.40
1.35
1.30
-40
-20
0
20
40
60
80
100
Temperature (°C)

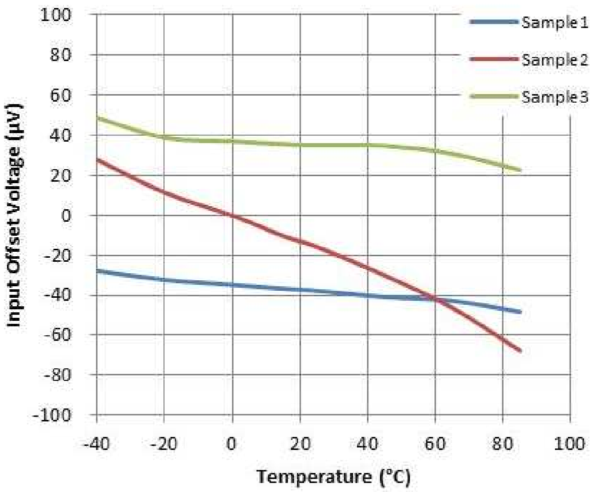
Clock Frequency vs Temperature (OSC)
VDD=VREFA+=VREFIN=3V



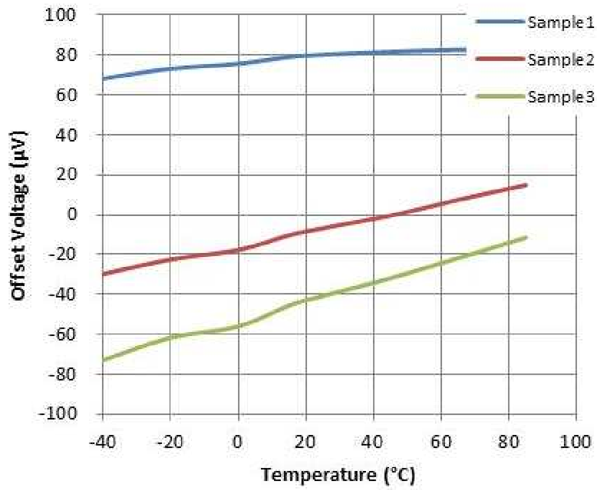
Input Offset Voltage vs Temperature (OPA)
VDD=VREFA+=VREFIN=3V, Null-Amp Method



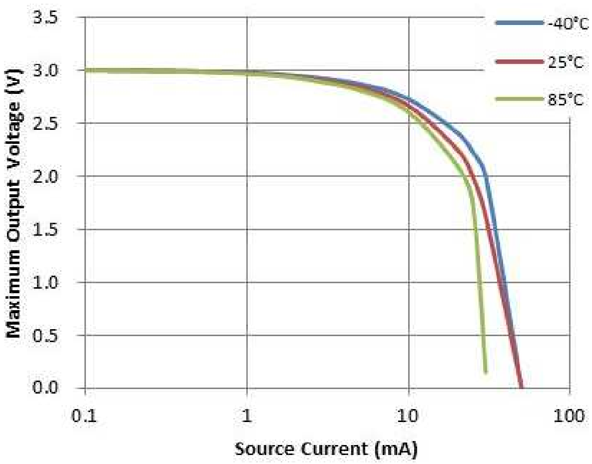
Input Offset Voltage vs Temperature (OPB)
VDD=VREFA+=VREFIN=3V, Null-Amp Method



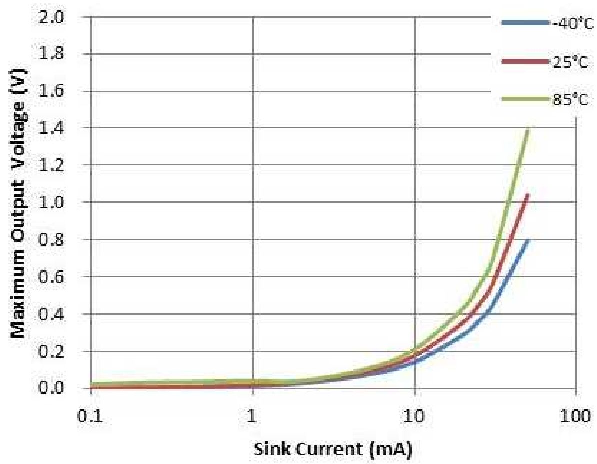
Offset Diffrence vs Temperature (OPA-OPB)
VDD=VREFA+=VREFIN=3V, Null-Amp Method

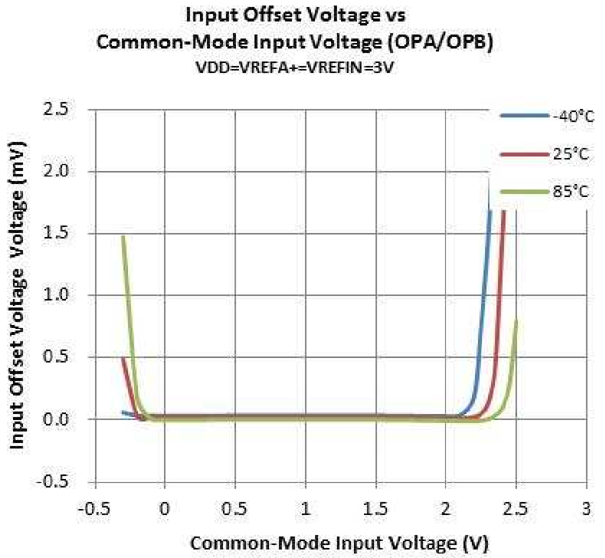


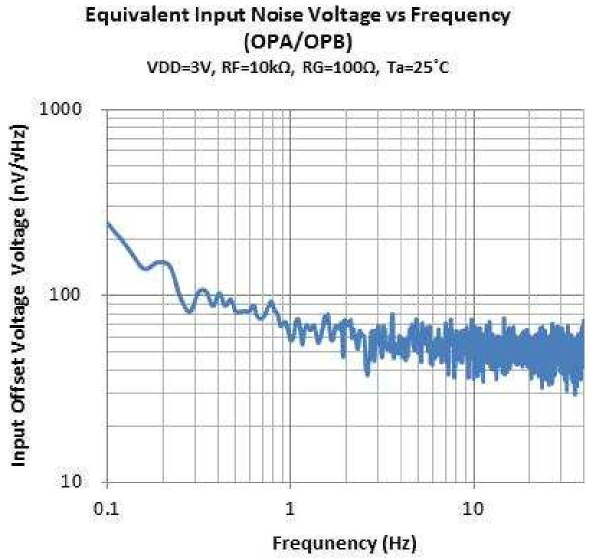
Maximum Output Voltage vs Source Current (OPA/OPB)
VDD=VREFA+=VREFIN=3V

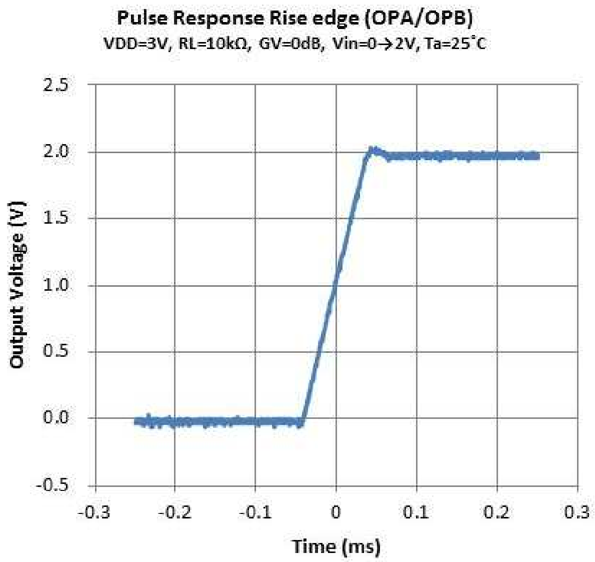


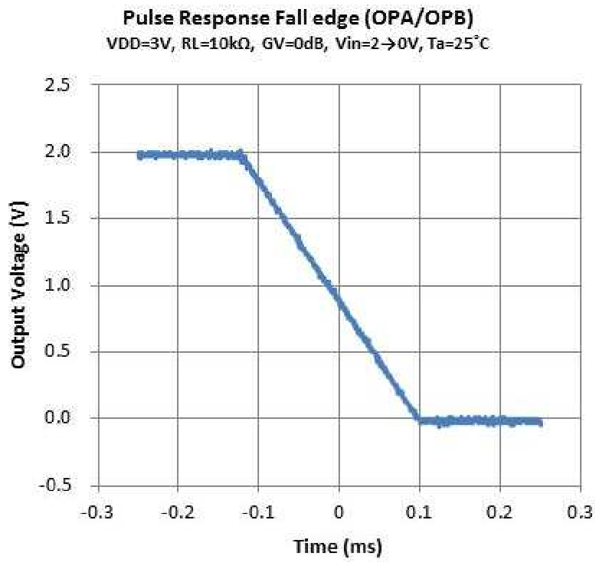
Maximum Output Voltage vs Sink Current (OPA/OPB)
VDD=VREFA+=VREFIN=3V

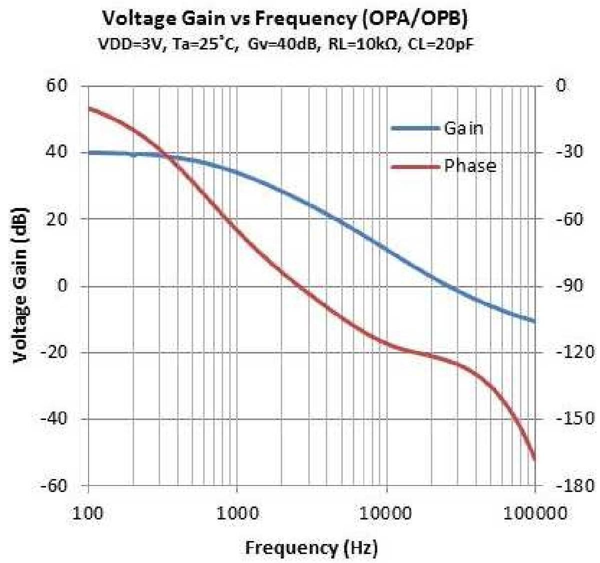


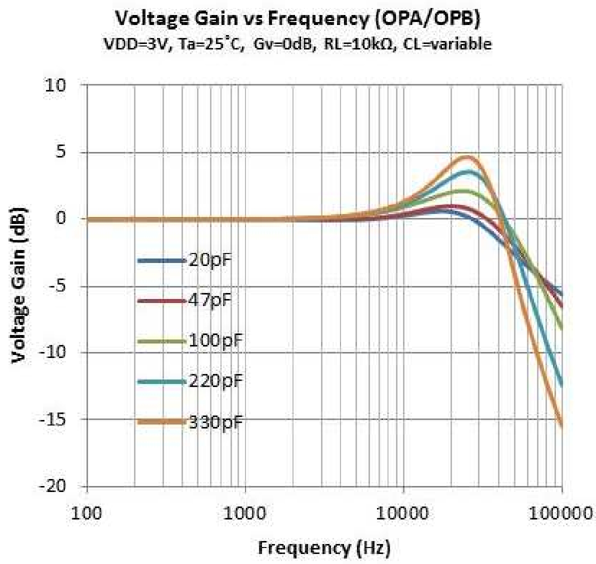

Input Offset Voltage vs
Common-Mode Input Voltage (OPA/OPB)
VDD=VREFA+=VREFIN=3V
-40°C
25°C
85°C
Input Offset Voltage Voltage (mV)
Common-Mode Input Voltage (V)


Equivalent Input Noise Voltage vs Frequency
(OPA/OPB)
VDD=3V, RF=10kΩ, RG=100Ω, Ta=25°C
Input Offset Voltage Voltage (nV/√Hz)
Frequnency (Hz)

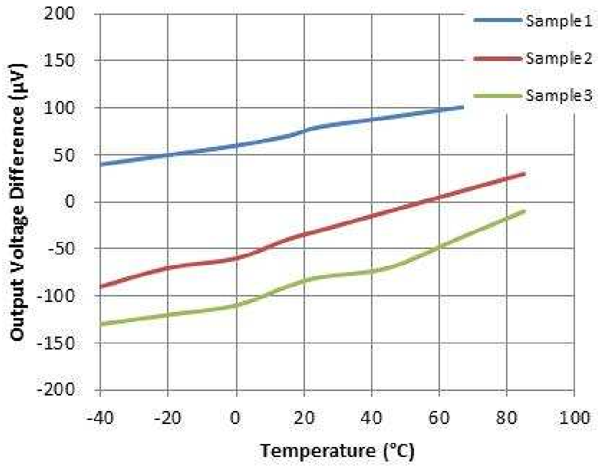

Pulse Response Rise edge (OPA/OPB)
VDD=3V, RL=10kΩ, GV=0dB, Vin=0→2V, Ta=25°C
Output Voltage (V)
Time (ms)


Pulse Response Fall edge (OPA/OPB)
VDD=3V, RL=10kΩ, GV=0dB, Vin=2→0V, Ta=25°C
Output Voltage (V)
Time (ms)

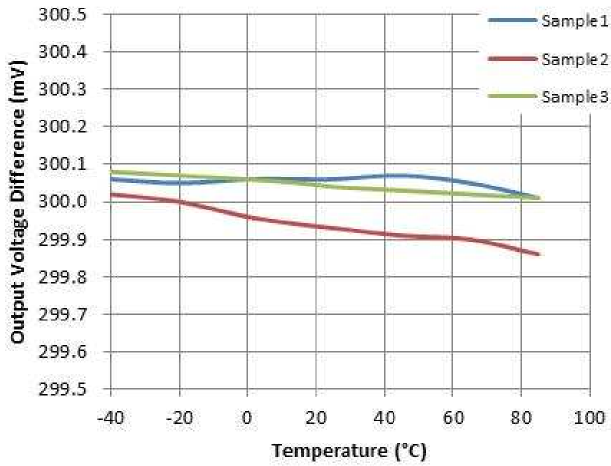

Voltage Gain vs Frequency (OPA/OPB)
VDD=3V, Ta=25°C, Gv=40dB, RL=10kΩ, CL=20pF
Gain
Phase
Voltage Gain (dB)
Frequency (Hz)


Voltage Gain vs Frequency (OPA/OPB)
VDD=3V, Ta=25°C, Gv=0dB, RL=10kΩ, CL=variable
20pF
47pF
100pF
220pF
330pF
Voltage Gain (dB)
Frequency (Hz)

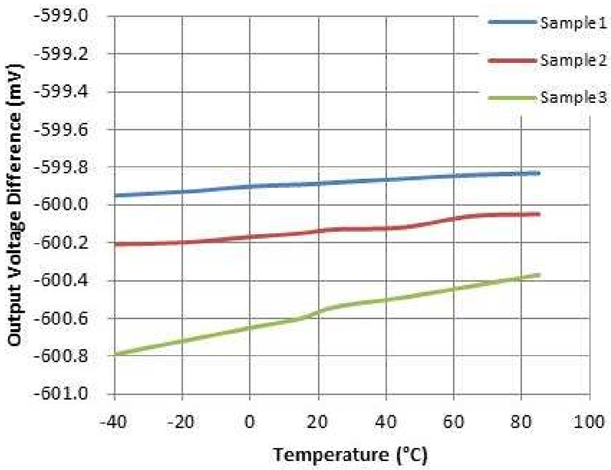
BIAS Voltage Diffrence vs Temperature
(OPA-OPB) OPA_Bias = OPB_Bias = 1V
VDD=VREFA+=VREFIN=3V, Buffer Output



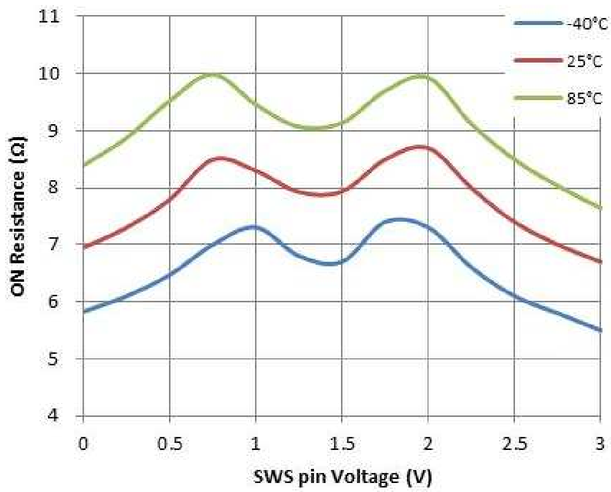
BIAS Voltage Diffrence vs Temperature
(OPA-OPB) OPA_Bias =1V, OPB_Bias = 0.7V
VDD=VREFA+=VREFIN=3V, Buffer Output



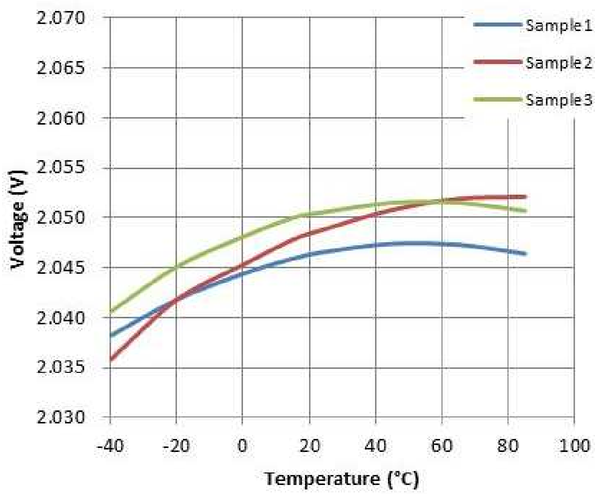
BIAS Voltage Diffrence vs Temperature
(OPA-OPB) OPA_Bias =1V, OPB_Bias = 1.6V
VDD=VREFA+=VREFIN=3V, Buffer Output



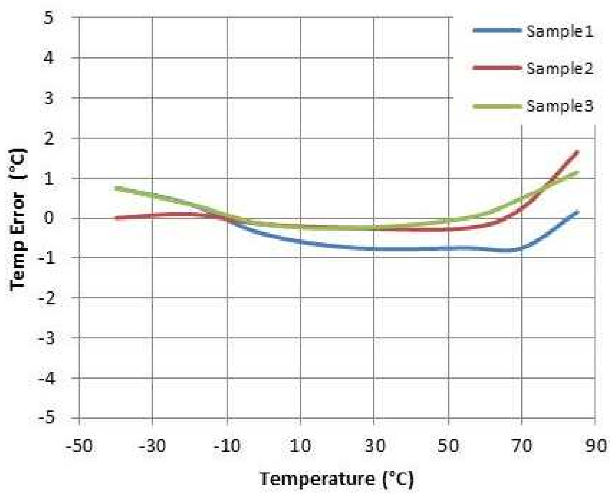
ON Resistance vs SWS pin Voltage (ANASW)
VDD=3V, ANASW="1", IDS=-10mA

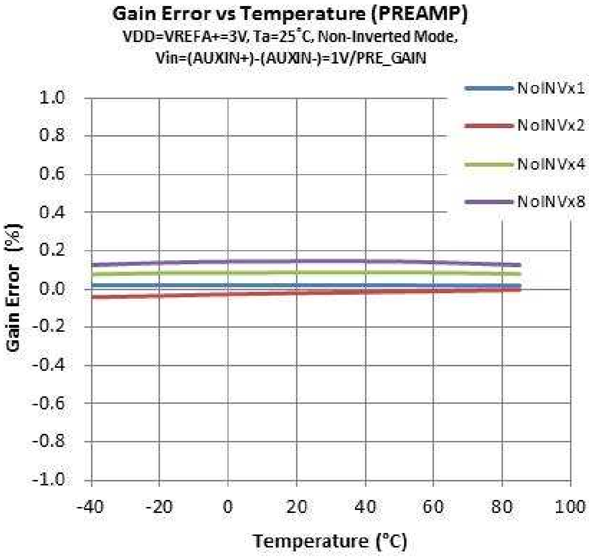


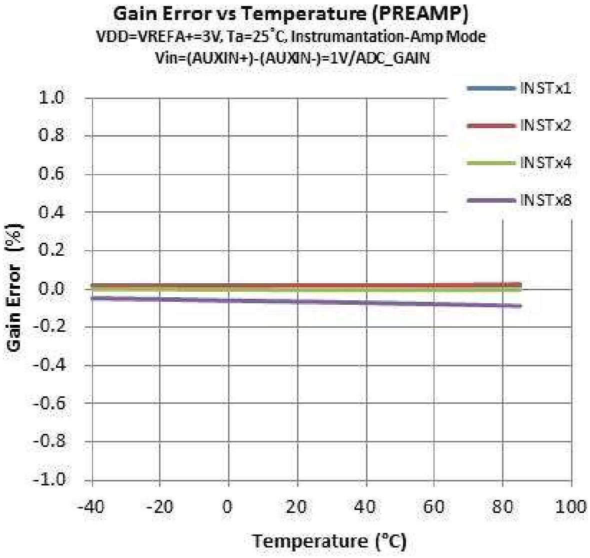
Voltage vs Temperature (INTVREF:2.048V)
VDD=3V

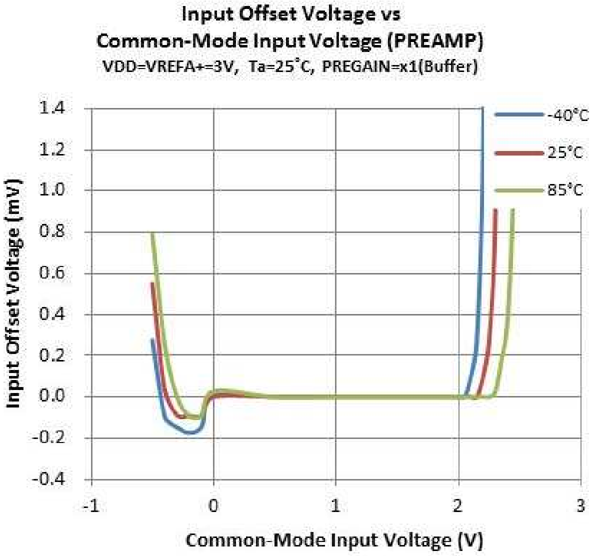


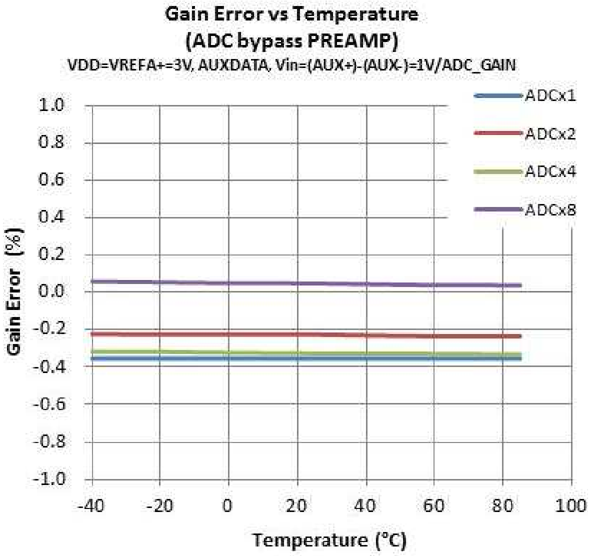
Temp Error vs Temperature (TEMP SENSOR)
VDD=VREFA+=VREFIN=3V,

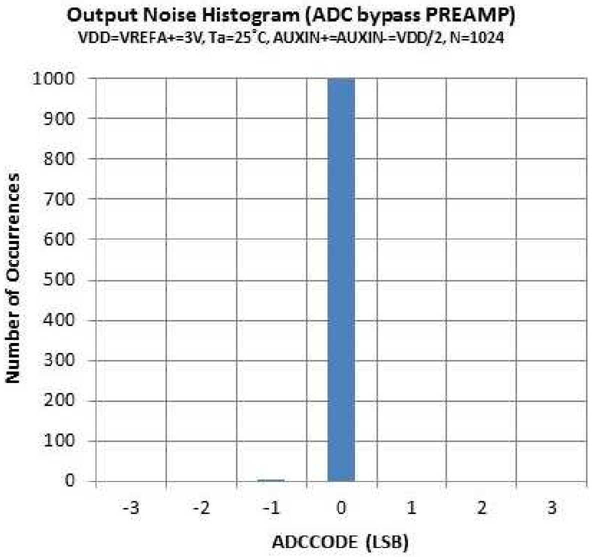


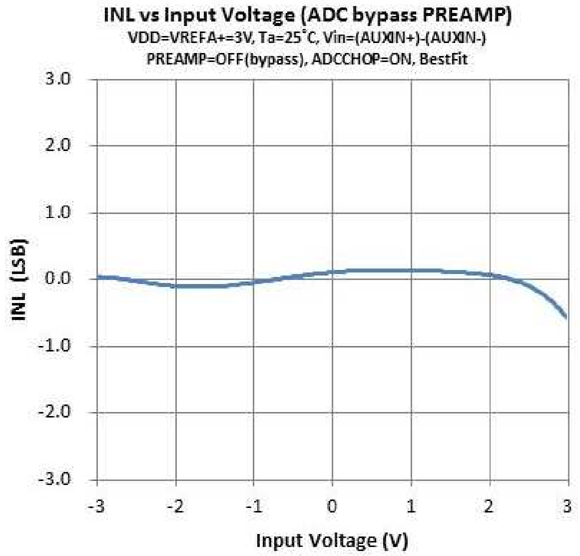

Gain Error vs Temperature (PREAMP)
VDD=VREFA+=3V, Ta=25˚C, Non-Inverted Mode,
Vin=(AUXIN+)-(AUXIN-)=1V/PRE_GAIN
NoINVx1
NoINVx2
NoINVx4
NoINVx8
Gain Error (%)
Temperature (°C)


Gain Error vs Temperature (PREAMP)
VDD=VREFA+=3V, Ta=25˚C, Instrumantation-Amp Mode
Vin=(AUXIN+)-(AUXIN-)=1V/ADC_GAIN
INSTx1
INSTx2
INSTx4
INSTx8
Gain Error (%)
Temperature (°C)


Input Offset Voltage vs
Common-Mode Input Voltage (PREAMP)
VDD=VREFA+=3V, Ta=25˚C, PREGAIN=x1(Buffer)
-40°C
25°C
85°C
Input Offset Voltage (mV)
Common-Mode Input Voltage (V)


Gain Error vs Temperature
(ADC bypass PREAMP)
VDD=VREFA+=3V, AUXDATA, Vin=(AUX+)-(AUX-)=1V/ADC_GAIN
ADCx1
ADCx2
ADCx4
ADCx8
Gain Error (%)
Temperature (°C)


Output Noise Histogram (ADC bypass PREAMP)
VDD=VREFA+=3V, Ta=25˚C, AUXIN+=AUXIN-=VDD/2, N=1024
Number of Occurrences
ADCCODE (LSB)


INL vs Input Voltage (ADC bypass PREAMP)
VDD=VREFA+=3V, Ta=25˚C, Vin=(AUXIN+)-(AUXIN-)
PREAMP=OFF(bypass), ADCCHOP=ON, BestFit
INL (LSB)
Input Voltage (V)

■APPLICATION NOTE / GLOSSARY

NJU9101 consists of the following circuit block.

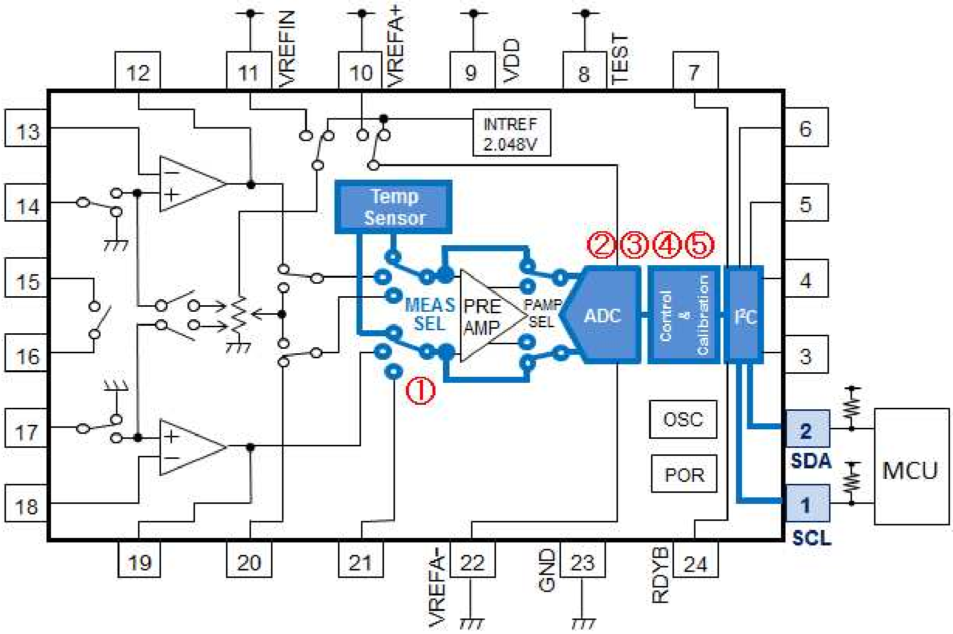
CIRCUIT BLOCK NAME	SYMBOL
2 Low Current Operational Amplifier	"OPA"、"OPB"
Bias Level Setting Register	"BIASRES"
10Ω Analog Switch	"ANASW"
Variable Gain Pre-Amplifier	"PREAMP"
Temperature Sensor	"TempSensor"
Internal Reference	"INTVREF (2.048V)"
16-Bit sigma delta ADC	"16-Bit ADC"
Digital Control & Calibration	"Control&Calibration"
I^2C Bus Compatible Control	"I^2C"

NJU9101 is suitable for many kinds of low power analog signal applications by using these circuit blocks.

1. Signal channel selection for Measurement

1.1 Temperature Sensor Measurement

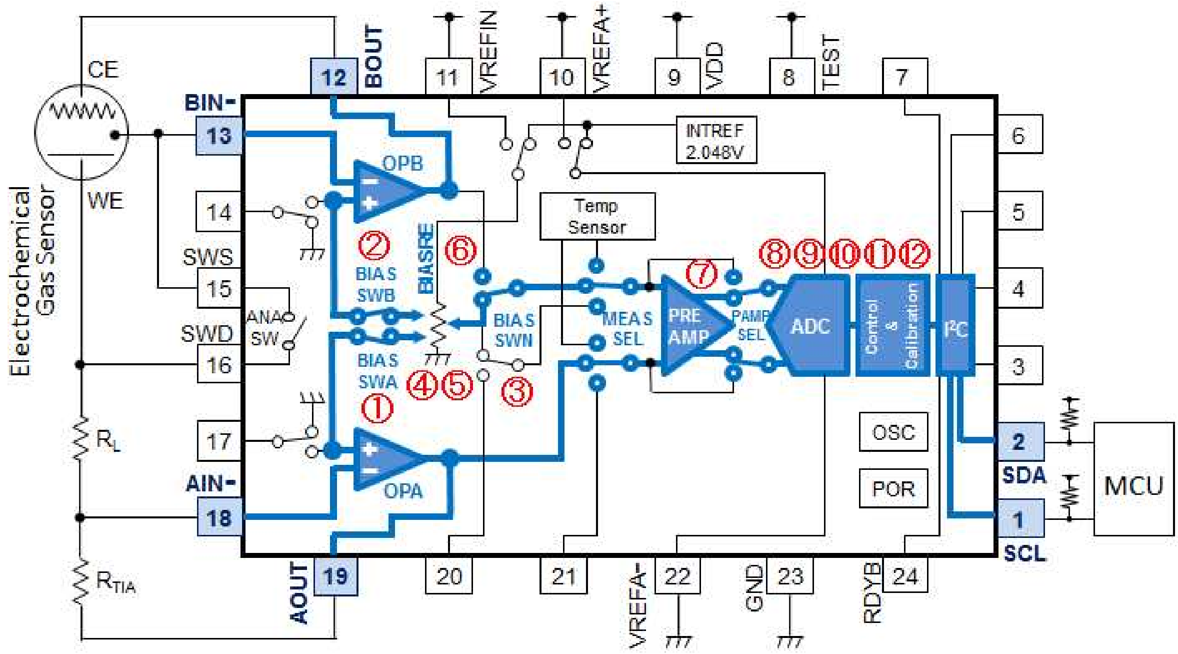
Write below code to measure Temperature.



No.	CONTENS	REGISTER ADDRESS	REGISTER NAME	BIT NAME	BIT	VALUE
1	Select Temperature Input Mode	0x00	CTRL	MEAS_SEL	[2:1]	00
2	Select ADC Conversion Mode (Exp. Single Conversion)			MEAS_SC	[0]	0
3	Start AD Conversion			MEAS	[3]	1
4	Check completion of the AD conversion ("MEAS" bit = "0")					-
5	Acquire AD conversion data. (TMPDATA)	0x06 0x07	TMPDATA0 TMPDATA1	TMPDATA	[9:0]	-

1.2 System Example 1 (Potentiostat Measurement)

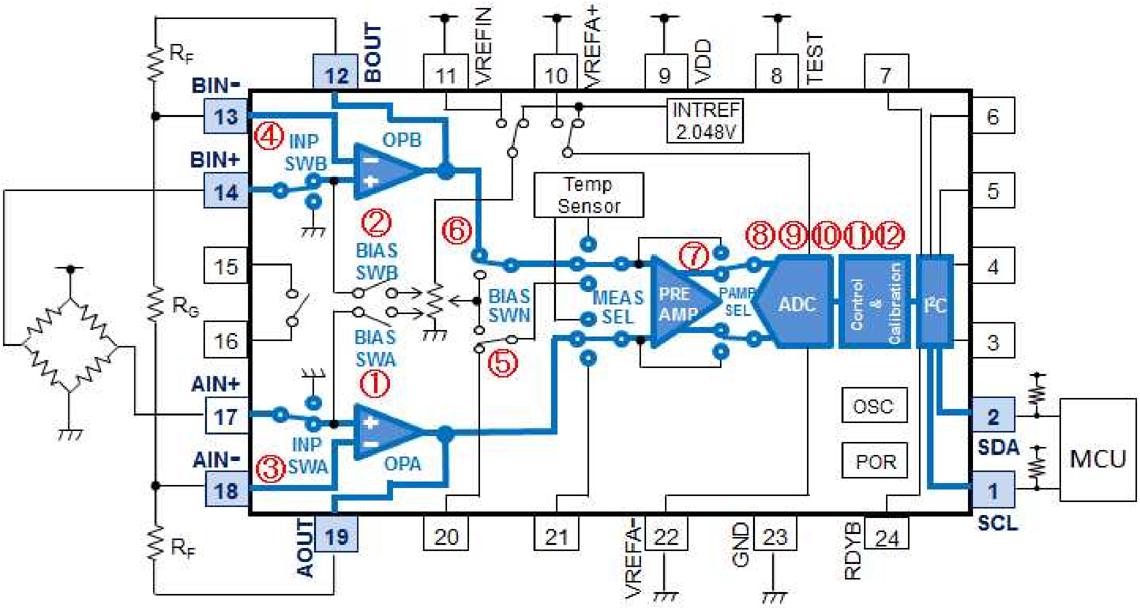
Write below code to constitute “potentiostat” and “trans-impedance-amplifier”



No.	CONTENS	REGISTER ADDRESS	REGISTER NAME	BIT NAME	BIT	VALUE
1	Connect the switch “BIASRES” and “OPA”	0x0F	BLKCONN0	BIASSWA	[5]	1
2	Connect the switch “BIASRES” and “OPB”			BIASSWB	[4]	1
3	Select output of BIASRES	0x11	BLKCONN2	BIASSWN	[3]	1
4	Bias level for “trance-impedance-amplifier” (GND to 1.7V)	0x10	BLKCONN1	OPA_BIAS	[7:5]	any
5	Bias level for “potentiostat” (GND to 1.75V)			OPB_BIAS	[4:0]	
6	Powered on BIASRES, OPA, OPB, OSC	0x12	BLKCTRL	BLKCTRL	[7:0]	0xF0
7	Enable PREAMP	0x11	BLKCONN2	PAMPSEL	[2]	1
8	Select Amp Input Mode	0x00	CTRL	MEAS_SEL	[2:1]	01
9	Set Measurement Mode for ADC (ex.: Single conversion)			MEAS_SC	[0]	0
10	Start measurement			MEAS	[3]	1
11	Check completion of the AD conversion (“MEAS” bit = “0”)					-
12	Acquire AD conversion data (AMPDATA)	0x02 0x03	AMPDATA0 AMPDATA1	AMPDATA	[15:0]	-

1.3 System Example 2 (Differential Input)

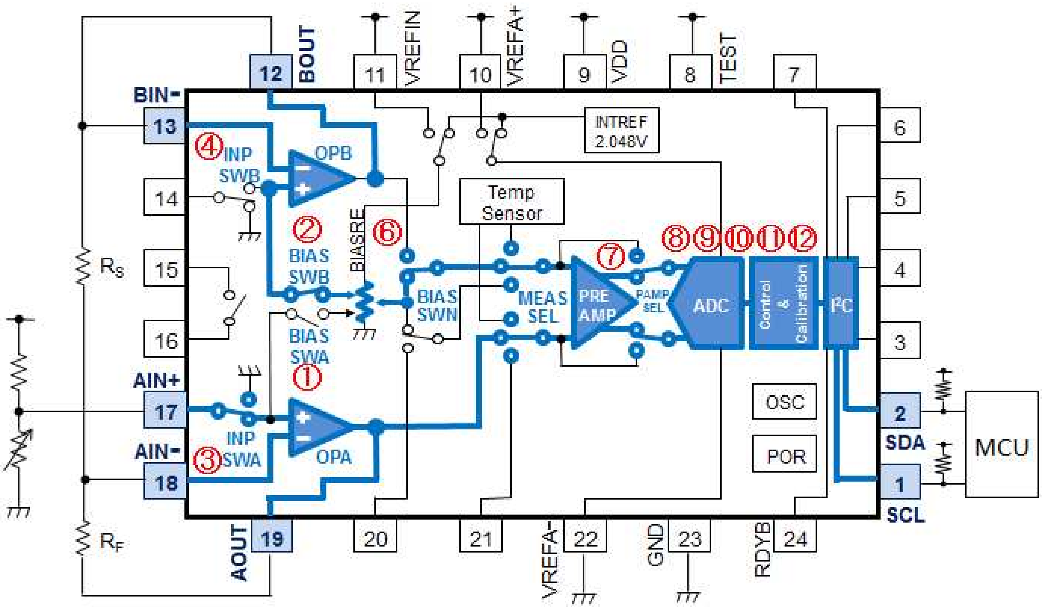
Write below code to constitute “Differential Amplifier Input” by using OPA/OPB.



No.	CONTENTS	REGISTER ADDRESS	REGISTER NAME	BIT NAME	BIT	VALUE
1	Open OPA input switch	0x0F	BLKCONN0	BIASSWA	[5]	0
2	Open OPB input switch			BIASSWB	[4]	0
3	Select OPA sensor signal input	0x11	BLKCONN2	INPSWA	[6]	1
4	Select OPB sensor signal input			INPSWB	[5]	1
5	Select OPB output			BIASSWN	[3]	0
6	Powered on OPA, OPB, OSC	0x12	BLKCTRL	BLKCTRL	[7:0]	0x70
7	Enable PREAMP	0x11	BLKCONN2	PAMPSEL	[2]	1
8	Select Amp Input Mode	0x00	CTRL	MEAS_SEL	[2:1]	01
9	Set Measurement Mode for ADC (ex.: Single conversion)			MEAS_SC	[0]	0
10	Start measurement			MEAS	[3]	1
11	Check completion of the AD conversion (“MEAS” bit = “0”)					-
12	Acquire AD conversion data (AMPDATA)	0x02 0x03	AMPDATA0 AMPDATA1	AMPDATA	[15:0]	-

1.4 System Example 3 (Single Input (Non-Inverting))

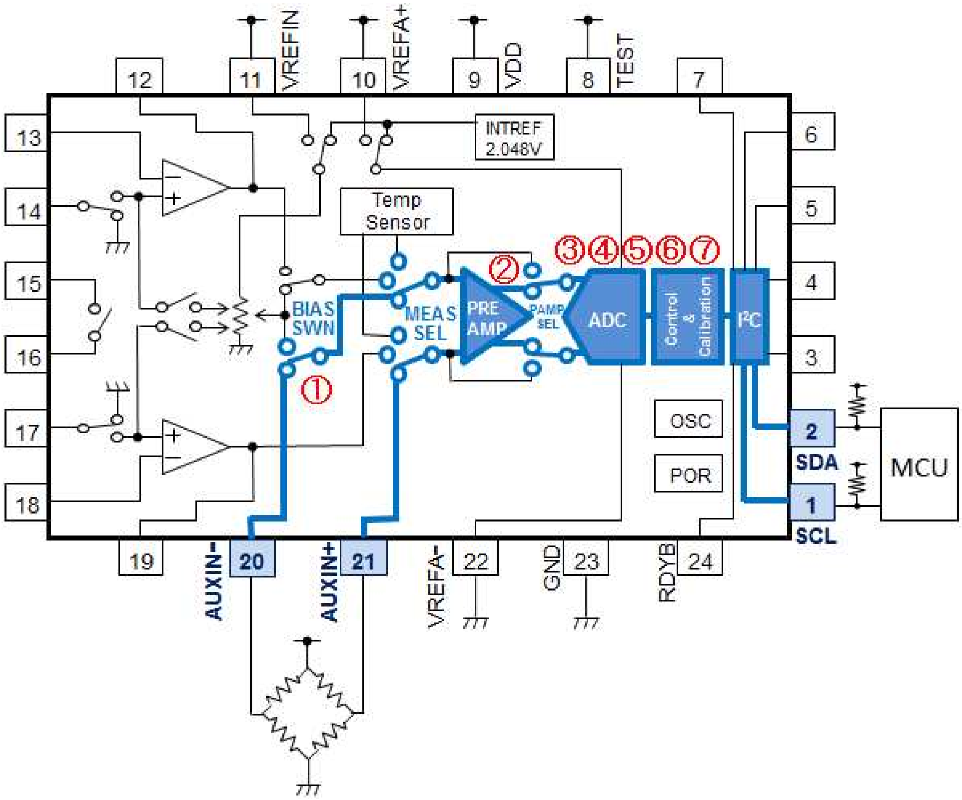
Write below code to constitute “Single Amplifier Input” by using OPA/OPB.



No.	CONTENTS	REGISTER ADDRESS	REGISTER NAME	BIT NAME	BIT	VALUE
1	Open OPA input switch	0x0F	BLKCONN0	BIASSWA	[5]	0
2	Close OPB input switch			BIASSWB	[4]	1
3	Select OPA sensor signal input	0x11	BLKCONN2	INPSWA	[6]	1
4	Connect OPB positive input to GND			INPSWB	[5]	0
5	Select BIASRES output			BIASSWN	[3]	1
6	Powered on BIASRES, OPA, OPB, OSC	0x12	BLKCTRL	BLKCTRL	[7:0]	0xF0
7	Enable PREAMP	0x11	BLKCONN2	PAMPSEL	[2]	1
8	Select Amp Input Mode	0x00	CTRL	MEAS_SEL	[2:1]	01
9	Set Measurement Mode for ADC (ex.: Single conversion)			MEAS_SC	[0]	0
10	Start measurement			MEAS	[3]	1
11	Check completion of the AD conversion (“MEAS” bit = “0”)					-
12	Acquire AD conversion data (AMPDATA)	0x02 0x03	AMPDATA0 AMPDATA1	AMPDATA	[15:0]	-

1.5 Auxiliary (external Input) Measurement

Write below code to constitute “Differential Amplifier Input” by using PREAMP.



No.	CONTENTS	REGISTER ADDRESS	REGISTER NAME	BIT NAME	BIT	VALUE
1	Select AUXIN input	0x11	BLKCONN2	BIASSWN	[3]	1
2	Enable PREAMP			PAMPSEL	[2]	1
3	Select Auxiliary input mode	0x00	CTRL	MEAS_SEL	[2:1]	10
4	Set Measurement Mode for ADC (ex.: Single conversion)			MEAS_SC	[0]	0
5	Start measurement			MEAS	[3]	1
6	Check completion of the AD conversion (“MEAS” bit = “0”)					-
7	Acquire AD conversion data (AUXDATA)	0x04 0x05	AUXDATA0 AUXDATA1	AUXDATA	[15:0]	-

2. Potentiostat & Ttans-impedance-amp circuit block

Potentiostat consists of "OPB", "Variable Bias Resister (BIASRES)". "Reference Electrode (RE)" bias voltage is set by "Variable Bias Resister (BIASRES)" using command in "OPB_BIAS" bits. "Trans-impedance-amp(OPA)" connected to the "Working Electrode (WE)" is used to provide an output voltage that is proportional to the cell current. Bias Voltage of OPA is also set by BIASRES using command in "OPA_BIAS" bits.

OPA gain is set by external resister (R_{TIA}). And, please connect R_L between WE and negative input of OPA.

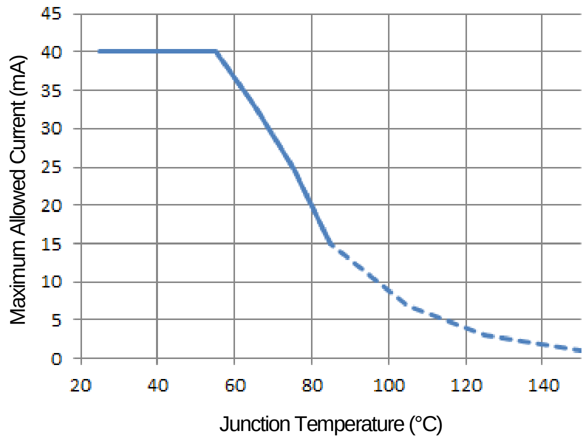
3. Shorting FET Function

NJU9101 has Internal Analog Switch (ANASW). This switch can connect between WE and RE of Chemical Sensor Cell. This Switch is switched on/off by "ANASW" bit.

In discrete system, depletion FET (ex. J177) is usually used as shorting FET. But, this switch "ANASW" in NJU9101 is enhancement FET (not depletion FET).

Therefore, this switch "ANASW" is effective only during powered on. This means that "ANASW" can't turn on during powered off.

ON resistance of this switch "ANASW" is **10Ω typ**. This is to get a quick stabilized time after powered on.



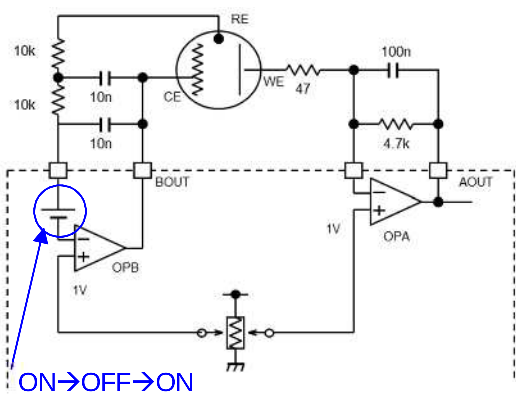
4. Regarding Sensor Diagnostic Function

NJU9101 has Sensor Diagnostic Function using "SENSCK" bits.

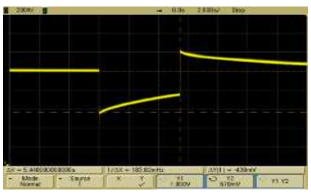
When "SENSCK" mode turns ON ("1"), Offset Voltage of "OPA" changes around ±5mV. To switch "SENSCK" bits to "0"→"1"→"0", you can get as below waveforms.

* This is one of way to Sensor Diagnostic that we propose only.

Sensor Condition	AOUT Voltage		BOUT Condition
	SENSCK OFF	SENSCK ON	
ALL connected	1V	0.6V	Waveform1
WE opened	1V	1V	Waveform2
CE opened	1V	1V	Waveform2
RE opened	0V	0V	Waveform3

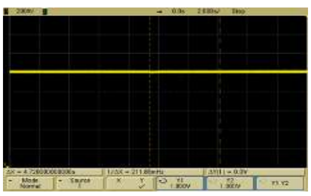


Waveform1



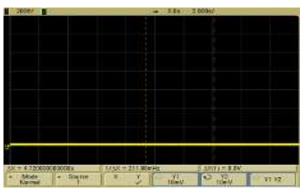
All connected

Waveform2



WE or CE opened

Waveform3



RE opened

5. Variable Bias Register (BIASRES)

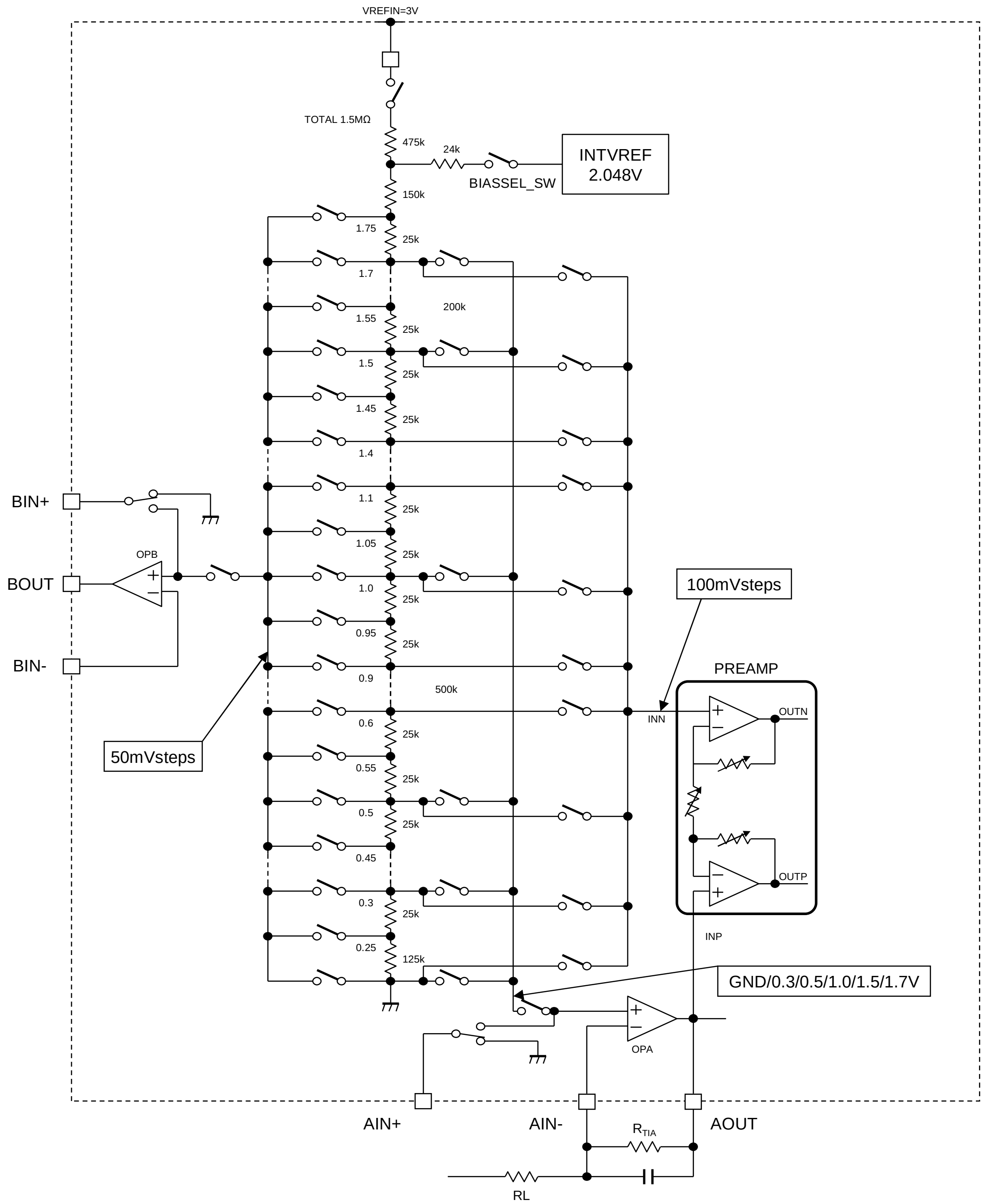
"Variable Bias Resister (BIASRES)" for "OPA", "OPB", and "PREAMP" are shown in below.

The Bias Voltage for these amplifiers are given by resister ladder ratio (total resister = 1.5MΩ). These resister ladder ratio are set by "OPA_BIAS", "OPB_BIAS", "PRE_BIAS" registers. Setting Name of these register (ex. 0.5V @ VREFIN=3V) is in VREFIN=3V condition.

If VREFIN is not 3V (ex. VREFIN=2.5V), the selected Voltage is shifted as follow.

If register setting is "1.5V @ VREFIN=3V" → Actual Voltage is 1.5V * (2.5V/3.0V) = 1.25V

And, when "BIASSEL = 0", BIASSEL_SW is turned on and fixed voltage "INTVREF (2.048V)" is given to the resister ladder shown in figure below.

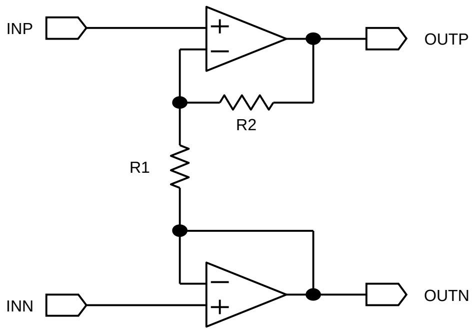


6. PREAMP Gain Calculation

"Non-Inverted Amplifier" or "Instrumentation Amplifier" is selected by "PREMODE" bit.
"Pre-Amplifier-Gain" is selected by "PRE_GAIN" bits.

Input Voltage range of INP&INM is "0V" to "VDD-1V".
Output Voltage range of OUTP&OUTN is "0.05V" to "VDD-0.05V".
* Please design not to exceed Input & Output Voltage range.

6.1. PREMODE = 0 (Non-Inverted Amplifier)



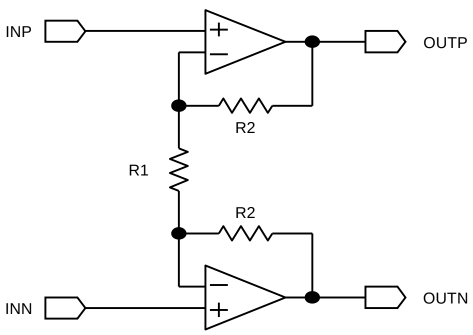
$$V(OUTP) = V(INP) + \frac{R2}{R1} \times V(INP - INN)$$

$$V(OUTN) = V(INN)$$

$$GAIN = \frac{V(OUTP - OUTN)}{V(INP - INN)} = 1 + \frac{R2}{R1}$$

Gain	PRE_GAIN	R1	R2
1 V/V	00	320kΩ	0Ω
2 V/V	01	160kΩ	160kΩ
4 V/V	10	80kΩ	240kΩ
8 V/V	11	40kΩ	280kΩ

6.2. PREMODE = 1 (Instrumentation Amplifier)



$$V(OUTP) = V(INP) + \frac{R2}{R1} \times V(INP - INN)$$

$$V(OUTN) = V(INN) + \frac{R2}{R1} \times V(INN - INP)$$

$$GAIN = \frac{V(OUTP - OUTN)}{V(INP - INN)} = 1 + 2 \times \frac{R2}{R1}$$

Gain	PRE_GAIN	R1	R2
1 V/V	00	320kΩ	0Ω
2 V/V	01	160kΩ	80kΩ
4 V/V	10	80kΩ	120kΩ
8 V/V	11	40kΩ	140kΩ

7. Low Power Management

NJU9101 is intended for use in portable devices, so the power consumption is as low as possible in order to ensure a long battery life. Following usage assumption of NJU9101 is in a portable gas detector. And its power consumption is summarized in below. The total power consumption for NJU9101 is below @3V average over time, this excludes any current drawn from any pin, please consider another device's consumption.

< Condition >

- The system is used about 8 hours a day, and 16 hours a day it is in Standby mode.
- Basically, Only "OPB" and "BIASRES" block are turned On in Standby mode.
- Potentiostat Measurement is once per second.
- Aux Data Measurement is one per minutes.
- Temperature Measurement is one per minutes.
- ADC conversion time uses approximately 16.6ms. (OSR="01", REJ="10", ADCCHOP="1")

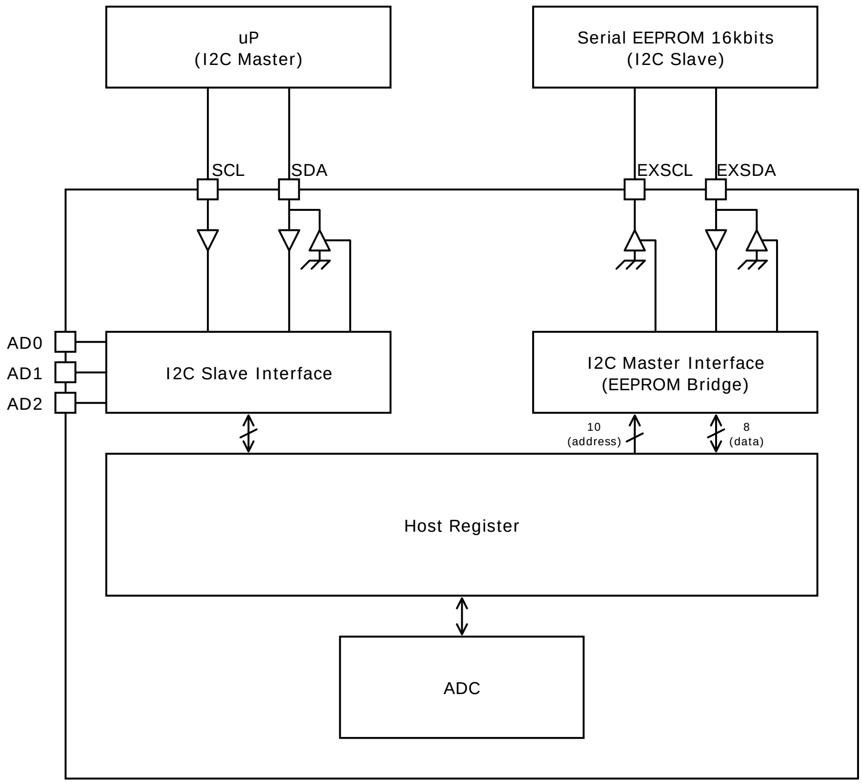
	Standby	3-Lead Potentiostat	Potentiostat Measurement	Aux Data Measurement	Temperature Measurement	Total Current Consumption
Current Consumption	0.5µA	10.5µA	215.5µA	160.5µA	250.5µA	
Time On a Day	16 (h)	8 (h)	480 (s)	8 (s)	8 (s)	
	66.6%	33.3%	0.556%	0.009%	0.009%	
Average Current	0.33µA	3.5µA	1.2µA	0.01µA	0.02µA	**5.01µA**
ANASW	ON	OFF	OFF	OFF	OFF	
BIASRES	OFF	ON	ON	ON	ON	
OPA	OFF	ON	ON	ON	ON	
OPB	OFF	ON	ON	ON	ON	
PREAMP	OFF	OFF	ON	OFF	ON	
ADC	OFF	OFF	ON	ON	ON	
Temp. sensor	OFF	OFF	OFF	OFF	ON	
I^2C & Logic	ON	ON	ON	ON	ON	

8. I²C-BUS Interface

NJU9101 has 2 types of I²C bus, one bus communicates to host device such as MCU, the other bus communicates to external EEPROM which is to retain the IC configurations, calibration parameters, .etc. These 2 types of I²C bus operate independently. NJU9101 operates for host interface as I²C slave device, and operates for EEPROM interface as I²C Master Device.

One I²C-bus which connects to host device is SCL/SDA, and the other I²C-bus which connects to external EEPROM is EXSCL/EXSDA.

Communicate	I²C bus	I/O	Master / Slave
Host Device (e.g.: MPU)	SCL	Input	NJU9101:Slave
	SDA	Input / Open-Drain Output	
External EEPROM	EXSCL	Open-Drain Output	NJU9101:Master
	EXSDA	Input / Open-Drain Output	



8.1. I²C Slave Interface

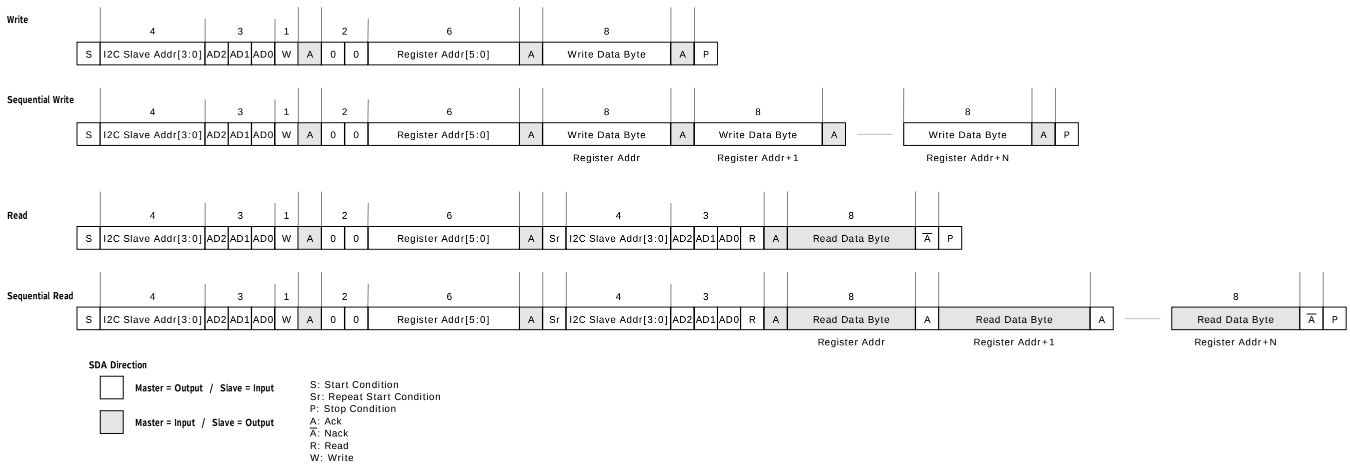
This interface is used for the Host that accesses to registers in NJU9101. NJU9101 is a I²C Slave device for the host MCU. The operation of which conversion trigger, conversion data reading, access external EEPROM, .etc. are executed through reading and writing of registers in NJU9101. Registers in NJU9101 are register address 0x00 to 0x3F and each address has 8 bits width register.

● I²C Protocol

7bit-I^{2}C Slave address consists of a fixed four-bit ‘0x9(b1001)’ and chip address pin ‘AD2’, ‘AD1’, ‘AD1’.

In case of write operation, transmit the writing data in following,
‘Slave address’ + ‘Write bit (0)’ + ‘Write Register address’ + ‘Write data’.
When more than 2 bites of write data are transmitted, register address are increment automatically, and write the date into corresponding registers. When register address is over 0x3F, return to address 0x00 and lap around.

In case of read operation, transmit the data in following,
‘Slave address’ + ‘Write bit (0)’ + ‘Read Register address’ and then transmit ‘repeat start’ command.
When more than 2 bites of read data are read, register address are increment automatically, and read the date into corresponding address. When register address is over 0x3F, return to address 0x00 and lap around.



● I²C external EEPROM Interface

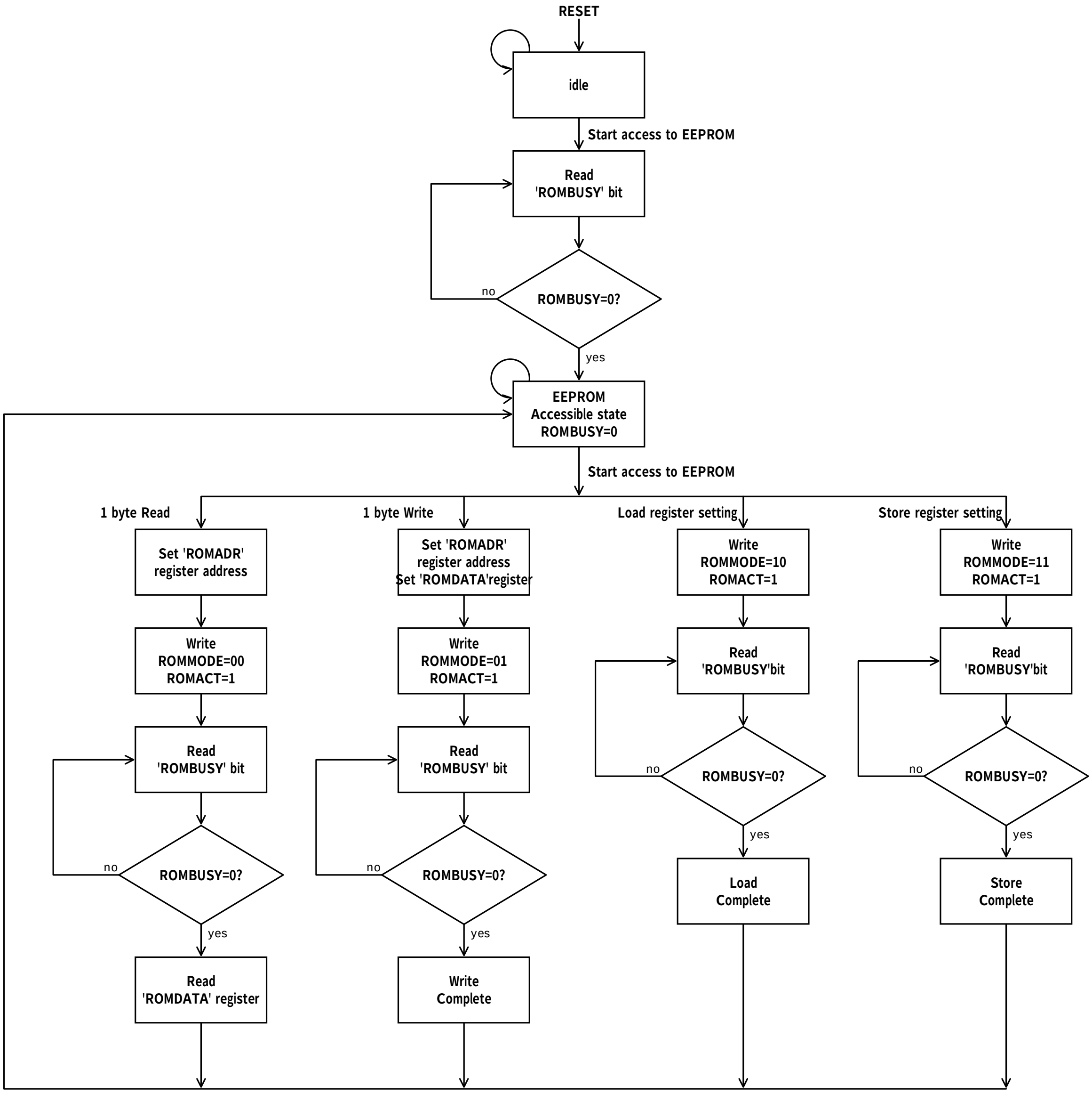
I^{2}C external EEPROM of 16k-Bit (2kByte) can be connected as a external storage device for NJU9101. ‘Microchip 24LC16B’ is used as a standard External EEPROM. Other I^{2}C Serial EEPROM with communication compatible can be used. Some areas in external EEPROM are used as preset area for configuration data of NJU9101. The remaining areas in external EEPROM can be used for any uses.

NJU9101 supports 4-operations for external EEPROM from host-interface (MCU).
· Read data from arbitrary address area in external EEPROM.
· Write data to arbitrary address area in external EEPROM.
· Load the all data from external EEPROM to host register (MCU).
· Store register data in host register (MCU) to external EEPROM.

See also, “EVERY REGISTER DESCRIPTION : ROMCTRL” to control the external EEPROM.

● **External EEPROM operating flow & External EEPROM I^2C bus timing**

Flow chart of access to external EEPROM is shown in below. When access to external EEPROM, system clock has to be operating and 'ROMBUSY' bit has to be '0'. And it can also access to external EEPROM under ADC conversion (Except for reading the initial register value just after reset release.).



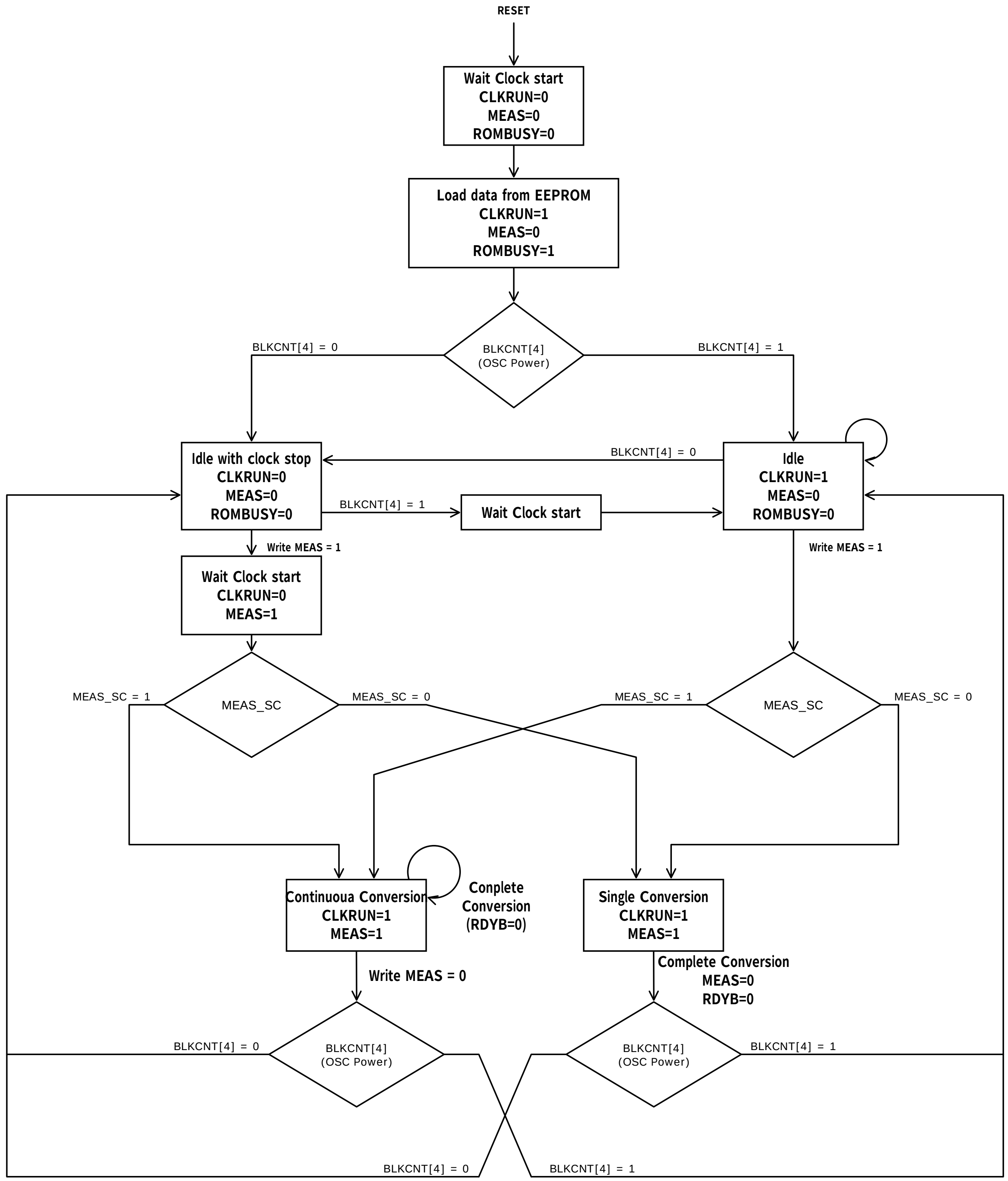
External EEPROM requires about 5ms of write time internally after write operation. During this period, NJU9101 cannot read/write from/to external EEPROM and external EEPROM returns 'NACK' for address byte. When NJU9101 starts to access to external EEPROM, NJU9101 does polling until receive 'ACK', and wait for completion of writing time in external EEPROM.

When NJU9101 is not connected with external EEPROM, address byte of NJU9101 always receives 'NACK'. Therefore, External EEPROM Control block in NJU9101 cannot stop polling. In such case, stop accessing to external EEPROM quickly by writing "1" to "ROMSTOP" bit, or it can break out of the polling by generating communication error ("ROMERR"="1") with fixed "0" for EXSDA terminal.

I^2C-bus of external EEPROM uses 3-system clock every 1 bit transfer, therefore maximum translate is fin/3[bps].

● ΔΣ ADC control

ΔΣ ADC conversion flow is shown in below.



● Start-Up

After power-on reset or release I^2C reset, start internal clock (OSC) and load data from external EEPROM to NJU9101's register. During loading, 'ROMBUSY' shows '1'. After finish loading to NJU9101's register, NJU9101 becomes idle state or idle state with clock stop which are following BLKCNT [4] setting.

● Idle State

"Idle state" means in the state which is not conversion state. In the idle state, 'BLKCNT [4](OSC power down)'bit changes the powered-on/off of system clock. During stopping the system clock, NJU9101 is idle state with clock stop, and it cannot write the data of NJU9101 register except 'CTRL' and 'BLKCNT' register. This means that **"Please write 'BLKCNT[4]'='1', when change the data of NJU9101 register".**

● Conversion

When write 'MEAS' bit = '1', conversion starts with following NJU9101 register setting.

First, Wake up time of modulator T_{wu} is required after conversion started.

$T_{WU} = 20 / f_{mod}$ [sec]

T_{adc} is the time which is divided 'decimation rate (set in OSR / REJ bit) by f_{mod} (normal modulation clock frequency of ΔΣ modulator ≈ 153.6 kHz).

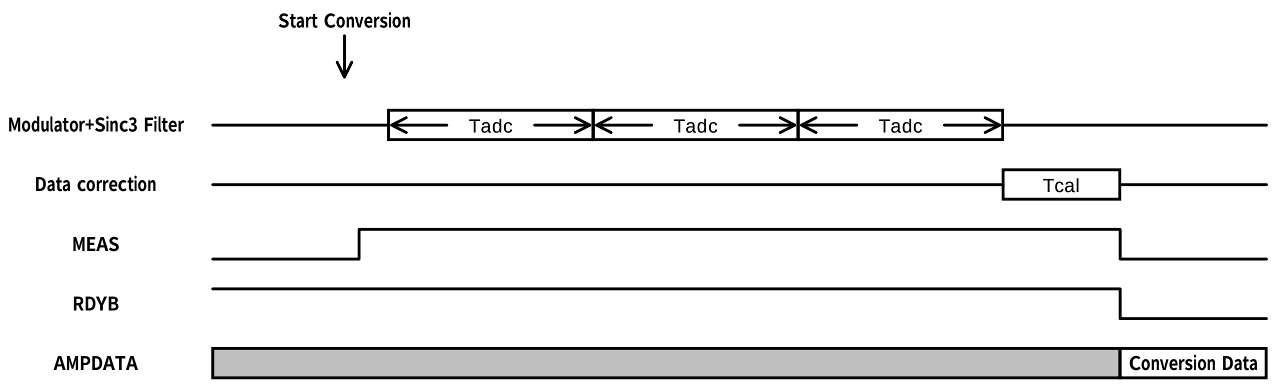
T_{adc} = Decimation rate / f_{mod} [sec]

Standard timing of ADC conversion is defined as T_{adc}.
And, after completion of conversion, it requires around 70 cycle of system clock (70 / f_{OSC}) to do data corrective calculation.
This calculation time is defined as T_{cal}.

$T_{cal} = 70 / f_{OSC} \approx 230\mu$ [sec]

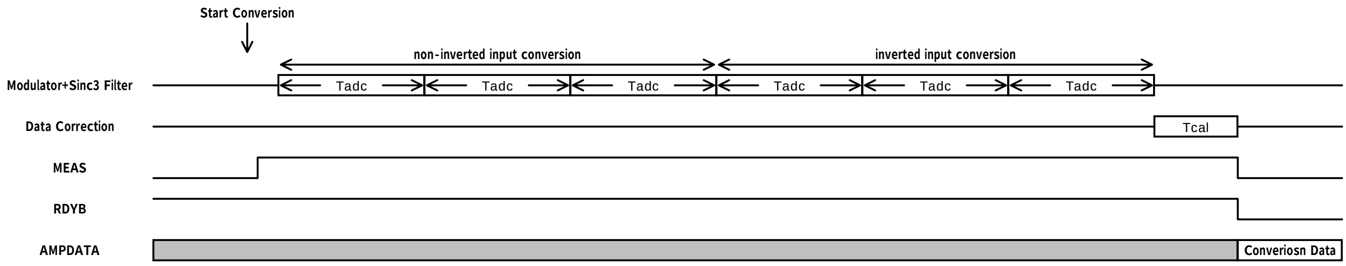
● Single Conversion

Conversion time of 'Single conversion' is ' T_{wu} + 3 * T_{adc} + 'T_{cal}'. The settling time of ADC requires ' 3 * T_{adc}'.
After complete data correction, data register is updated, and RDYB bit is asserted.



- **Single Conversion + Chopping Operation**

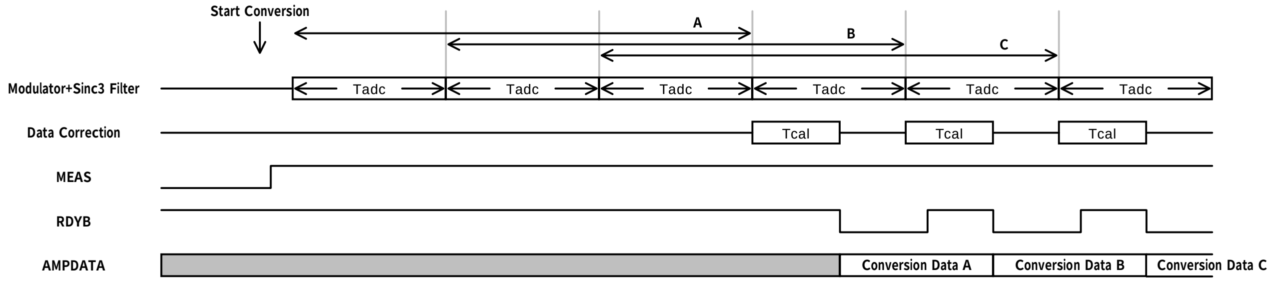
Conversion time of ‘Single Conversion + Chopping Operation’ is ‘ $T_{wu} + 6 * T_{adc} + T_{cal}$ ’. The settling time of ADC requires ‘ $6 * T_{adc}$ ’. After complete data correction, data register is updated, and ‘RDYB’ bit is asserted. And then, ‘MEAS’ bit turns to ‘0’, become idle state again. Chopping operation can cancel offset voltage into ADC by swapping differential positive - negative input.



- **Continuous Conversion**

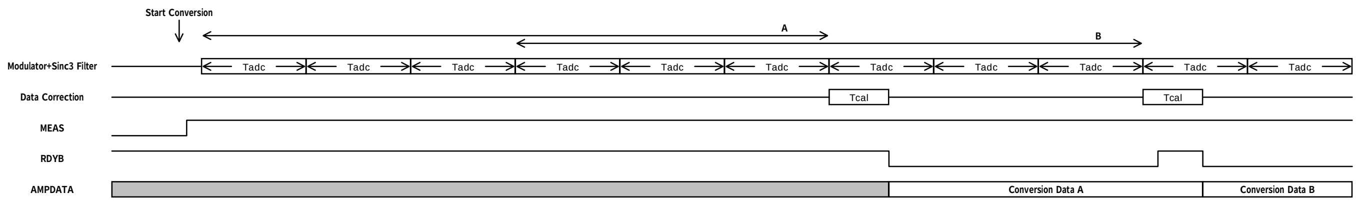
The first conversion time of ‘Continuous Conversion’ is ‘ $T_{wu} + 3 * T_{adc} + T_{cal}$ ’. The settling time of ADC requires T_{adc}.

After complete the first conversion data correction, data register is updated, and RDYB bit is asserted. And after that, data register is updated and RDYB bit is asserted every T_{adc}. Conversion rate after the first conversion is 1/Tadc [sps]. This conversion is continued until written ‘MEAS = 0’.



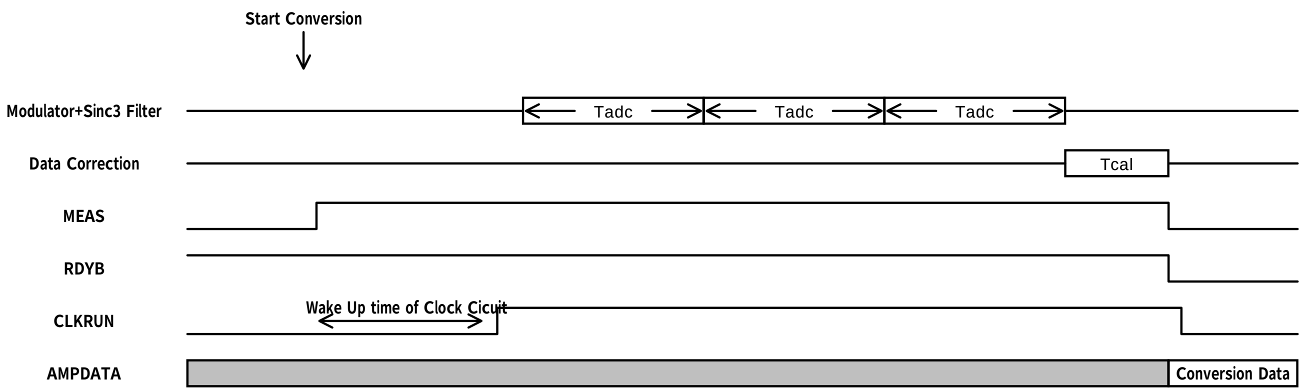
- **Continuous Conversion + Chopping Operation**

The first conversion time of ‘Continuous Conversion + Chopping Operation’ is ‘$T_{wu} + 6 * T_{adc} + T_{cal}$’. The settling time of ADC requires ‘$6 * T_{adc}$’. After complete data correction, data register is updated, and RDYB bit is asserted. And after that, data register is updated and RDYB bit is asserted every ‘$3 * T_{adc}$’. Conversion rate after the first conversion is ‘$1/(3 * T_{adc})$’ [sps]. This conversion is continued until written ‘MEAS = 0’.



● Conversion at 'Idle state with Clock Stop'

In case of 'Idle state with Clock Stop (BLKCNT[4]=0)', it is necessary an additional time (≈450us) to wake up the clock circuit after start conversion trigger. When 'Single Conversion' is set, it turns 'Idle state with Clock Stop (BLKCNT [4] = 0)' automatically after complete the conversion.



● Power-Down Control

Power down control signal of each circuit block in NJU9101 is controlled by following registers value 'MEAS', 'MEAS_SEL', 'VREFSEL', 'PAMPSEL', and 'BLKCNT[7:0]'.

BIASRES circuit block power down

Block	BLKCNT [7]	Power Condition
BIASRES	0	PWR DOWN
	1	OPERATE

OPA circuit block power down

Block	MEAS	MEAS_SEL [1:0]	BLKCNT [5]	Power Condition
OPA	0	-	0	PWR DOWN
	1	00 / 10	0	
	1	01	0	OPERATE
	-	-	1	

OPB circuit block power down

Block	MEAS	MEAS_SEL [1:0]	BLKCNT [6]	Power Condition
OPB	0	-	0	PWR DOWN
	1	00 / 10	0	
	1	01	0	OPERATE
	-	-	1	

OSC circuit block power down

Block	MEAS	BLKCNT [4]	BLKCNT [1]	Power Condition
		OSC	ADC	
OSC	0	0	0	PWR DOWN
	1	0	0	OPERATE
	-	1	-	
	-	-	1	

PREAMP circuit block power down

Block	MEAS	MEAS_SEL [1:0]	PAMPSEL	BLKCNT [3]	Power Condition
PREAMP	0	-	-	0	PWR DOWN
	1	00	-	-	OPERATE
	1	01 / 10	0	0	PWR DOWN
	1	01 / 10	1	0	OPERATE
	-	-	-	1	

2.048V INTVREF circuit block power down

Block	MEAS	MEAS_SEL [1:0]	BIASSEL	VREFSEL	BLKCNT [2]	Power Condition
INTVREF	0	-	1	-	0	PWR DOWN
	1	00	1	-	0	OPERATE
	1	01 / 10	1	0	0	
	1	01 / 10	1	1	0	PWR DOWN
	-	-	1	-	1	OPERATE
	-	-	0	-	-	

ADC circuit block power down

Block	MEAS	BLKCNT [1]	Power Condition
ADC	0	0	PWR DOWN
	1	0	OPERATE
	-	1	

Temperature Sensor circuit power down

Block	MEAS	MEAS_SEL [1:0]	BLKCNT [0]	Power Condition
Temp. Sensor	0	-	0	PWR DOWN
	1	00	0	OPERATE
	1	01 / 10	0	PWR DOWN
	-	-	1	OPERATE

● **Data Processing**

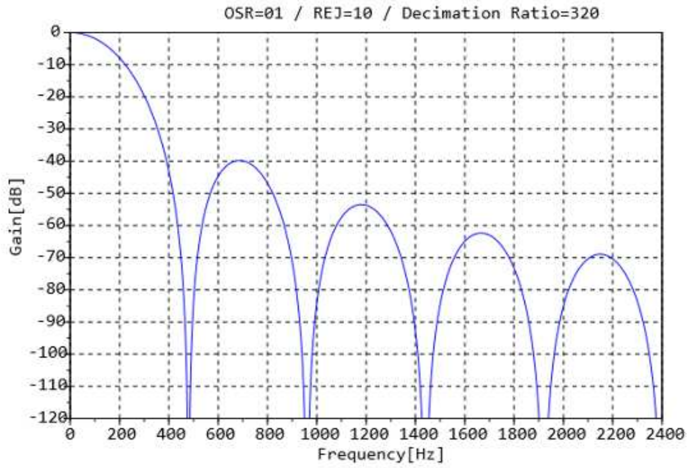
Analog Input is modulated to PDM signal by 2nd Order ΔΣ modulator. And then, this PDM signal changes to PCM signal by Sinc3 Digital Filter. Sinc3 Digital Output data is stored to AMPDATA / AUXDATA / TMPDATA register after data calibration.

● **ΔΣ Modulator**

Normal modulation clock frequency of ΔΣ (Sigma Delta) modulator (fmod) is 153.6 kHz. This frequency (fmod) is the over-sampling clock of the ADC which is divided OSC system clock (f_{OSC}) with setting of 'CLKDIV' bit. Modulated ratio of this modulator is 66.7%. When +1.5Vpp of differential signal is input, modulated output goes to +1Vpp.

● **Sinc3 Digital Filter**

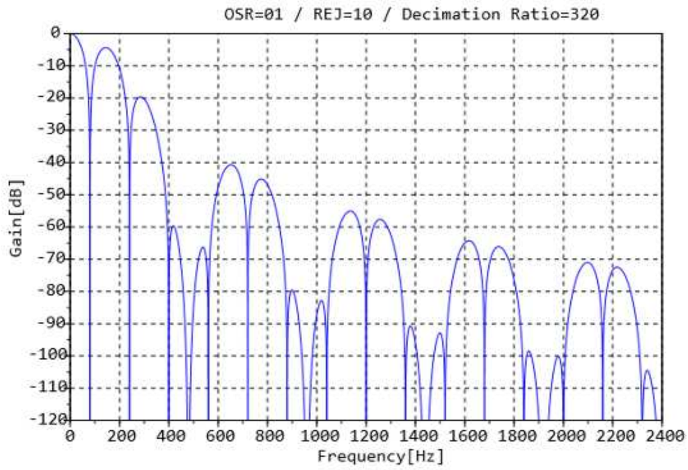
Digital Filter in NJU9101 is 3rd Order Sinc-Filter that has 768 of maximum decimation ratio. This decimation ratio can be set by 'OSR' and 'REJ' bit.



■ Sinc3 filter frequency example 1
(CHOPPING OFF setting example)

Conversion Time = 7.5ms (Single conversion)

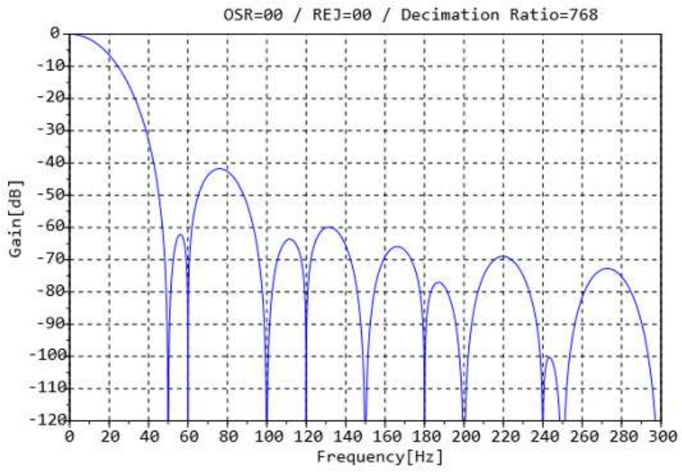
Decimation Ratio=320
(OSR=01, REJ=10, CLKDIV=00, ADCCHOP=0)



■ Sinc3 filter frequency example 2
(CHOPPING ON setting example)

Conversion Time = 13.8ms (Single conversion)

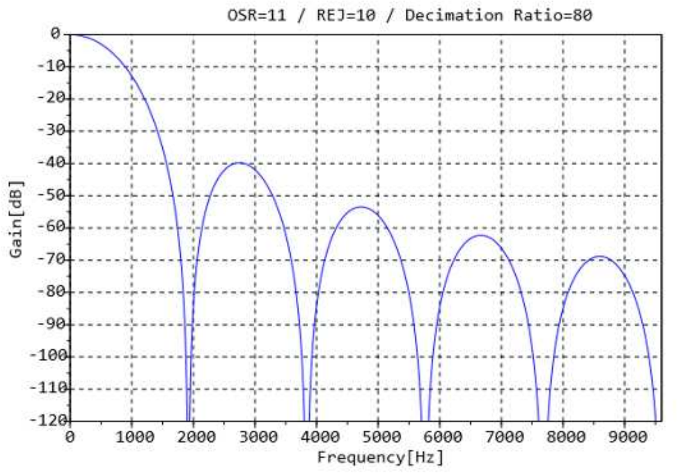
Decimation Ratio = 320
(OSR=01, REJ=10, CLKDIV=00, ADCCHOP=1)



■ Sinc3 filter frequency example 3
(50 / 60Hz Reduction setting example)

Conversion Time = 61.6ms (Single Conversion)

Decimation Ratio = 768
(OSR=00, REJ=00, CLKDIV=10, ADCCHOP=0)



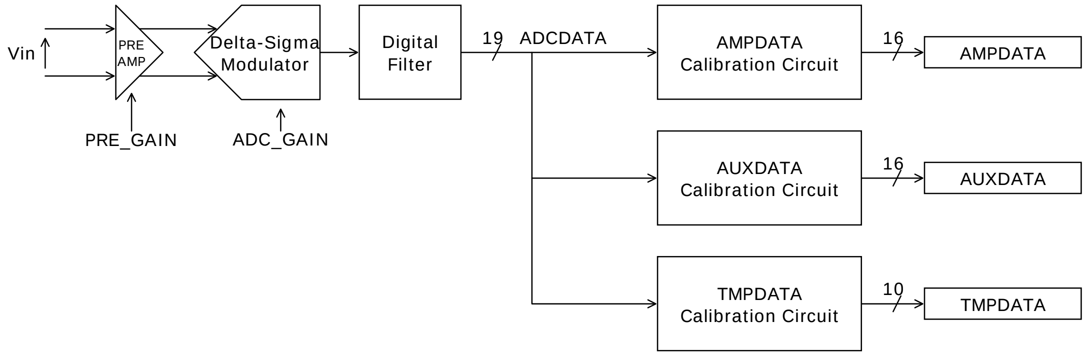
■ Sinc3 filter frequency example 4
(Fastest Conversion Time setting example)

Conversion Time = 2.8ms (Single Conversion)

Decimation Ratio = 80
(OSR=11, REJ=10, CLKDIV=00, ADCCHOP=0)

● **Data Calibration**

Analog Input is modulated to PDM signal by 2nd Order ΔΣ modulator. And then, this PDM signal is changed to signed 19 bit PCM signal (ADCDATA) by Sinc3 Digital Filter. The full-scale range of ADCDATA is -262144 to +26143 (0x40000 to 0x3FFFF). ADCDATA is stored to AMPDATA / AUXDATA / TMPDATA register after data calibration.



Regarding calculation of ADCDATA, Voltage GAIN of PREAMP (G_{pre}) and Conversion GAIN of ADC (G_{adc}) are defined as below,

Gain of PREAMP

PAMPSEL	PRE_GAIN	G_{pre}
0	XX	1
1	00	1
1	01	2
1	10	4
1	11	8

Gain of ADC

ADC_GAIN	G_{adc}
00	1
01	2
10	4
11	8

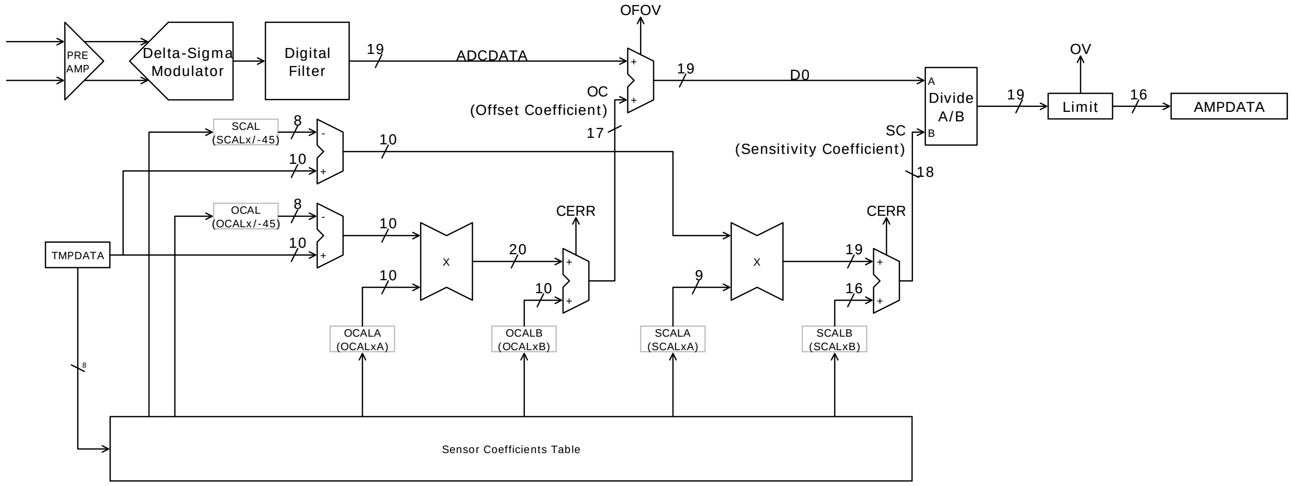
When it is assumed that
"Vref" :Reference Voltage selected by "VREFSEL"bit.
"Vin" :Differential Input Voltage of PREAMP

Digital Filter Output (ADCDATA) is output as below, when ADCDATA range is limited as signed 19 bit range (min:-262144(0x40000), max:+262143(0x3FFFF).

$$\mathrm{ADCDATA} = 262144 \times G_{pre} \times G_{adc} \times \frac{2}{3} \times \frac{V_{in}}{V_{ref}}$$

● AMPDATA Calibration

AMPDATA Calibration has temperature calibration of offset and Sensitivity for ADCDATA. And then, calibrated data is stored to AMPDATA[15:0] register. AMPDATA calibration path is shown in below.



Calibration coefficients for offset are set for four temperature areas. For these temperature areas, 0-order coefficient (offset value: OCALxB at OCALx[°C]) and 1st-order coefficient (temperature slope: OCALxA) are set. These temperature area are set by OCALx[°C] (-45°C ≤ OCAL1 < OCAL2 < OCAL3 ≤ 127°C). These coefficients are automatically selected by TEMPDATA value. Offset Calibration coefficient "OC" is signed 17-bits factor and calculated as below

Condition	Calculation
-45 ≤ TEMPDATA [9:2] < OCAL1	OC = [{TEMPDATA – (-45 x 4) } x OCAL1A] + (OCAL1B x 4)
OCAL1 ≤ TEMPDATA [9:2] < OCAL2	OC = [{TEMPDATA – (OCAL1 x 4) } x OCAL2A] + (OCAL2B x 4)
OCAL2 ≤ TEMPDATA [9:2] < OCAL3	OC = [{TEMPDATA – (OCAL2 x 4) } x OCAL3A] + (OCAL3B x 4)
OCAL3 ≤ TEMPDATA [9:2]	OC = [{TEMPDATA – (OCAL3 x 4) } x OCAL4A] + (OCAL4B x 4)

* When "OC" value exceeds signed 17-bits range (-65536 to +65535 (0x10000 to 0x0FFFF)), "CERR" bit is set as error flag of offset calibration coefficient. In this situation, AMPDATA is not correct value.

And then, ADCDATA and offset coefficient "OC" are summed. Converted DATA "D0" is calculated as below,

D0 = ADCDATA + (OC x 4)

* When "D0" value exceeds signed 19-bits range (-262144 to +262143 (0x40000 to 0x3FFFF)), "OFOV" bit is set as error flag. In this situation, AMPDATA is not correct value.

Calibration coefficients for sensitivity are set for four temperature areas. For these temperature areas, 0-order coefficient (sensitivity value: SCALxB at SCALx[°C]) and 1st-order coefficient (temperature slope: SCALxA) are set. These temperature area are set by SCALx[°C] (-45°C ≤ SCAL1 < SCAL2 < SCAL3 ≤ 127°C). These coefficients are automatically selected by TEMPDATA value. Sensitivity Calibration coefficient "SC" is unsigned 18-bits factor and calculated as below.

Condition	Caluculation
-45 ≤ TEMPDATA [9:2] < SCAL1	SC = [{TEMPDATA – (-45 x 4) } x SCAL1A] + (SCAL1B x 4)
SCAL1 ≤ TEMPDATA [9:2] < SCAL2	SC = [{TEMPDATA – (SCAL1 x 4) } x SCAL2A] + (SCAL2B x 4)
SCAL2 ≤ TEMPDATA [9:2] < SCAL3	SC = [{TEMPDATA – (SCAL2 x 4) } x SCAL3A] + (SCAL3B x 4)
SCAL3 ≤ TEMPDATA [9:2]	SC = [{TEMPDATA – (SCAL3 x 4) } + (SCAL4B x 4)

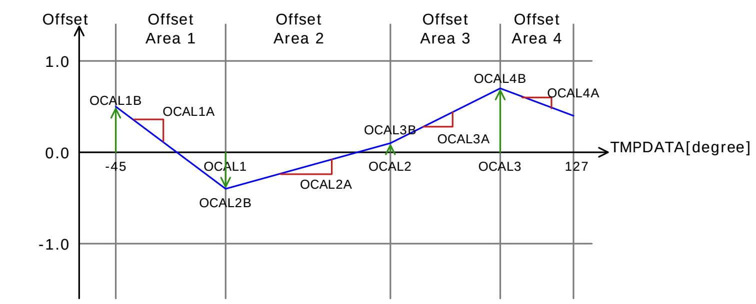
* When "SC" value exceeds the range of 8192 to 262143 (0x2000 to 0x3FFFF), "CERR" bit is set as error flag of sensitivity calibration coefficient. In this situation, AMPDATA is not correct value. And when "SC" value is regarded as signed 2.16 fixed point, this data range is equivalent to 4.0 to 0.125.

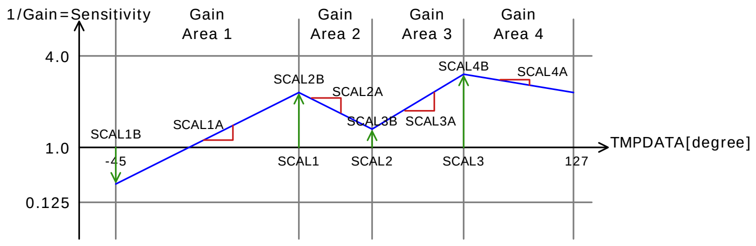
For Sensitivity calculation, offset conversion data "D0" is divided by "SC". This result (quotient) is rounded to integer, and then, AMPDATA is decided.

$$\mathrm{AMPDATA} = \mathrm{Round}\left(\frac{D0 \times 2^{14}}{SC}\right)$$

* When AMPDATA value exceeds signed 16-bits range (-32768 to +32767 (0x8000 to 0x7FFF)), "OV" bit is set as error flag. In this situation, ADCDATA value is limited to min: -32768(0x8000) or max: +32767(0x7FFF), and then stored to AMPDATA register.

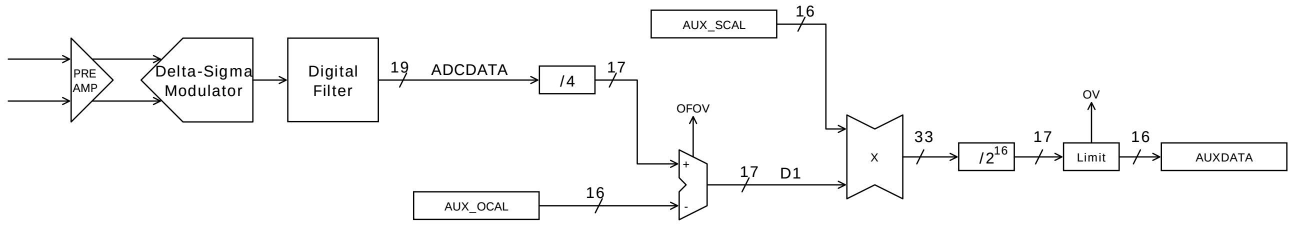
		Register	Calibration Range		Set Resolution	
			±1.0 conv.	14-Bit conv.	±1.0 conv.	14-Bit conv.
Offset coef.						
	0^{th}	OCALxB	±1.0	±8192	1 / (2^14)	0.5LSB
	1^{st}	OCALxA	±0.03125 / °C	±256LSB / °C	1 / (2 to 14) / °C	0.5LSB / °C
Sens coef.						
	0^{th}	SCALxB	x0.125 to x4.0	-	61ppm	-
	1^{st}	SCALxA	±15625ppm / °C	-	61ppm / °C	-





● **AUXDATA Calibration**

AUXDATA Calibration has offset and Sensitivity calibration for ADCDATA. And then, calibrated data is stored to AUXDATA[15:0] register. AUXDATA calibration path is shown in below.



Conversion Data "D1" after offset calibration is calculated as below. (Low order 2-bit of ADCDATA are rounded down)

$$\mathrm{D1} = \mathrm{Truncate}\left(\frac{ADCDATA}{4}\right) - \mathrm{AUX\_OCAL}$$

* When "D1" value exceeds signed 17-bits range (-65536 to +65535 (0x10000 to 0x0FFFF)), "OFOV" bit is set as error flag. In this situation, AUXDATA value is not correct value.

For sensitivity calibration, it is multiplied conversion data "D1" by "AUX_SCAL" coefficient. This result (product) is divided by 2^16, and is rounded to integer. And then, AMPDATA is decided.

$$\mathrm{AUXDATA} = \mathrm{Round}\left(\frac{D1 \times AUX\_SCAL}{2^{16}}\right)$$

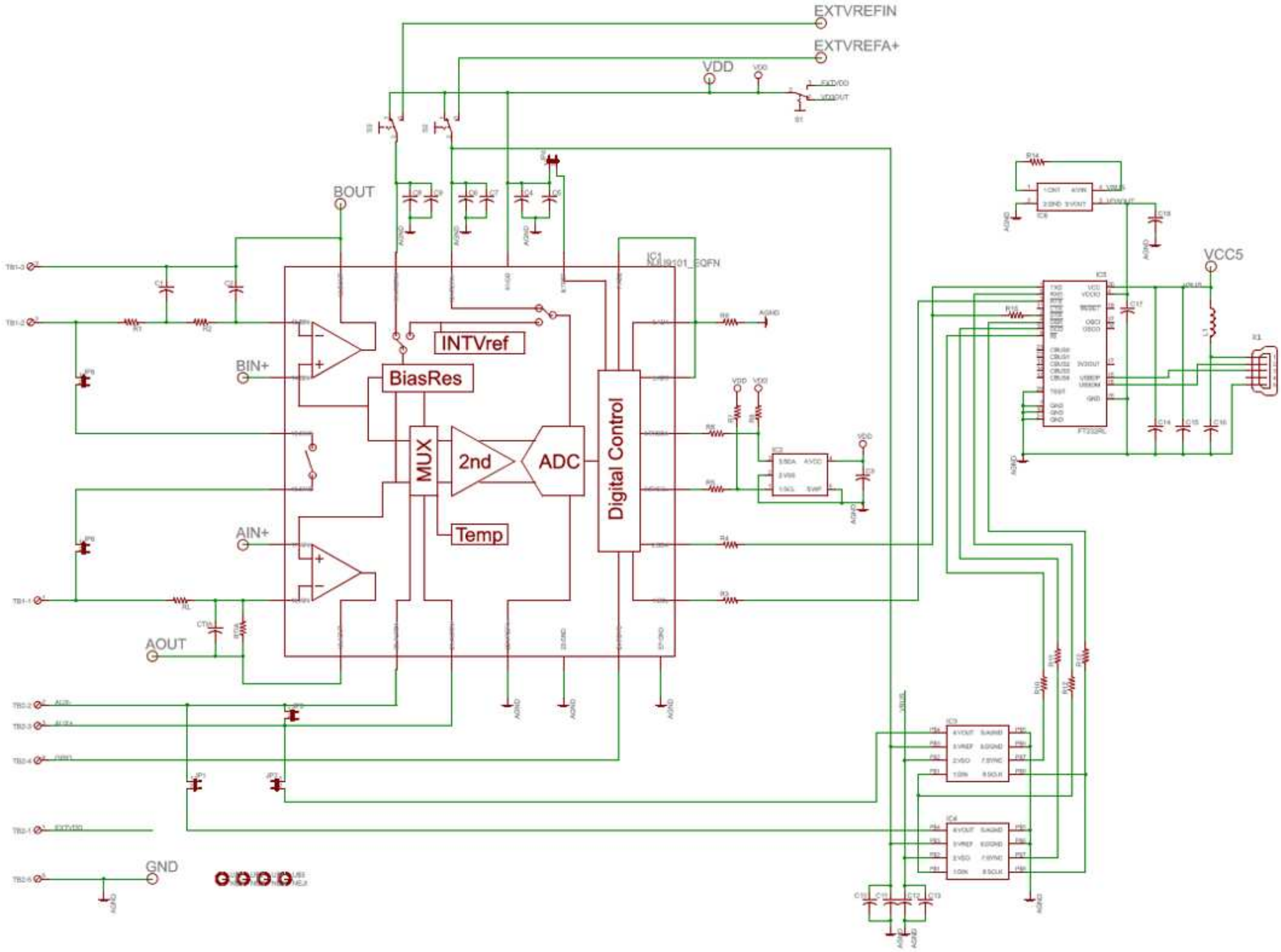
* When AUXDATA value exceeds signed 16-bits range (-32768 to +32767 (0x8000 to 0x7FFF)), "OV" bit is set as error flag. In this situation, ADCDATA value is limited to min: -32768(0x8000) or max: +32767(0x7FFF), and then stored to AUXDATA register.

	Register	Calibration Range		Set Resolution	
		±1.0 conv.	14-Bit conv.	±1.0 conv.	14-Bit conv.
Offset calibration coef.	AUX_OCAL	±0.5	±4096	1 / (2^17)	0.125LSB
Sensitivity calibration coef.	AUX_SCAL	x0.0 to x2.0	-	30.5ppm / °C	-

● **TMPDATA Calibration**

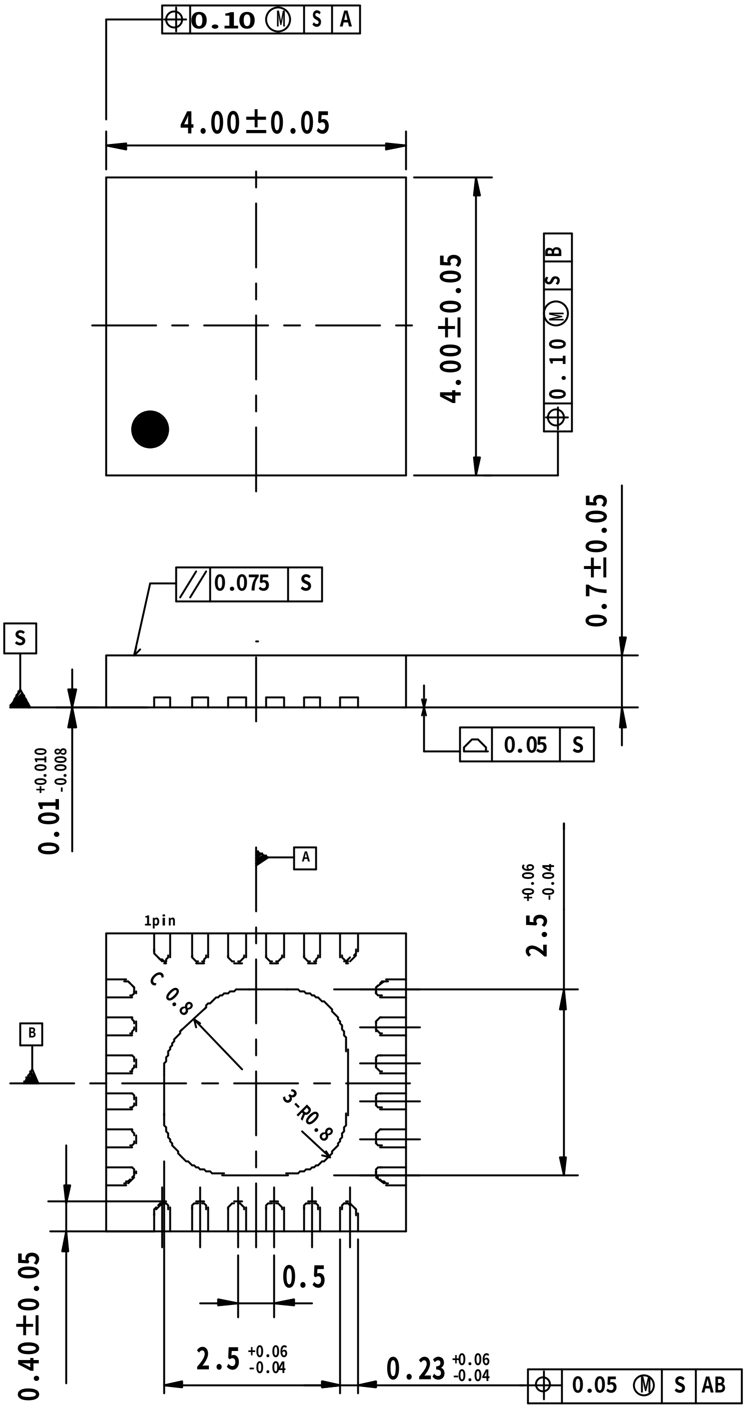
TMPDATA data conversion are converted ADCDATA to temperature code. In TMPDATA conversion, fixed setting of these bits "VREFSEL", "ADC_GAIN", PRE_GAIN" are used. TMPDATA is converted to signed 10-bits data shown as 0.25°C/LSB. The data range of TMPDATA is -45.00°C to +127.75°C (0x34C to 0x1FF). When converted value exceeds this range, "OV" bit is set as error flag. In this situation, ADCDATA value is limited to min: -45.00°C (0x34C) or max: +127.75°C (0x1FF), and then stored to TMPDATA register.

■EVALUATION BOARD・PCB LAYOUT



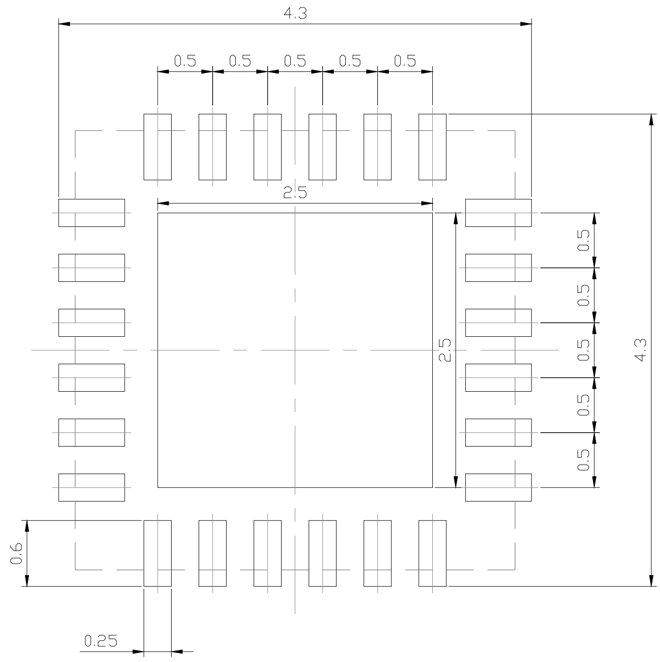
(Note) Install the decoupling capacitor in the proximity of the NJU9101.

■PACKAGE OUTLINE
EQFN-24-LE



■SOLDER FOOT PRINT

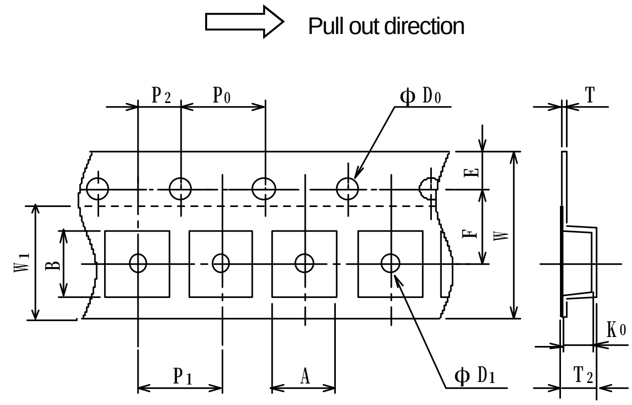
EQFN-24-LE



■**PACKING SPECIFICATION**

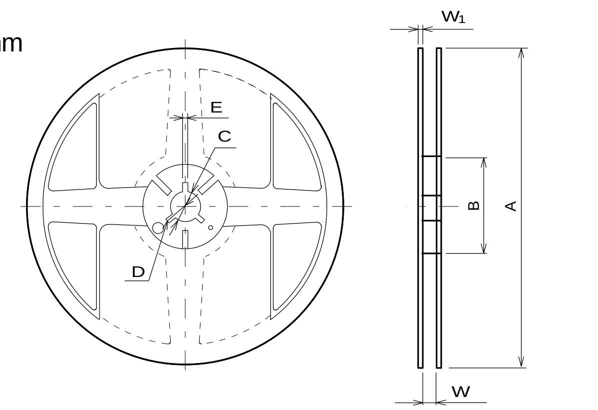
EQFN Emboss Taping (TE1)

Symbol	EQFN18-E7	EQFN24-LK	EQFN24-LE	Remark
A	2.25±0.05	4.35±0.05	4.35±0.05	Bottom size
B	2.25±0.05	4.35±0.05	4.35±0.05	Bottom size
D_0	1.5 +0.1/-0	1.5 +0.1/-0	1.5 +0.1/-0	
D_1	0.5±0.1	1.0±0.1	1.0±0.1	
E	1.75±0.1	1.75±0.1	1.75±0.1	
F	3.5±0.05	5.5±0.05	5.5±0.05	
P_0	4.0±0.1	4.0±0.1	4.0±0.1	
P_1	4.0±0.1	8.0±0.1	8.0±0.1	
P_2	2.0±0.05	2.0±0.05	2.0±0.05	
T	0.25±0.05	0.3±0.05	0.3±0.05	
T_2	1.0±0.07	1.3±0.07	1.3±0.07	
K_0	0.65±0.05	-	-	
W	8.0±0.2	12.0±0.3	12.0±0.3	
W_1	5.5	9.5	9.5	Thickness 0.1MAX

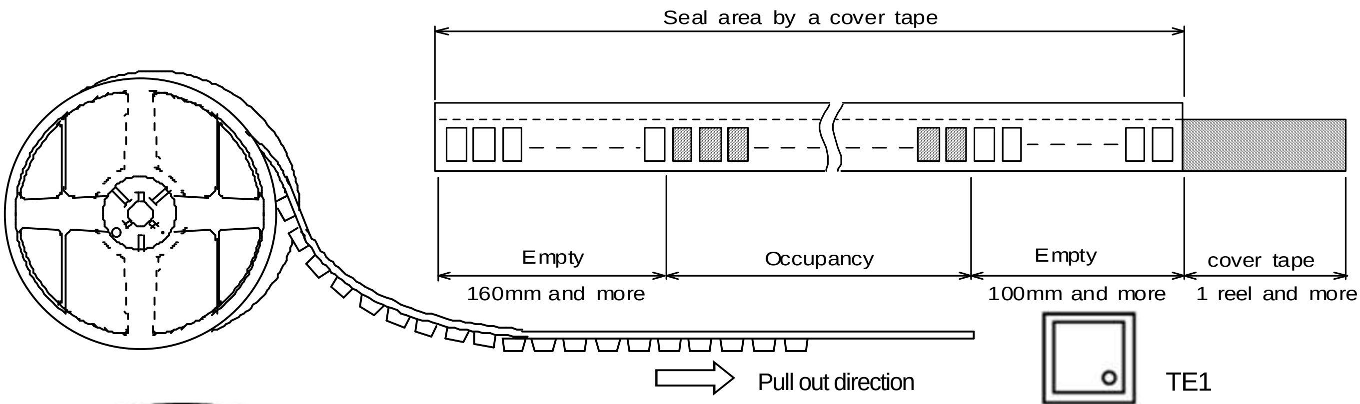


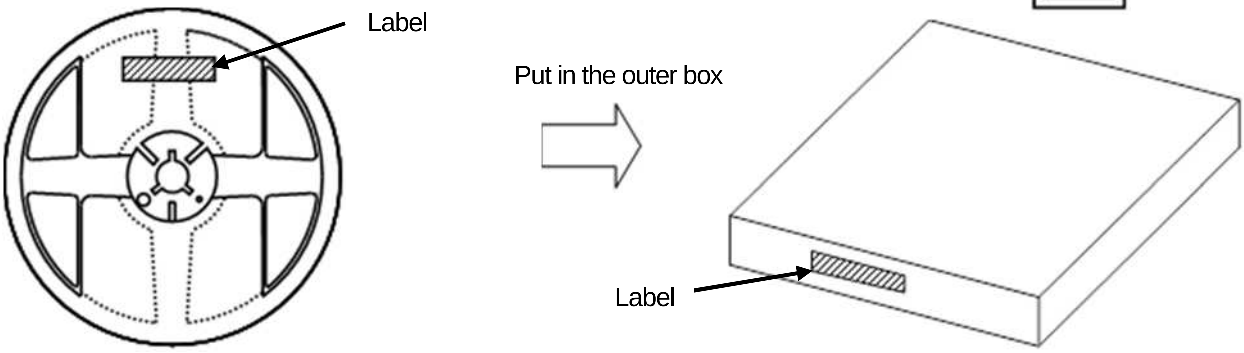
Unit: mm

Symbol	EQFN18-E7	EQFN24-LK	EQFN24-LE
A	Ø 180 +0/-1.5	Ø 180 +0/-1.5	
B	Ø 60 +1/-0	Ø 60 +1/-0	
D_0	Ø 13±0.2	Ø 13±0.2	
D_1	Ø 21±0.8	Ø 21 ± 0.8	
E	2.0±0.5	2.0±0.5	
W	9.0 +0.3/-0	13.0 +1.0/-0	
W_1	1.2	1.2	
Contents	3,000pcs	1,000pcs	



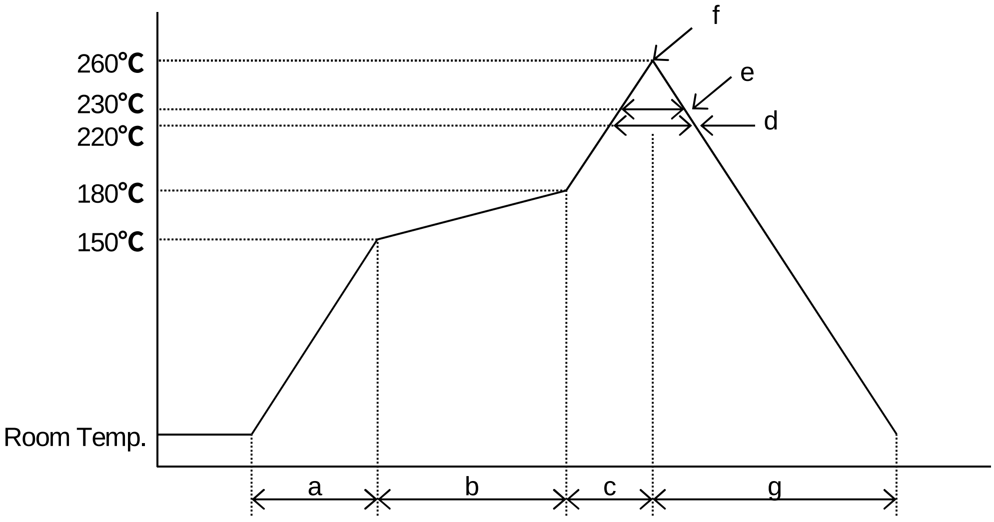
Unit: mm





■RECOMMENDED MOUNTING METHOD

＊Recommended reflow soldering procedure



a : Temperature ramping rate	: 1 to 4°C/s
b : Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c : Temperature ramp rate	: 1 to 4°C/s
d : 220°C or higher time	: Shorter than 60s
e : 230°C or higher time	: Shorter than 40s
f : Peak temperature	: Lower than 260°C
g : Temperature ramping rate	: 1 to 6°C/s

The temperature indicates at the surface of mold package.

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