DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

2SK3114

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

Description

The 2SK3114 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

Ordering Information

Part Number	Package
2SK3114	Isolated TO-220

Features

- Low gate charge :
  Q_G = 15 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 4.0 A)
- Gate voltage rating : ±30 V
- Low On-state resistance :
  $R_{DS(on)}$ = 2.2 Ω MAX. (V_{GS} = 10 V, I_D = 2.0 A)
- Avalanche Capability Ratings
- Isolated TO-220 package

Absolute Maximum Ratings (T_A = 25 °C)

Drain to source voltage (V_{GS} = 0 V)	V_{DSS}	600	V
Gate to source voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain current (DC) (T_C = 25 °C)	$I_{D(DC)}$	±4.0	A
Drain current (pulse) Note1	$I_{D(pulse)}$	±16	A
Total power dissipation (T_A = 25 °C)	P_{T1}	2.0	W
Total power dissipation (T_C = 25 °C)	P_{T2}	30	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C
Single avalanche current Note2	I_{AS}	4.0	A
Single avalanche energy Note2	E_{AS}	10.7	mJ
Diode recovery dv/dt Note3	dv/dt	3.5	V/ns

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

3. I_F ≤ 2.0 A, V_{clamp} = 600 V, di/dt ≤ 100 A /μs, T_A = 25 °C

The information in this document is subject to change without notice

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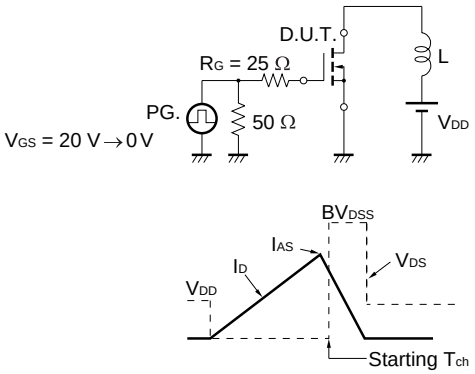
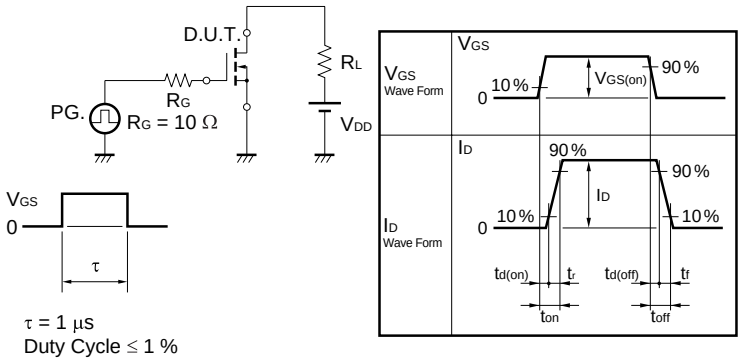
Electrical Characteristics (T_A = 25 °C)

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Drain leakage current	I_{DSS}			100	μA	V_{DS} = 600 V, V_{GS} = 0 V
Gate leakage current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0 V
Gate cutoff voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance	$\lvert y_{fs} \rvert$	1.0			S	V_{DS} = 10 V, I_D = 2.0 A
Drain to source on-state resistance	$R_{DS(on)}$		1.6	2.2	Ω	V_{GS} = 10 V, I_D = 2.0 A
Input capacitance	C_{iss}		550		pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance	C_{oss}		115		pF	
Reverse transfer capacitance	C_{rss}		13		pF	
Turn-on delay time	$t_{d(on)}$		12		ns	V_{DD} = 150 V, I_D = 2.0 A, $V_{GS(on)}$ = 10 V, R_G = 10 Ω, R_L = 10 Ω
Rise time	t_r		6		ns	
Turn-off delay time	$t_{d(off)}$		35		ns	
Fall time	t_f		12		ns	
Total gate charge	Q_G		15		nC	V_{DD} = 450 V, V_{GS} = 10 V, I_D = 4.0 A
Gate to source charge	Q_{GS}		4		nC	
Gate to drain charge	Q_{GD}		4.4		nC	
Diode forward voltage	$V_{F(S-D)}$		0.9		V	I_F = 4.0 A, V_{GS} = 0 V
Reverse recovery time	t_{rr}		1.3		μs	I_F = 4.0 A, V_{GS} = 0 V, di/dt = 50 A /μs
Reverse recovery charge	Q_{rr}		4.3		μC	

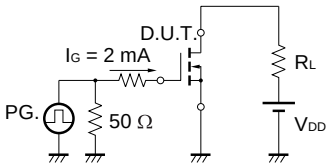
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

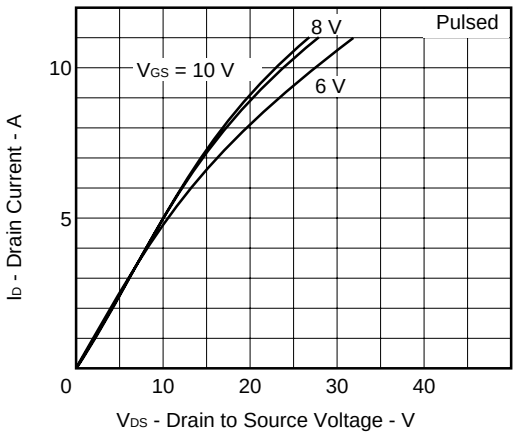


Test Circuit 3 Gate Charge

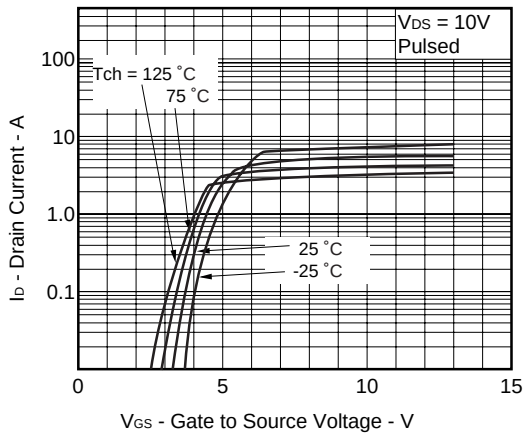


Typical Characteristics (T_A = 25 °C)

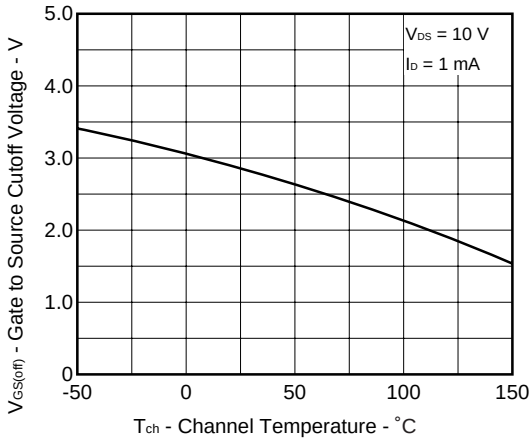
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



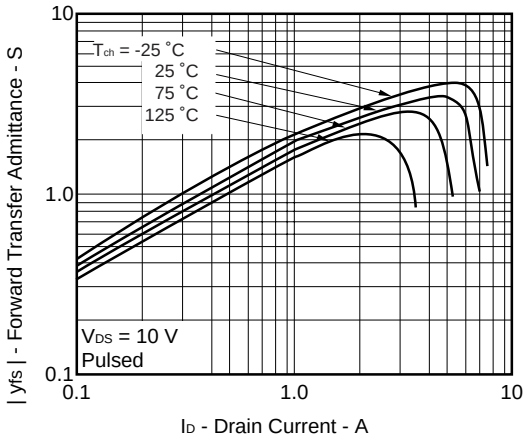
FORWARD TRANSFER CHARACTERISTICS



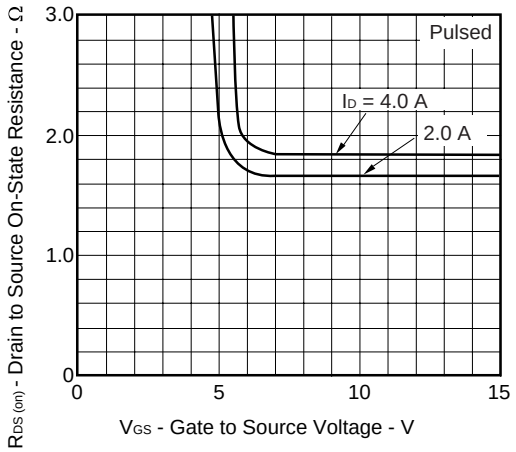
GATE TO SOURCE CUTOFF VOLTAGE
vs. CHANNEL TEMPERATURE



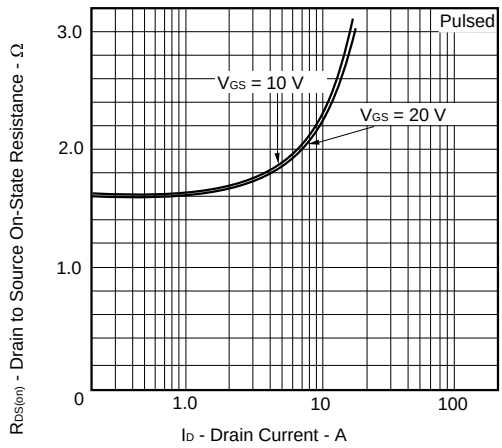
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



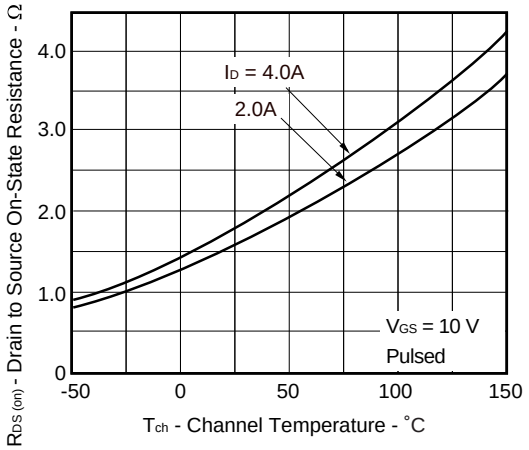
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



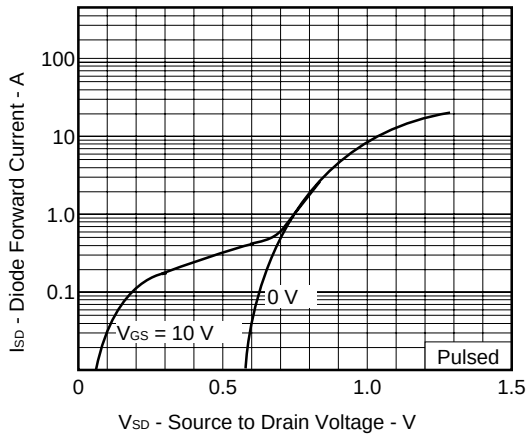
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



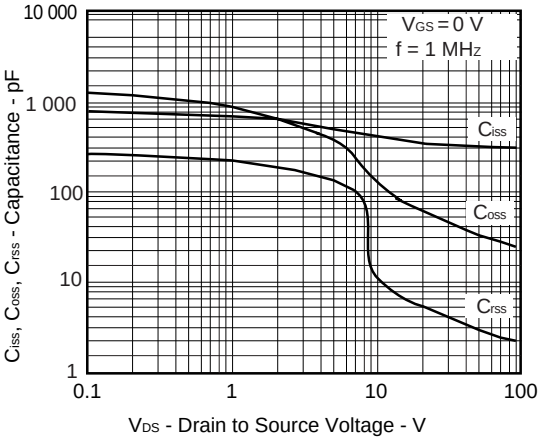
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



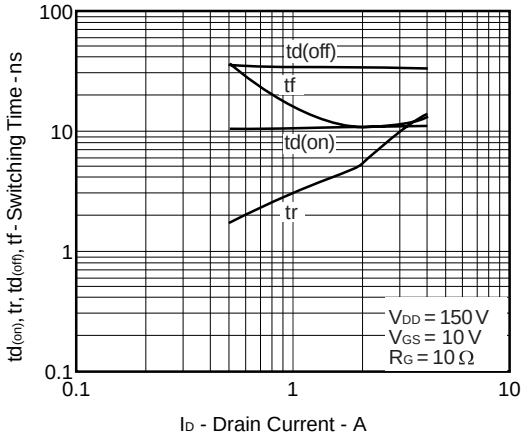
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



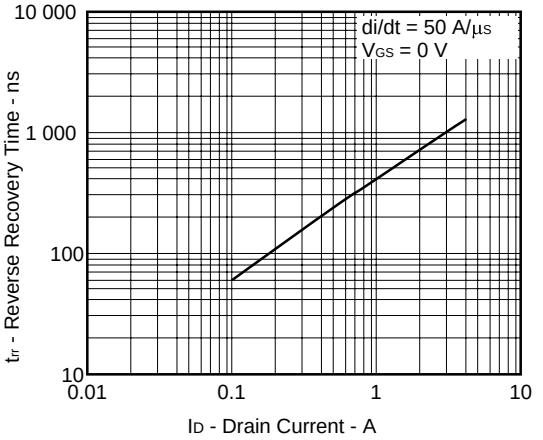
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



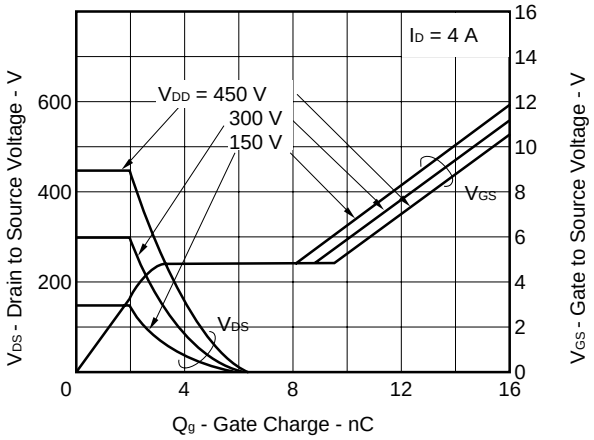
SWITCHING CHARACTERISTICS



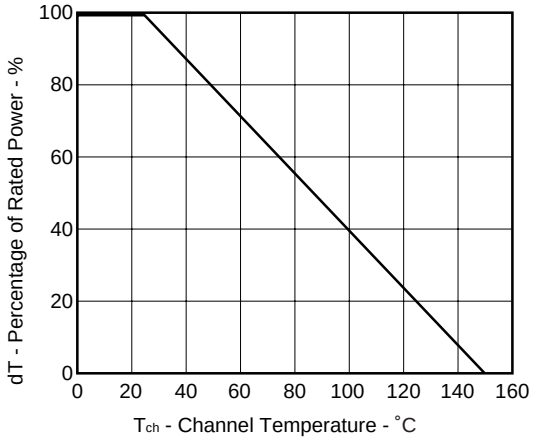
REVERSE RECOVERY TIME vs. DRAIN CURRENT



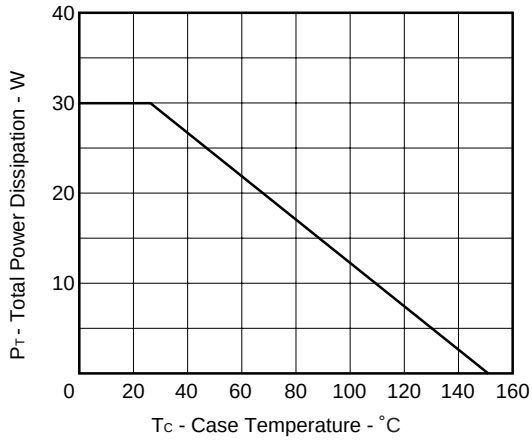
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



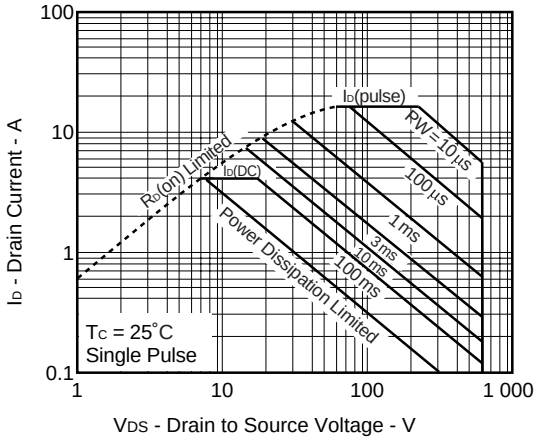
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



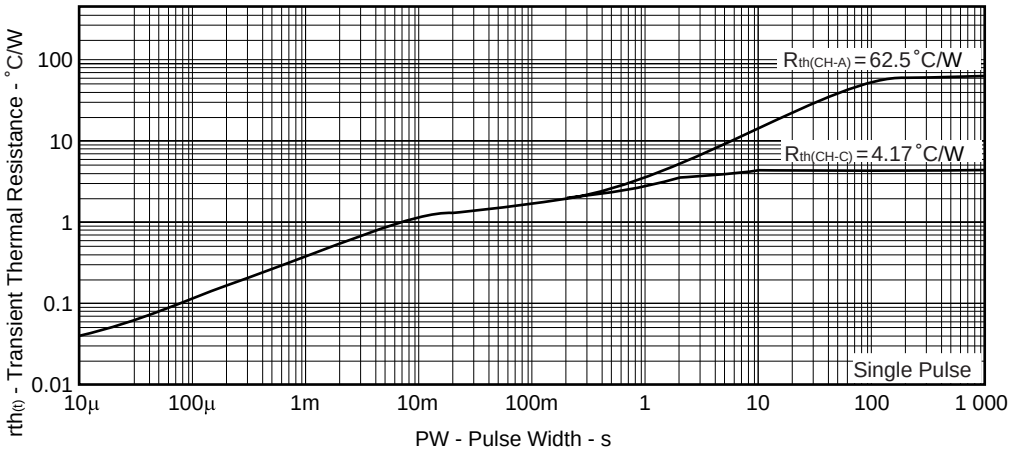
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

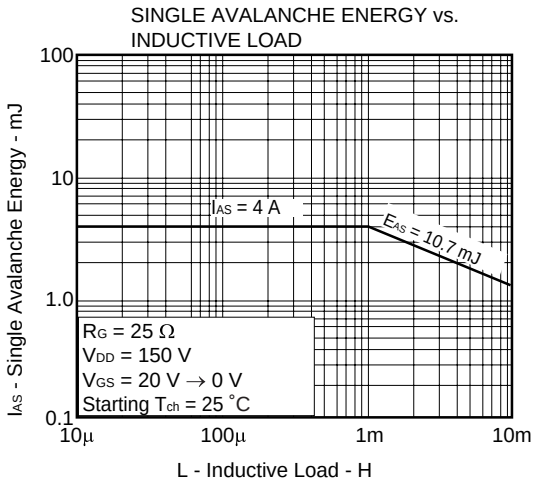


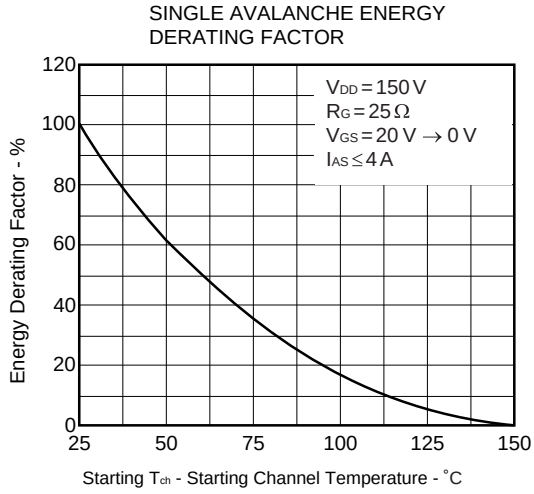
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

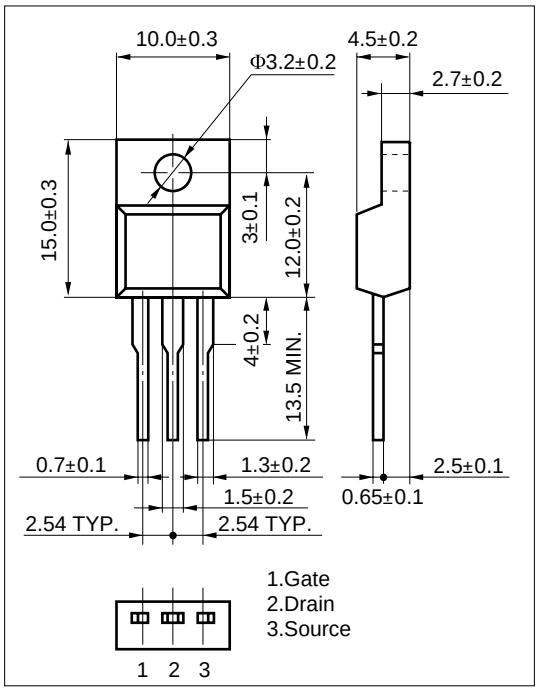




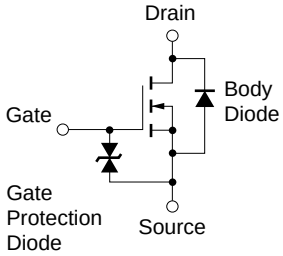


Package Drawing (Unit : mm)

Isolated TO-220 (MP-45F)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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