TelCom Semiconductor, Inc.

APPLICATION NOTE 28

TC4420/4429 UNIVERSAL POWER MOSFET INTERFACE IC

By Ron Vinsant

The TC4420/4429 are high power driver ICs in an 8-pin mini-dip package. These parts have additional improvements over the TC429 driver. Added features are 4 kV of ESD protection, latch-up protection of >1.5kA of reverse output current, logic inputable to withstand up to 5V negative swings. Although designed as a power MOSFET driver, it can act as a level shifter, comparator, waveshaper, and pulse transformer driver, just to mention a few of its possible uses.

Some of the other notable parameters of the TC4420/4429 are its excellent noise immunity due to a Schmitt trigger input and CMOS construction, its minimal quiescent current draw (with its input in the low state it consumes less than 150 µA), and its rise and fall time are matched and is typically at 25 ns at 25°C into 2,500 pF load.

Due to their low current CMOS input, the TC4420/4429 do not need speed up capacitors in the input. This type of input also has the ability to accept any amplitude signal from negative 5V to the supply voltage.

Parameters and Attributes of the TC429 Timing

Rise and Fall Times

In the TC4420/4429 the tr and tf are governed by three factors. These are temperature, supply voltage and output load (see figures 3 through 5). Definition of the first two parameters is self explanatory, but output load is not defined in the ordinary dimensions of ohms or Watts as might be expected. Since the TC4420/4429 were designed to drive power MOSFETs their load is expressed in capacitance. This is due to the fact that a MOSFET gate looks like a capacitor to the driving device.

Since a MOSFET actually appears as a variable capacitance as it turns on and off, it is hard to say exactly what the rise and fall times of the driver are going to be in any particular circuit. In order to simplify the measuring method we chose a fixed value of capacitance. This allows the designer to compare driving devices on a specification sheet. Actual evaluation in your application, however, is the best way to compare any two drivers.

When measuring time relationships be sure to take into account any delays that might skew the measurement. This can come from oscilloscope probes of unequal length or propagation delays through current probes and their associated amplifiers.

There are three anomalies that are associated with the rise and fall time:

1. The rise and fall times are not equal creating a small asymmetry in the output waveform. (See figures 2, 6 and 7.) This is due to having a P-channel device source current and an N-channel sink current from the load. (See figure 11.) P-channels do not perform as well as N types, so the input of the TC4420/4429 we have made the P larger to compensate. This does not make the P equal to the N in dynamic performance, only in static RDS(ON). This difference is most notable at higher loads. (See Figure 6.) At light loads the P actually outperforms the N in speed. (See Figure 2.)
2. There occurs a small "notch" in the rising waveform of about 5 ns in duration. It only occurs with loads above 4000 pF and is not normally of any concern. In Figure 1, wave form A shows the output of the TC4420/4429 with a 6800 pF load. The "notch" is noticeable in the rising waveform; and waveform B is a magnified view of that rising edge. Note that if the "notch" were not there, the rise time would not substantially change.

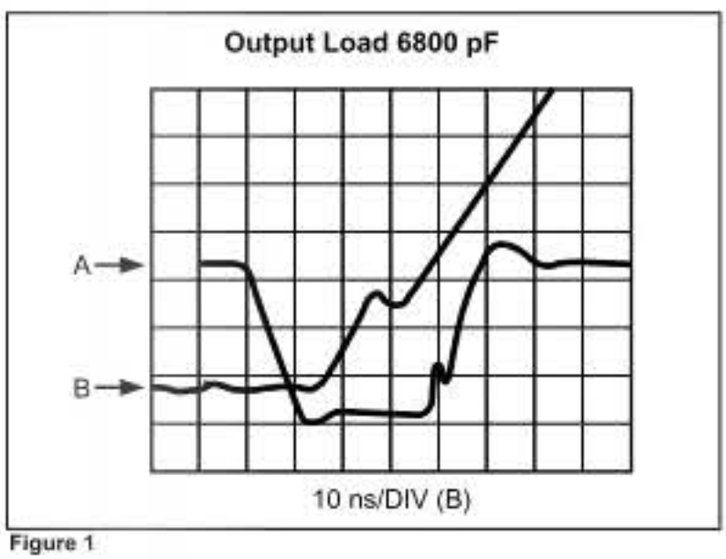

Figure 1

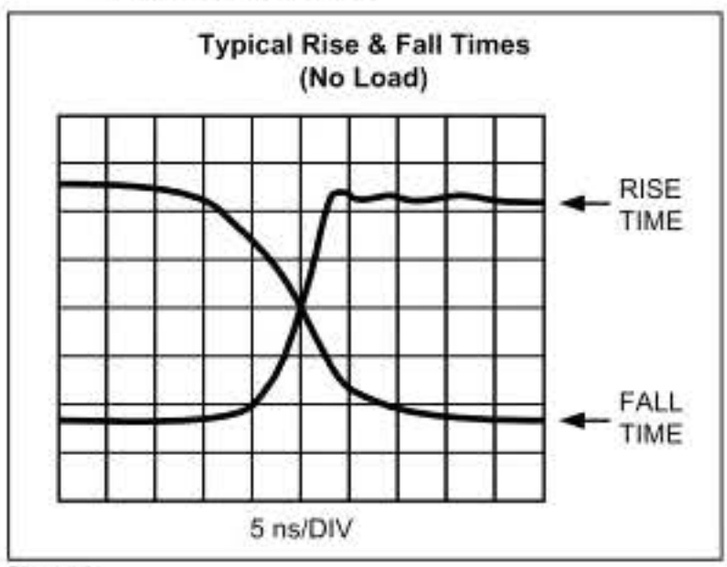

Figure 2

Rise Time vs Supply Voltage

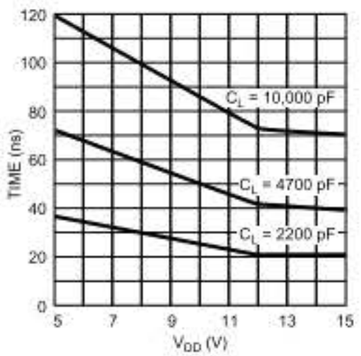

Figure 3

Fall Time vs Supply Voltage

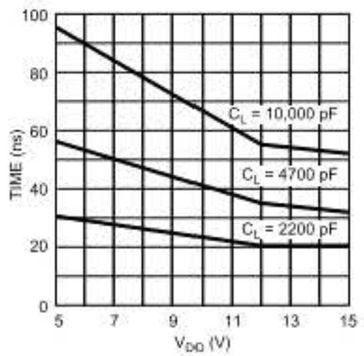

Figure 4

Rise and Fall Time vs Temperature

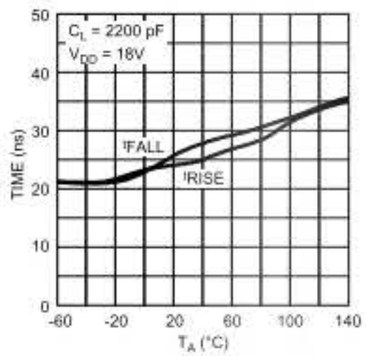

Figure 5

3300 pF Load

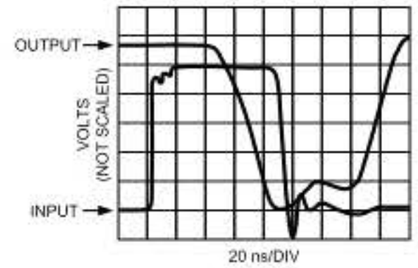

Figure 6

No Load

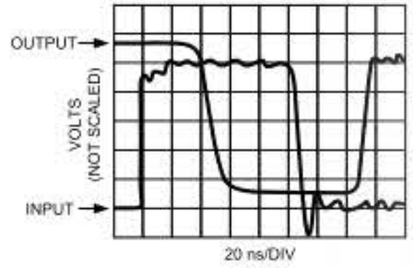

Figure 7

Effect of Input Amplitude on Propagation Delay

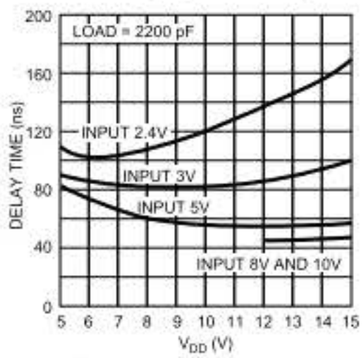

Figure 8

Propagation Delay Time vs Supply Voltage

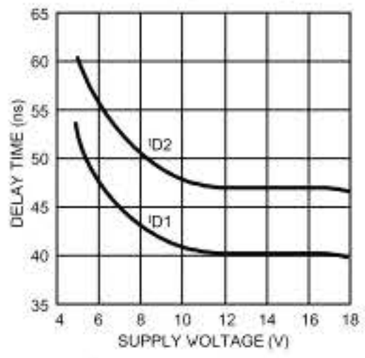

Figure 9

Propagation Delay Time vs Temperature

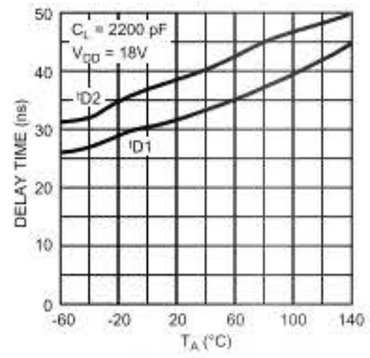

Figure 10

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3. Rise and fall times also determine the minimum pulse width in that if an input pulse has a width that is less than the sum of the rise and fall times the output cannot make a full transition. If carried to the extreme no output pulse will occur. At light loads typical minimum pulse widths would be in the 35 ns region. Figure 6 is an example of typical rise and fall times and minimum pulse width when driving a 3300 pF load.

Output rise and fall times are independent of input waveshape due to the Schmitt trigger input. In this respect, the device can be used as a waveshaper.

Delay Time (Propagation Delay)

Delay time is a function of input amplitude, supply voltage, and temperature. Figures 8, 9 & 10 show the effects of these parameters on delay time. Little can be done to lower the delay except for keeping the device temperature low and keeping the input amplitude above 5V. Please note that slow rising input signals can give the appearance of long delay times. This comes from the fact that the trip point of the Schmitt trigger input (about 1.5 volts) can often be higher than the 10% point in the waveform. In the specifications the times are measured from the 10 and 90 percent points as is industry practice. Figures 6 and 7 show typical performance. Note that the input waveform is shifted by 1/2 division on the vertical axis for purposes of clarity.

Input

Hysteresis

As we have mentioned before the TC4420/4429 has Schmitt trigger inputs. The hysteresis provided by the Schmitt action is measured with conditions static (DC) for the data sheet, and can change substantially when driven by a pulse. (For an explanation of how the input section works see the section entitled "Input Effects on Quiescent Current.") The input is capacitive as the input signal is driving a MOSFET gate. (See Figure 11.) It therefore has the characteristic Miller capacitance from drain to gate, as well as the gate to source capacitance. The device works most effectively when driven by a relatively low impedance source such as a CMOS or TTL buffer.

Since the input threshold is set by the input MOSFET's threshold (Figure 11), the trip point changes with temperature at the rate of approximately -5 mV/°C. For this reason, any input waveform that has slow rise times, such as open collector TTL, can exhibit a change in pulse width with a change in temperature at the output of the TC4420/4429. In applications where exact reproduction of pulse width from input to output is important, fast rise and fall times are important.

In other types of applications, however, where exact timing is not important the TC4420/4429 will act to improve the rise and fall times of slow rising input waveforms. (See Figure 12.)

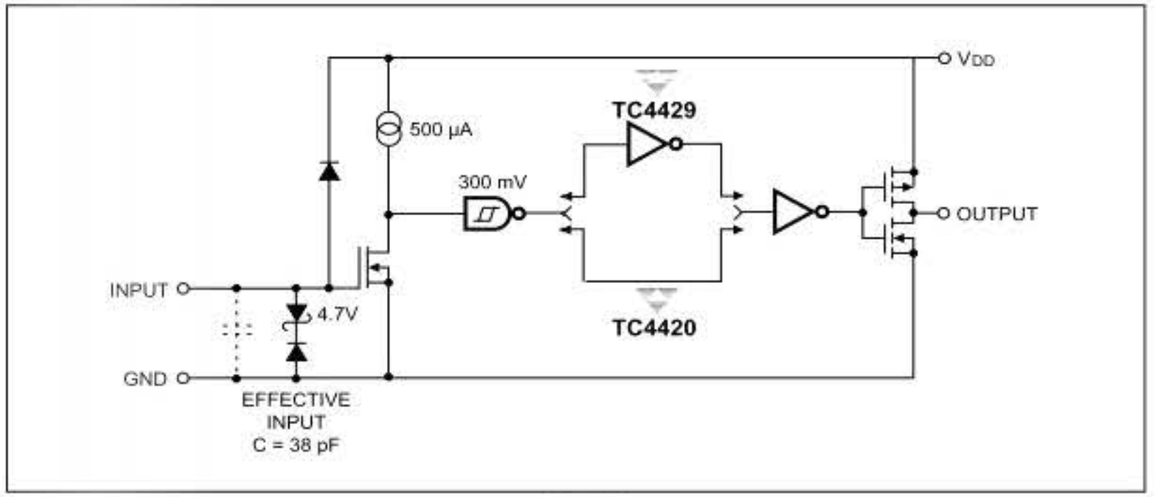

Figure 11

Input Section

The input is fully TTL compatible, yet can be driven by any amplitude signal up to the supply voltage and down to ground. This attribute makes the TC4420/4429 an excellent level translator from TTL to small motor or lamp loads on 12 to 15 volt systems.

Input Effects on Quiescent Current

The state of the input signal changes the quiescent current draw of the TC4420/4429. The reason for this can be seen in Figure 11 which shows the input signal driving a MOSFET whose drain is attached to a current source of 500 µA. The drain is connected to an inverter with 300 mV of hysteresis.

When the input signal is below the input FET threshold, the input MOSFET is off, causing the input to the inverter to be pulled high by the 500 µA current source. The inverter output therefore is low, causing the P-channel device of TC4429 to be on and output to be high. Since the current source is not able to source the current, the quiescent current is then composed only of the bias currents required by the inverter sections. (Assuming on load on the output.) In the state where the input is above the input FETs threshold, the input MOSFET turns on, sinking the 500 µA current source. This current increases the quiescent current draw in the high input state.

The hysteresis value changes with frequency (less hysteresis with increasing frequency). This phenomena occurs because of the characteristic decrease in the transconductance of the input FET with increasing frequency.

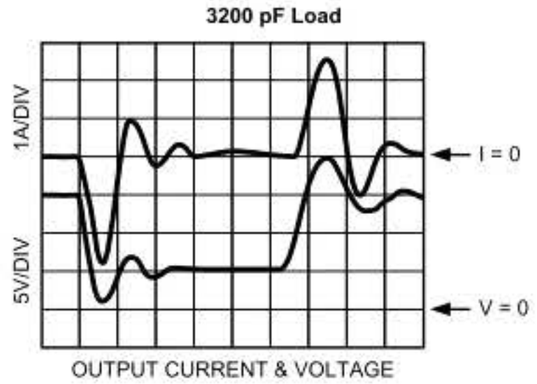

Figure 12

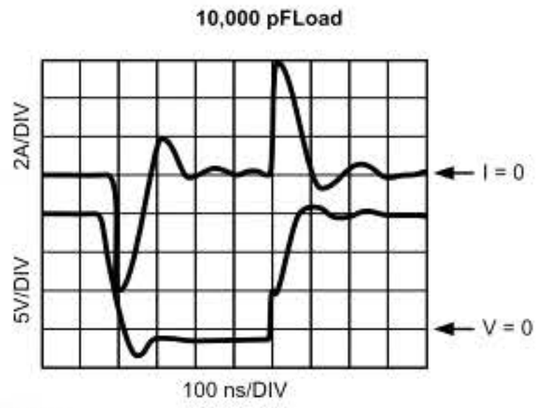

Figure 13

Output

Output Current

The TC4420/4429 can sink and source significant amounts of current. For example with a 10,000 pF load the output will swing from 15 volts to ground in 52 ns, sinking a current of almost 7 amps peak and then source 6 amps peak to bring the output back to 15 volts in 71 ns. (See Figures 3, 4 and 13.) This difference in switching times comes from the device construction described in the section on rise and fall times.

Due to the ability of the device to source large currents it is easy to exceed the power dissipation rating of the device under short circuit conditions. There is no thermal or overcurrent protection designed into the device so a short circuit for an extended period of time should be avoided.

"Saturation" Voltage

The output typically swings to within 25 mV of the supply rails. For applications where a steady state current is supplied by the device the on losses can be found in Figures 14 and 15.

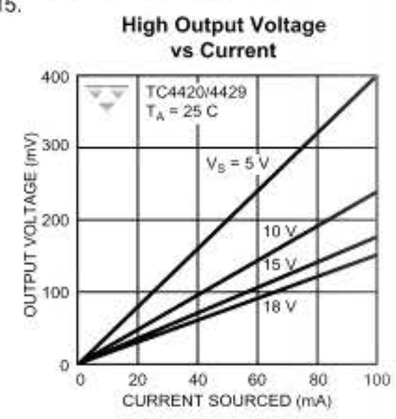

Figure 14

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Power Dissipation

Quiescent Dissipation

The quiescent dissipation of the TC4420/4429 are very low, even with the input in the high state. (See "Input" section on the effects of input state on power dissipation.) As an example, at maximum temperature for the plastic package (70°C) the static current draw is guaranteed to be 3 mA or less. If the supply voltage is 15 volts then the device dissipation is 45 mW at 70°C so the device is well within its range at worst case.

The typical current is normally in the region of 450 µA so the example cited above is indeed worst case.

Cross Over Dissipation

During the transition between the output states the P channel and N channel transistors can be on simultaneously. Although this happens for only a few nanoseconds, this additional power that is dissipated can be significant at frequencies above 1 MHz at 100 pF and above 250 kHz at 10,000 pF. (See Figures 11 and 27.)

Capacitive Load Dissipation

Capacitive load dissipation is the result of charging and discharging the load. The larger the capacitive load the longer the driver is in the linear region. As long as the device is in this area of operation it is dissipating significant amounts of power.

Calculating Power Dissipation

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

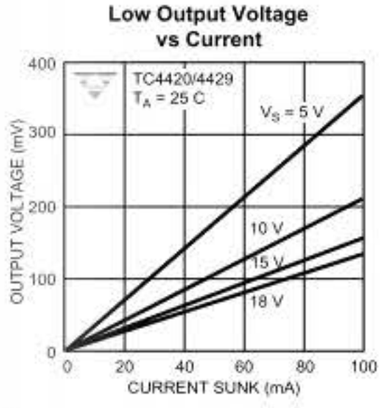


Figure 15

Equation 1:

$$P_C = f\ C\ V_S^2$$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 150 µA total current drain. Logic high signals raise the current to 1.5 mA maximum. The quiescent power dissipation is:

Equation 2:

$$P_Q = VS\ (D\ (I_H) + (1\text{-}D)\ I_L)$$

where: I_H = quiescent current with input high (1.5 mA Max)
I_L = quiescent current with input low (150 µA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

Equation 3:

$$P_T = f\ V_S\ (3.0 \times 10^{-9})$$

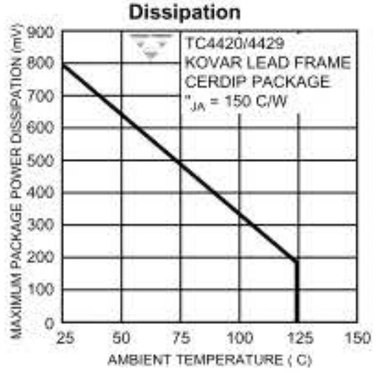
An example shows the relative magnitude for each term.

Example 1:
C = 2500 pf
V_S = 15 V
D = 50%
f = 200 kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 9 mW + 12.4 mW
= 134.4 mW
Max. operating temperature = $T_J - \theta_{JA}\ (P_D)$
= 130°

where:
T_J = Max allowable junction temperature (150°C)
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

Note: Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

Package Power Dissipation



TC4420/4429 Maximum Operating Frequency

V_s	f_{Max}
18V	500 kHz
15V	800 kHz
10V	2 MHz
5V	>3 MHz

Table 1

Conditions: 1. CerDIP Package [θ_{JA} = 105°C/W]
2. T_A = 25°C
3. C_L = 2200 pF

Heatsinking

If too much dissipation becomes a problem it is possible to heatsink the TC4420/4429. This accomplished by the use of a ground plane, or a heatsink attached to the device by a clip or thermal epoxy. Heat sink manufacturers such items. The use of the ground plane as a heatsink is done by inserting a small quantity of thermal grease on the bottom of the device before insertion to the board. The grease will transfer the heat to the ground plane.

Of the two packages the ceramic cerDIP package is the best for applications requiring heatsinking. This is due to the superior heat transfer ability of ceramic, in relation to the plastic. For this reason we recommend the use of the cerDIP package in all high dissipation applications (>300 mW).

In high power dissipation requirement, the 5-Pin TO-220 package can dissipate up to 12.5W at 25 degree C with proper heatsinking. The thermal impedance to case is 10 degrees per Watt. In free air, the 5-Pin TO-220 can dissipate 1.5W.

Designing With The TC4420/4429 Grounding Techniques

Grounding

The High current capability of the TC4420/4429 demands careful PC board layout for best performance. The TC4429 is an inverting driver. Any ground lead impedance will appear as negative feedback which can degrade noise immunity. The feedback is especially noticeable with slow-rise time inputs, such as are produced by an open collector output with resistor pull-up. The TC4420 is a non-inverting driver. It is very important to separate the digital input ground from the output ground. Any ground loop coupling from the output ground return to the input signal return may cause high frequency oscillation due to positive feedback. When using the TC4420 non-inverting driver, be sure the output ground is separated from the input signal ground return.

Figure 17 shows the feedback effect in detail. As the TC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the TC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the TC4429 GND pins should be connected to power ground. (See layout section)

Decoupling (Bypassing)

Decoupling the TC4429 requires careful layout and the use of good quality capacitors. A good quality film cap of low ESR such as the WIMA MKS-2 1μF at 50 Volt in parallel with a low ESR high resonant frequency ceramic will usually keep the peak to peak ripple voltage under 500 mV provided the caps are placed right next to the power supply pins of the driver. Tantalums and small electrolytic are not a good choice due to the high ripple current that the TC4429 generates.

Layout Considerations

One of the most important considerations in the application of the TC4429 is the PC board layout. As we have previously mentioned grounding is very important. Since the device generates very high recirculating currents due to its fast switching speed and low output impedance it is necessary to identify the paths of these currents and isolate them from the input signal (due to the negative feedback problem) and from the rest of the system.

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The second consideration is radiated noise. A ground plane under the device can act as a noise shield and is highly recommended. This ground plane, if put on top of the board can also act as a heatsink. (See the section on heatsinking).

Third, the TC4420/4429 has been designed with two ground pins 4 and 5, two V_{CC} pins 1 and 8 and two output pins 6 and 7. In each case both pins should be used as the currents are so high that a single bonding wire internal to the device may not be able to handle the currents without opening. This two sire path for these currents also lowers the inductance of the path which will (along with proper decoupling) help minimize ringing in the circuit. (See Figures 16 and 17).

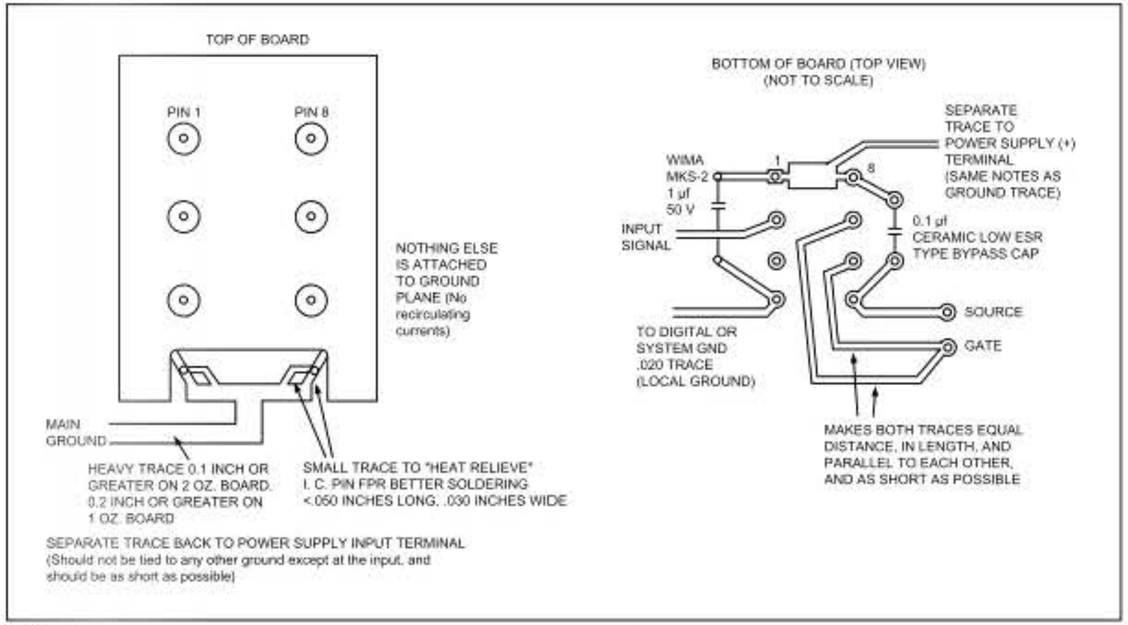

Figure 16

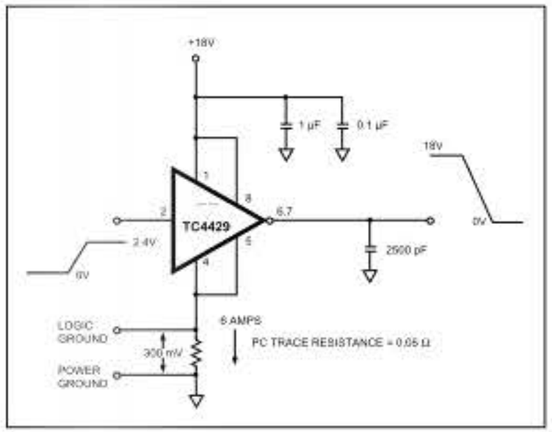

Figure 17: Switching Time Degradation Due to Negative Feedback

Driving Power MOSFETS

International Rectifier has published an application note, #973A, that describes the characteristics of a good MOSFET driver, and circuits that are suitable as drivers. Please note that many of the circuits described in this application note can be accomplished with the TC4420/4429 while improving performance, lower power consumption, and often with less parts.

In addition to the application note mentioned above, two other application notes by international Rectifier on driving MOSFETs are of use. The first, entitled "A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits" helps to understand the charge transfer necessary to drive MOSFETs, while the second application note, #947, entitled "Understanding HEXFET Switching Performance" gives a detailed mathematical analysis of the three turn on and turn off intervals. It also examines the effects of parasitic drain and source inductance, which can have a significant effect on switching performance indepen-

dent of the drive method.

These papers go into detail on what is important in driving MOSFETs and give additional necessary information that is beyond the scope of this paper.

We will show an example of a 400 volt 3 ohm FET being driven by a small CMOS driver (out of a CMOS 555 timer IC) and compare that to the same circuit where the TC4420 is driving the MOSFET. (See Figures 18 through 20). Nothing has been changed except for the addition of the TC4420. Note the substantial improvement in fall time.

Due to differences in timing characteristics the paralleling of two or more devices is not recommended. The best example of the reason for this is the problem of one device turning on a few nanoseconds before another. In this case the one that turned on first would be sinking current from the other. This would then create an increase in dissipation that could cause the faster device to overheat and self destruct. Since the rise and fall times of any two devices are not going to be the same, it is possible to get slower rise and fall times with two drivers in parallel than from a single driver due to the devices "fighting" each other.

Driving Inductive Loads

When driving inductive loads such as pulse transformers and small motors it may be necessary to keep the output from being driven beyond VCC. Leakage inductance and back EMF from motors can cause voltage spikes of sufficient amplitude to make the driver latch into its SCR mode.

The best way to prevent this from occurring is to put a Schottky diode from the output back to VCC. When the voltage at the output rises the diode turns on before the base emitter of the transistor and clamps the voltage to VCC plus the diode drop of 450mV. The same technique works for negative going excursions of voltage. (See Figure 26).

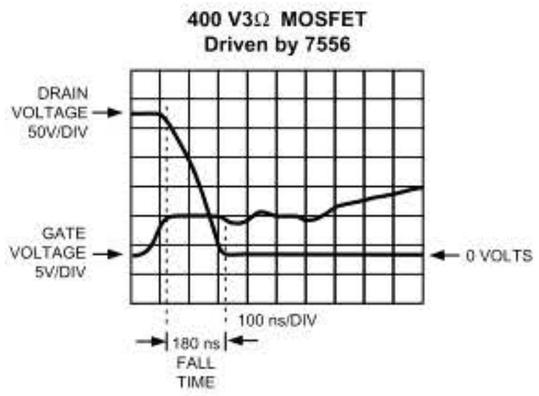

Figure 18

Applications

Small Motor Controller

Figure 21 shows a schematic of the TC4429 used as a small closed loop motor controller. The TC4429 is used as both driver and comparator in the control circuit. The back EMF of the motor is used as a feedback signal to detect motor speed.

Voltage Doubler

Figure 22 is a voltage doubler circuit. Typical performance is shown in Figure 23. Highest efficiency is obtained when using Schottky diodes in the output.

Voltage Inverter

Figure 24 is a voltage inverter with Figure 25 showing typical performance. As in the voltage doubler circuit

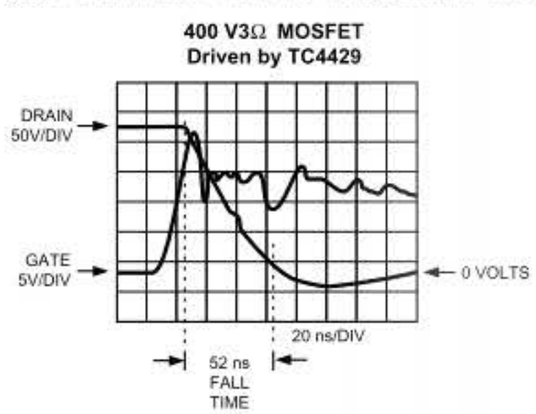

Figure 19

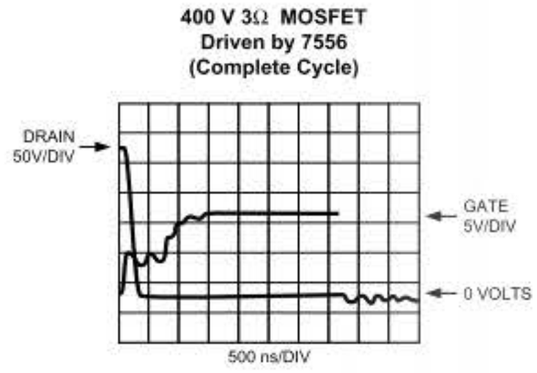

Figure 20

mentioned above the highest efficiency is obtained when using Schottky diodes, such as 1N5819. In both these circuits increasing the frequency of oscillation will help to reduce the value of the capacitors. Capacitors should be high quality electrolytics with low ESR. Ripple currents in the capacitors can be substantial in both of these circuits, so care should be taken in their selection.

High Power Pulse Transformer Driver

Figure 26 shows a high power pulse transformer driver that utilizes diode protection from leakage inductance spikes. This circuit can be used to drive large bipolar transistors, as well as FETs. The same sort of diode protection scheme should be applied to other inductive loads such as relays.

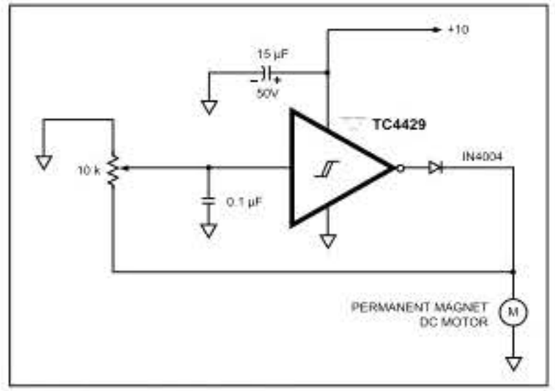

Figure 21: Motor Speed Controller

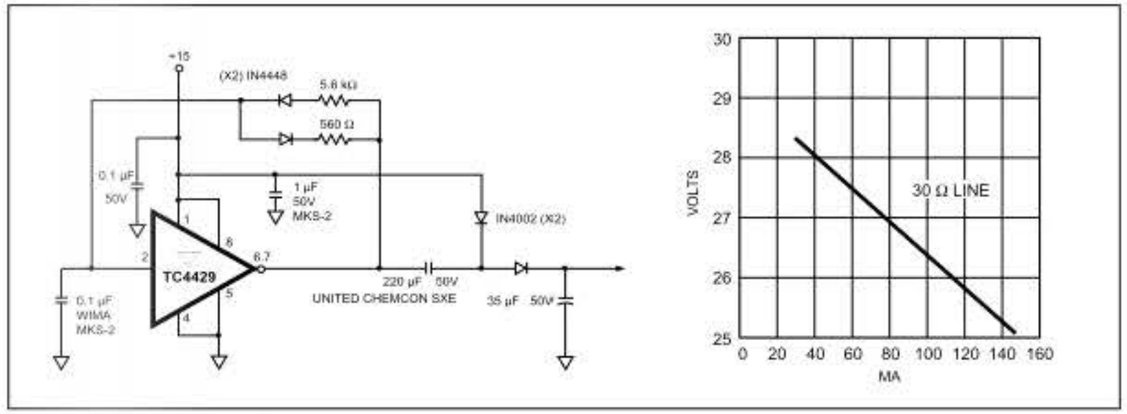

Figure 22: Self Contained Voltage Doubler

Figure 23

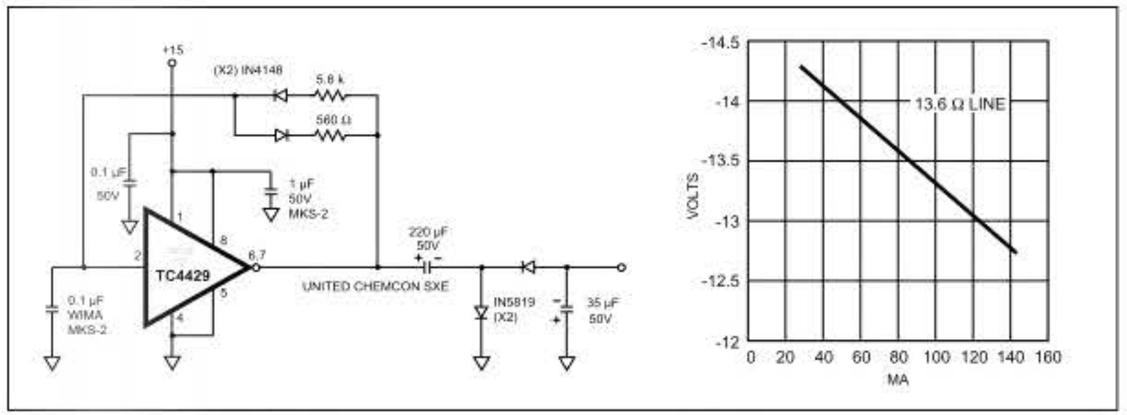

Figure 24: Self Contained Voltage Inverter

Figure 25

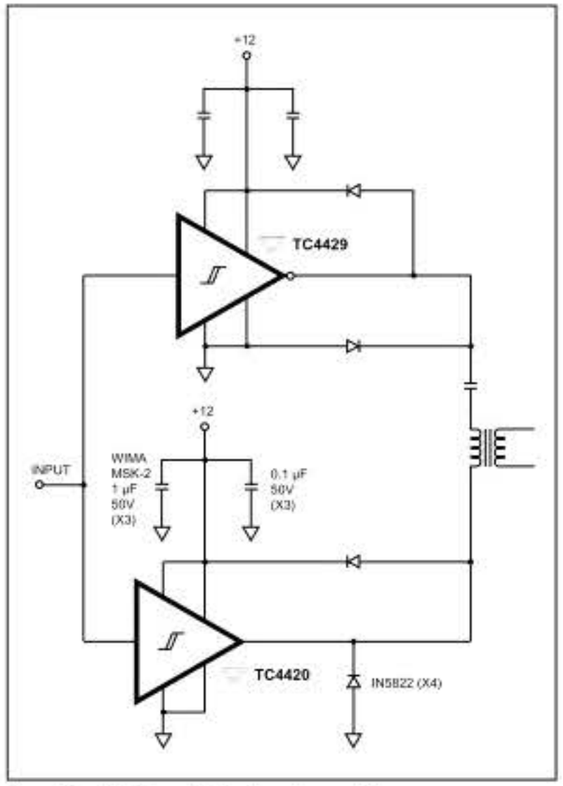

Figure 26: High Power Pulse Transformer Driver

Supply Current vx Capacitive Load

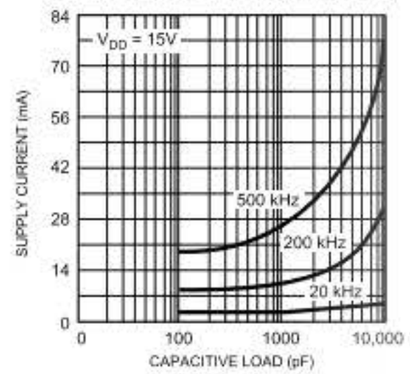

Figure 27

Supply Current vs Frequency

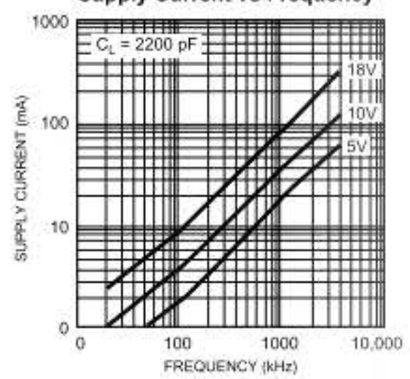

Figure 28

TC4420/4429 UNIVERSAL POWER
MOSFET INTERFACE IC

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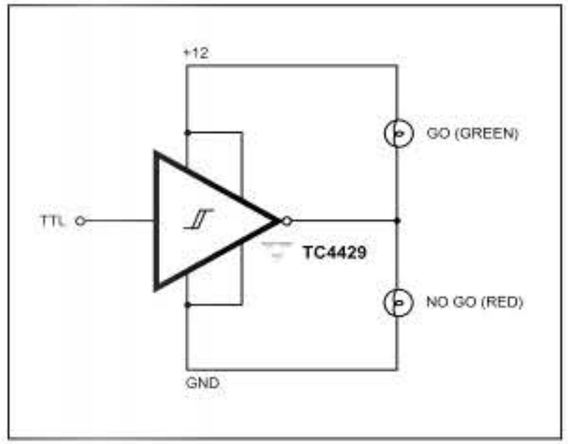
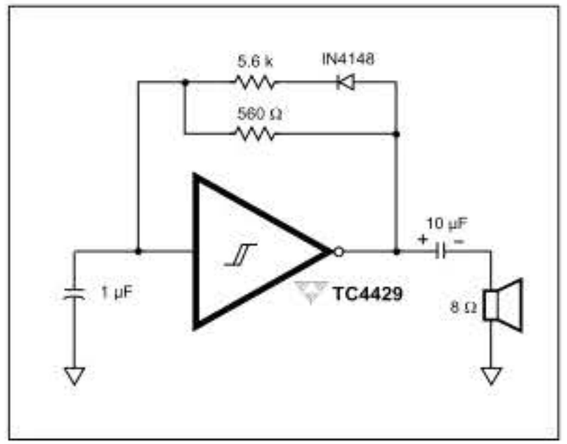
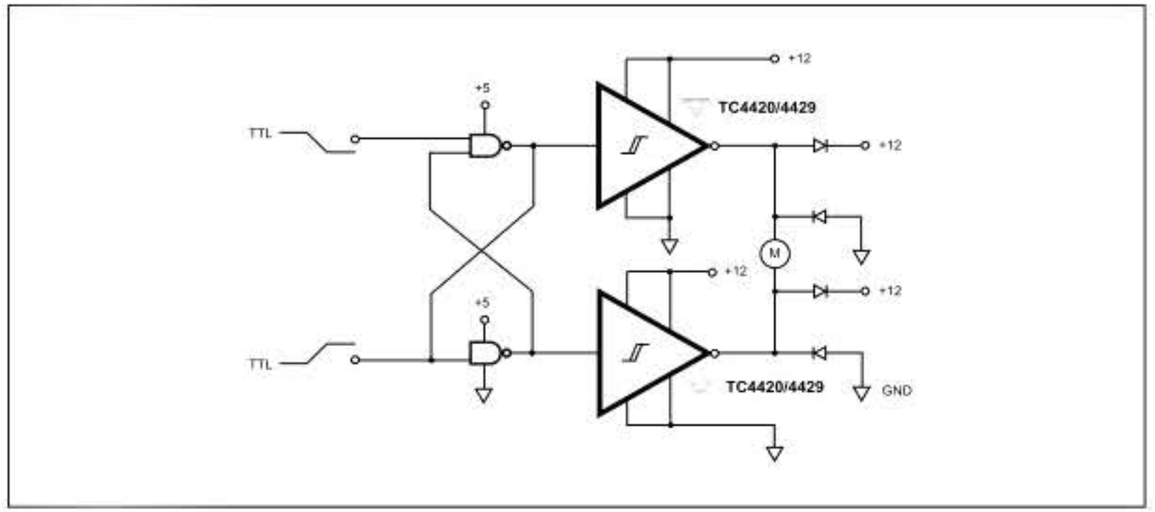
Warning Signal



Audio Oscillator



Motor Driver with Forward/Reverse and Lock Out



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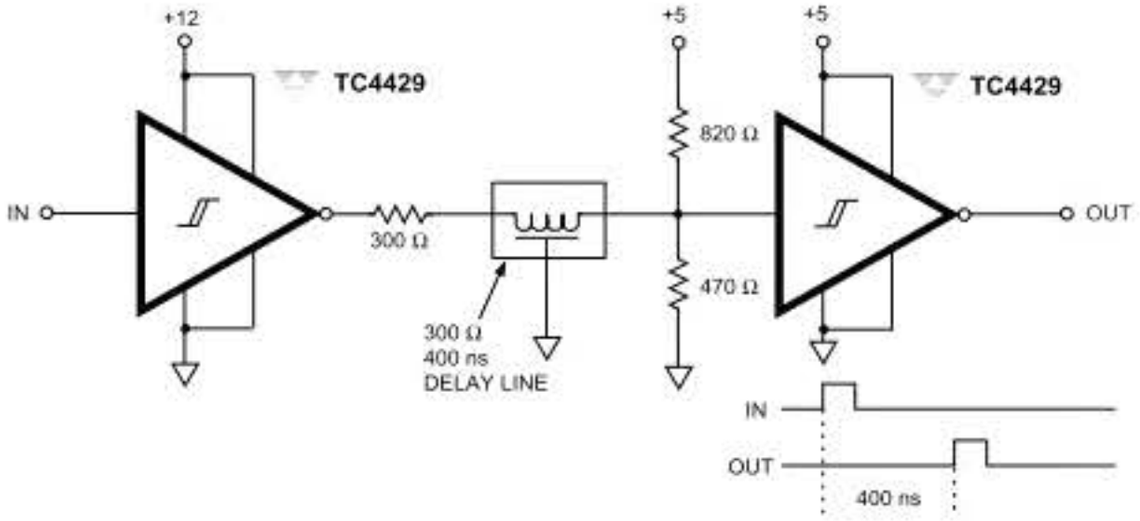
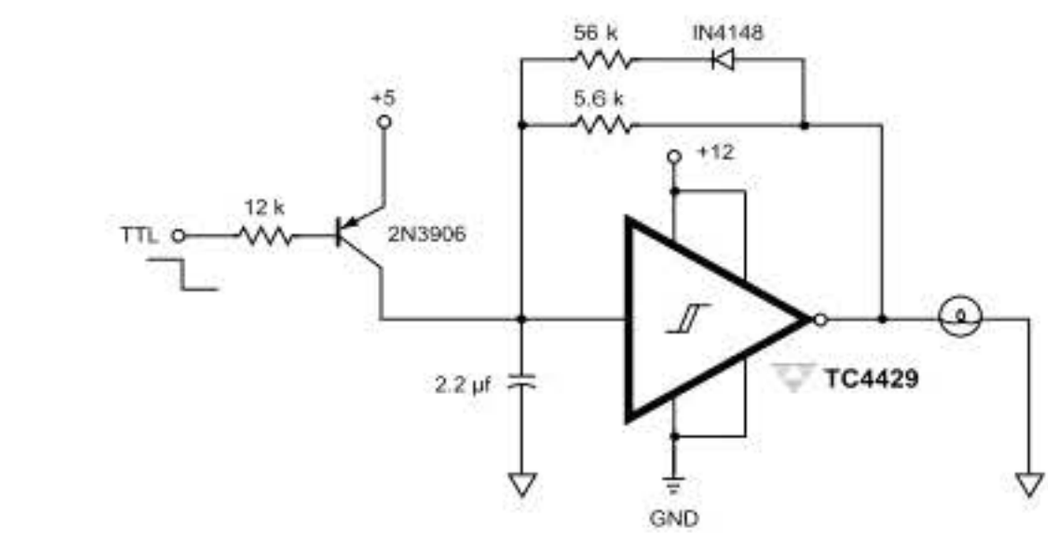
Delay Line Driver and Voltage Translator



TTL Controlled Light Flasher



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