TIMING DIAGRAMS

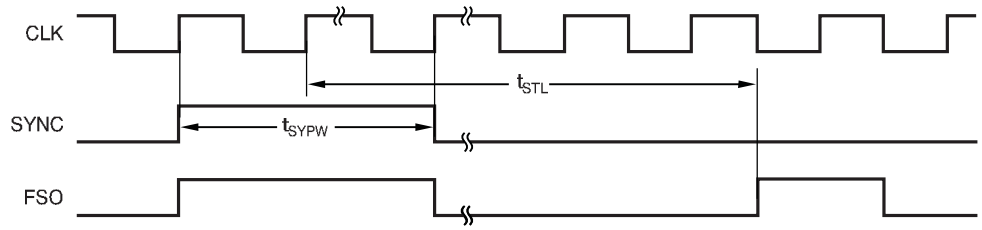

Figure 1. Initialization Timing

TIMING REQUIREMENTS

For T_A = –40°C to +85°C, DVDD = 2.7V to 3.6V, and IOVDD = 2.7V to 5.25V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SYPW}	SYNC positive pulse width	2		16	CLK periods
t_{STL}	Settling time of the ADS1601 (1)	51		52	Conversions
		816		832	

(1) An FSO pulse occuring prior to T_{STL} 816 CLK period should be ignored.

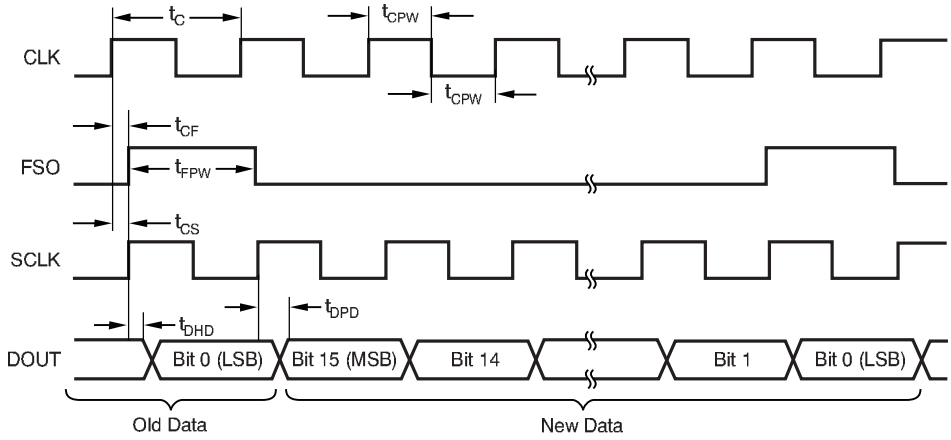

Figure 2. Data Retrieval Timing

TIMING REQUIREMENTS

For T_A = –40°C to +85°C, DVDD = 2.7V to 3.6V, and IOVDD = 2.7V to 5.25V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_C	CLK period ($1/f_{CLK}$)	50			ns
t_{CPW}	CLK positive or negative pulse width	25			ns
t_{CF}	Rising edge of CLK to rising edge of FSO			15	ns
t_{FPW}	FSO positive pulse width		1		CLK period
t_{CS}	Rising edge of CLK to rising edge of SCLK			15	ns
t_{DHD}	SCLK rising edge to old DOUT invalid (hold time)	0			ns
t_{DPD}	SCLK rising edge to new DOUT valid (propagation delay)			5	ns

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