Analysis, Design, and Performance Evaluation of Asymmetrical Half-Bridge Flyback Converter for Universal-Line-Voltage-Range Applications

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Abstract – **The asymmetrical half-bridge (AHB) flyback converter is an attractive topology for operation at higher switching frequencies because it can operate with zero-voltage switching of the primary-side switches and zero-current switching of the secondary-side rectifier. In this paper, a detailed analysis and design procedure of the AHB flyback converter for the universal-line-voltage-range applications is presented. The performance of the AHB flyback converter is evaluated by loss analysis based on the simulation waveforms obtained in Simplis and experimentally verified on a laboratory prototype of a 65-W (19.5-V, 3.33-A) universal-line-voltage-range adapter.**

I. Introduction

The increasing demand for size reduction of today's external power supplies such as adapters/chargers for laptops, tablets, mobile devices, game consoles, printers, etc., has continued to drive substantial development and research efforts in high-efficiency and high-power-density power conversion. As the silicon-based devices approach their theoretical performance limit, their ability to improve the performance of the next generation of power supplies is diminished. The emerging wide-band-gap devices, such as GaN-based devices, will inevitably bring about future significant incremental efficiency improvements. Generally, GaN MOSFETs have considerably lower gate charge and lower output capacitance than Si MOSFETs and, therefore, they have a good potential for operation at higher switching frequencies and, consequently, for size reduction of the power supplies [1]-[4].

In low-power offline applications, the flyback topology is the mostly used topology due to its simplicity and low cost. To achieve high efficiency at higher switching frequencies, the circuit parasitic components, such as the leakage inductance of the flyback transformer, should be exploited to play an active role in the circuit operation. Two flyback topologies enable efficient recycling of the leakage energy in the flyback transformer: the active-clamp (ACL) flyback [5]-[10] and the asymmetrical half-bridge (AHB) flyback [11]-[16]. Both ACL and AHB flyback topologies can operate with zero-voltage switching (ZVS) of the primary-side switches and zero-current switching (ZCS) of the secondary-side rectifier (diode rectifier or synchronous rectifier). Design and performance evaluation of the ACL flyback converter for the universal line-voltage range (90-264 Vrms) were already reported in the literature [7]-[9]. However, design and evaluation of the AHB flyback converter were presented only at constant input voltages [11]-[14] or at narrow line-voltage ranges [15], [16].

In this paper, a detailed analysis and design procedure of the AHB flyback converter for the universal line-voltage range is provided. The analysis of operation is illustrated by simulation waveforms obtained in Simplis. Detailed derivation of design equations is also provided. The performance of the AHB flyback converter is evaluated on a laboratory prototype of a 65-W (19.5-V, 3.33-A) universal-line-voltage-range adapter.

II. Analysis of Operation

The circuit diagram of the AHB flyback converter is shown in Fig. 1. It should be noted that in ac/dc applications the AHB converter in Fig. 1 is proceeded by the front-end stage consisting of the line-voltage rectifier and also power-factor-correction (PFC) circuit, if necessary.

In Fig. 1, the resonant inductor L_r includes the leakage inductance of the flyback transformer Tr. It should be noted that the circuit after the half bridge that is connected in parallel to the bottom switch of the half bridge can also be connected in parallel to the upper switch of the half bridge. In both cases, the operation of the circuit is identical. Key waveforms that illustrate the operation of the circuit in Fig. 1 are shown in Fig. 2. It can be recognized that the operation of the circuit in one switching cycle T_{sw} can be divided in seven subintervals, as shown in Figs. 2-4. The corresponding subtopologies are presented in Fig. 5. It should be noticed that secondary-side rectifier SR conducts only during subintervals $[T_3–T_4]$ and $[T_4–T_5]$.

A new switching cycle starts at instant $t = T_0$, when switch S_1 is turned on. During subinterval $[T_0–T_1]$, from the circuit equations

$$(L_m + L_r)\frac{di_{Lr}}{dt} = V_{in} - v_{Cr} \qquad (1)$$

and

$$C_r\frac{dv_{Cr}}{dt} = i_{Lr} \quad , \qquad (2)$$

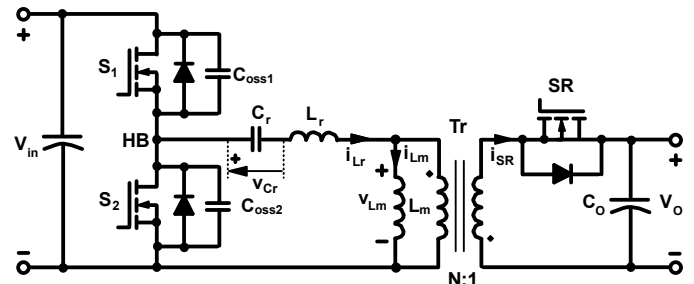the resonant-inductor current i_{Lr} and resonant capacitor voltage v_{Cr} can be determined as [17],
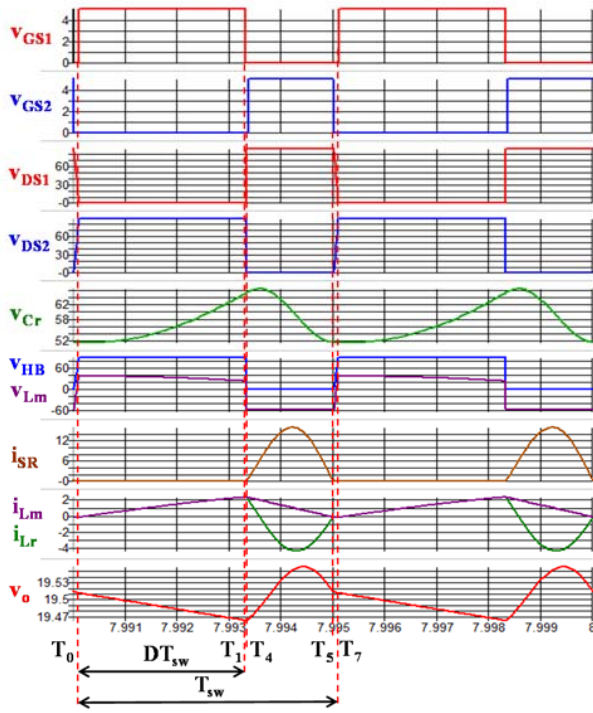

Fig. 1. Circuit diagram of AHB flyback converter.

Fig. 2. Key waveforms that illustrate operation of AHB flyback converter.

Fig. 3. Waveforms from Fig. 1 expanded between instants T_1 and T_4 .

$$i_{Lr}(t) = i_{Lr}(T_0) \cdot \cos[\omega_{r1}(t - T_0)] + \frac{V_{in} - v_{Cr}(T_0)}{Z_{r1}} \sin[\omega_{r1}(t - T_0)] \quad (3)$$

and

$$v_{Cr}(t) = V_{in} - [V_{in} - v_{Cr}(T_0)] \cdot \cos[\omega_{r1}(t - T_0)] + Z_{r1} i_{Lr}(T_0) \cdot \sin[\omega_{r1}(t - T_0)], (4)$$

where

$$\omega_{r1} = \frac{1}{\sqrt{(L_m + L_r) C_r}} \quad (5)$$

and

$$Z_{r1} = \sqrt{\frac{L_m + L_r}{C_r}} \quad . \quad (6)$$

Taking into account that $i_{Lr}(T_0) \approx 0$ (see Fig. 1), (3) and (4) can be simplified as

$$i_{Lr}(t) = \frac{V_{in} - v_{Cr}(T_0)}{Z_{r1}} \sin[\omega_{r1}(t - T_0)] \quad (7)$$

and

$$v_{Cr}(t) = V_{in} - [V_{in} - v_{Cr}(T_0)] \cdot \cos[\omega_{r1}(t - T_0)] \quad . \quad (8)$$

Equations (7) and (8) can be further simplified if resonant capacitor voltage v_{Cr} is approximated with its average value during a switching cycle, i.e.,

$$v_{Cr}(t) \approx v_{Cr,avg(T_{sw})} = v_{HB,avg(T_{sw})} = DV_{in} \quad . \quad (9)$$

With approximation in (9), the approximated resonant-inductor current i_{Lr} can be directly obtained from (1) as

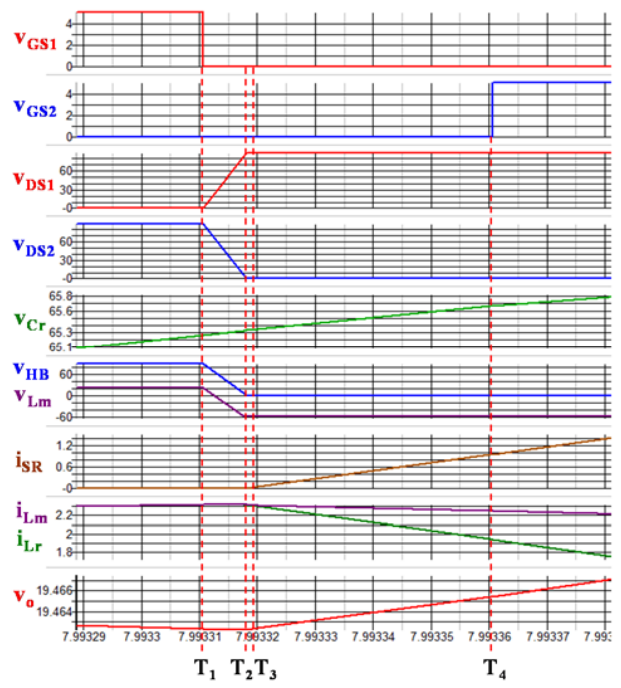$$i_{Lr}(t) \approx \frac{V_{in}(1 - D)}{L_m + L_r} \cdot (t - T_0) \quad . \quad (10)$$

During subinterval $[T_0–T_1]$, the primary voltage of transformer Tr, v_{Lm}, is positive (see Fig. 1), i.e., the secondary voltage of the transformer is negative and, therefore, the secondary-side rectifier does not conduct.

At instant $t = T_1$, switch S_1 turns off. During subinterval $[T_1–T_2]$, voltage $v_{HB} = v_{DS2}$ linearly decreases from V_{in} to zero, i.e.,

$$v_{HB}(t) = v_{DS2}(t) = V_{in} - \frac{i_{Lr}(T_1)}{C_{oss1} + C_{oss2}} \cdot (t - T_1) \quad , \quad (11)$$

and voltage v_{Lm} becomes negative, i.e., the secondary voltage of the transformer becomes positive, but lower than output voltage V_o. Therefore, the secondary-side rectifier does not conduct.

At instant $t = T_2$, the body diode of switch S_2 starts to conduct. During subinterval $[T_2–T_3]$, voltage v_{Cr} slightly increases and, consequently, the secondary voltage of transformer increases, but it is still smaller than output voltage V_o and the secondary-side rectifier does not conduct.

At instant $t = T_3$, the secondary voltage of the transformer increases to the output voltage V_o and the secondary-side rectifier starts to conduct. Therefore, the primary voltage of the transformer becomes $v_{Lm} = -NV_o$.

During subinterval $[T_3–T_4]$, from the circuit equations

$$L_r \frac{di_{Lr}}{dt} = NV_o - v_{Cr} \quad (12)$$

and

$$C_r \frac{dv_{Cr}}{dt} = i_{Lr} \quad , \quad (13)$$

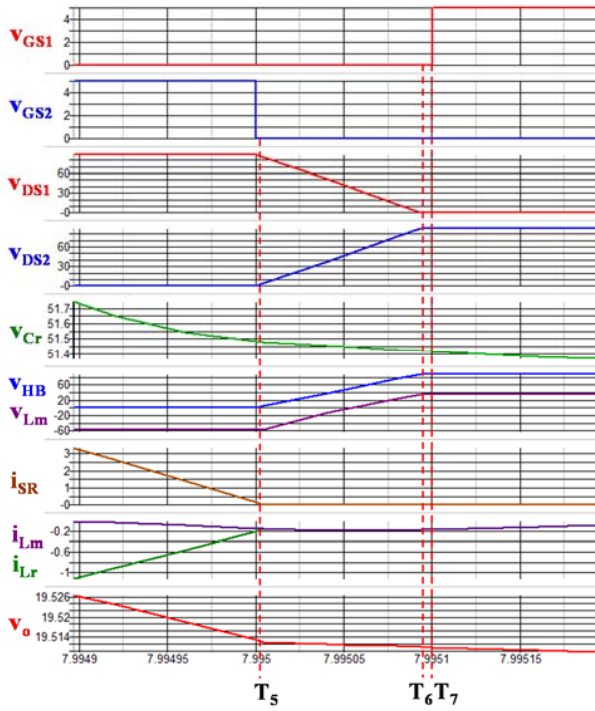the resonant-inductor current i_{Lr} and resonant capacitor voltage v_{Cr} can be determined as [17],

Fig. 4. Waveforms from Fig. 1 expanded between instants T_5 and T_7.

Fig. 5 Equivalent subtopologies corresponding to subintervals (a) [T_0-T_1], (b) [T_1-T_2], (b) [T_2-T_3], (d) [T_3-T_4], (e) [T_4-T_5], (f) [T_5-T_6], and (g) [T_6-T_7].

$$i_{Lr}(t) = i_{Lr}(T_3) \cdot \cos[\omega_{r2}(t-T_3)] + \frac{NV_o - v_{Cr}(T_3)}{Z_{r2}}\sin[\omega_{r2}(t-T_3)] \quad (14)$$

and

$$v_{Cr}(t) = NV_o - [NV_o - v_{Cr}(T_3)] \cdot \cos[\omega_{r2}(t-T_3)] + Z_{r2}\, i_{Lr}(T_3) \cdot \sin[\omega_{r2}(t-T_3)], \quad (15)$$

where

$$\omega_{r2} = \frac{1}{L_r C_r} \quad (16)$$

and

$$Z_{r2} = \sqrt{\frac{L_r}{C_r}} \quad . \quad (17)$$

Equations (14) and (15) can be further derived as

$$i_{Lr}(t) = -I_{Lr,m}\sin[\omega_{r2}(t-T_3) - \theta_2] \quad (18)$$

and

$$v_{Cr}(t) = NV_o + V_{Cr,m}\cos[\omega_{r2}(t-T_3) - \theta_2] \quad , \quad (19)$$

where

$$I_{Lr,m} = \sqrt{[i_{Lr}(T_3)]^2 + \left[\frac{NV_o - v_{Cr}(T_3)}{Z_{r2}}\right]^2} \quad , \quad (20)$$

$$V_{Cr,m} = Z_{r2}\, I_{Lr,m} \quad , \quad (21)$$

and

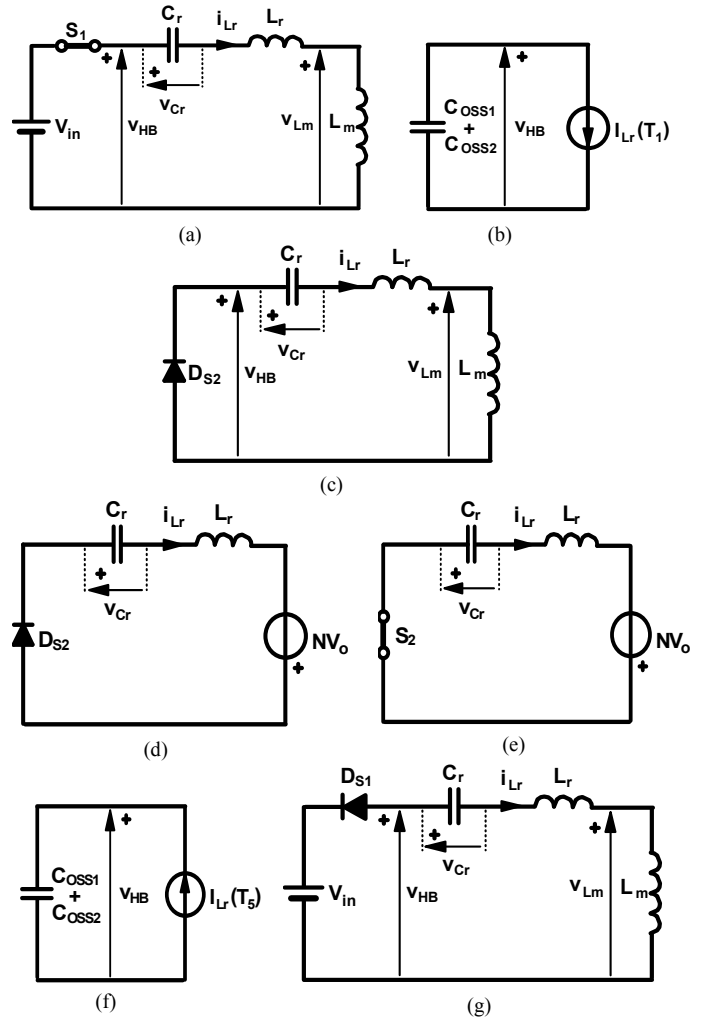$$\tan(\theta_2) = -\frac{Z_{r2}\, i_{Lr}(T_3)}{NV_o - v_{Cr}(T_3)} \quad . \quad (22)$$

At instant $t = T_4$, switch S_2 turns on with ZVS. During subinterval [T_4–T_5], the waveform of resonant-inductor current i_{Lr} and resonant capacitor voltage v_{Cr} follows Eqs. (18) and (19), respectively. At instant $t = T_5$, the secondary-side rectifier current decreases to zero and the rectifier turns off with ZCS. As a result, at $t = T_5$, $i_{Lr} = i_{Lm}$. At the same instant $t = T_5$, switch S_2 turns off.

It should be noted that if the secondary-side rectifier is a synchronous rectifiers SR, the conduction angle of SR is slightly smaller than the interval [T_3–T_5].

To better illustrate the operation of the circuit during the conduction interval of the secondary-side rectifier, [T_3–T_5], the waveforms of the resonant-inductor current i_{Lr} and resonant capacitor voltage v_{Cr} are redrawn with more details in Fig. 6.

During subinterval [T_5–T_6], voltage $v_{HB} = v_{DS2}$ linearly increases from zero to V_{in}, i.e.,

$$v_{HB}(t) = v_{DS2}(t) = \frac{i_{Lr}(T_5)}{C_{oss1} + C_{oss2}} \cdot (t - T_5) \quad , \quad (23)$$

whereas, voltage v_{DS1} linearly decreases from V_{in} to zero.

At instant $t = T_6$, the body diode of switch S_1 starts to conduct. Shortly after $t = T_6$, at instant $t = T_7$, switch S_1 turns on with ZVS and the new switching cycle starts.

It should be noted that the implementation of the operation of the AHB flyback converter for a wide input-voltage range requires operation with variable switching frequency. In simulations, the control circuit with variable switching frequency is implemented with voltage-mode control and by sensing the zero crossing of the secondary-side rectifier current.

III. DESIGN AND IMPLEMENTATION

The design procedure is illustrated on the example of a 65-W (19.5-V, 3.33-A) adapter for the universal line-voltage range (90-264 Vrms). Assuming a 120-μF bulk capacitor and 96% full-load efficiency of the AHB flyback dc/dc converter, the 90-264-Vrms line-voltage range corresponds to the rectified voltage range at the input of the AHB flyback converter from $V_{in,min} = 87.5$ V to $V_{in,max} \approx 375$ V. In this design, it is assumed that the minimum switching frequency that occurs at the minimum input voltage and full load is 200 kHz.

Design equations are derived starting from the volt-second balance of the flyback transformer,

$$(1-D)T_{sw}NV_o = \frac{L_m}{L_m + L_r} \int_{DT_{sw}} (V_{in} - v_{Cr})\, dt \quad . \quad (24)$$

where, $N = N_P/N_S$ is the turns ratio of the transformer. The right-hand side of (24) can be further expressed as

$$\frac{L_m}{L_m + L_r}\left(V_{in} DT_{sw} - \int_{DT_{sw}} v_{Cr}\, dt \right) = \frac{L_m}{L_m + L_r} D(1-D)V_{in}T_{sw}, \quad (25)$$

where, it is taken into account that the average voltage v_{Cr} during DT_{sw} is approximately equal to the average voltage v_{Cr} during T_{sw}, as it can be observed in Fig. 2, i.e.,

$$\int_{DT_{sw}} v_{Cr}\, dt = v_{Cr,avg(DT_{sw})} \approx v_{Cr,avg(T_{sw})} = D^2 V_{in}T_{sw} \quad . \quad (26)$$

It follows from (24) and (25) that the duty cycle D is

$$D = \frac{L_m + L_r}{L_m} \cdot \frac{NV_o}{V_{in}} \approx \frac{NV_o}{V_{in}} \quad , \text{ if } L_m \gg L_r \quad . \quad (27)$$

The voltage stress on the secondary-side rectifier is

$$V_{SR} = \frac{(1-D)V_{in}}{N} + V_o = \frac{V_{in}}{N} \quad . \quad (28)$$

The first design step is the selection of transformer turns ratio N. For lower voltage stress on the secondary-side rectifier, N should be as large as possible. However, N is limited by maximum duty cycle D_{max} at $V_{in,min}$. In fact, as the secondary-side current flows only during the $(1-D)T_{sw}$ interval, D_{max} has to be limited, typically, below 0.7 to 0.8. For $D_{max} = 0.7$ and $D_{max} = 0.8$, $N = 3.14$ and $N = 3.59$, respectively. In this design, $N = 3.5$ is selected, which results in $D_{max} = 0.78$ and $V_{SR,max} = 107$ V.

The second design step is the selection of the magnetizing inductance L_m of the transformer. From the waveform of the magnetizing current i_{Lm} in Fig. 2, the peak and valley values of i_{Lm} during a switching cycle can be obtained as

$$I_{Lm,peak} = I_{Lm,avg} + \frac{\Delta I_{Lm}}{2} = \frac{I_o}{N} + \frac{NV_o}{2L_m}(1-D)T_{sw} \quad (29)$$

and

$$I_{Lm,valley} = I_{Lm,avg} - \frac{\Delta I_{Lm}}{2} = \frac{I_o}{N} - \frac{NV_o}{2L_m}(1-D)T_{sw}, \quad (30)$$

respectively. The average value of i_{Lm} during a switching cycle, $I_{Lm,avg} = I_o/N$ in (29) and (30), can be derived as follows.

$$
\begin{aligned}
I_o T_{sw} &= \int_{T_{sw}} i_{SR}\, dt = N \int_{T_{sw}} (i_{Lm} - i_{Lr})\, dt \\
&= N\left(\int_{T_{sw}} i_{Lm}\, dt - \int_{T_{sw}} i_{Lr}\, dt \right) = N I_{Lm,avg} T_{sw}
\end{aligned} \quad , \quad (31)
$$

where, it is taken into account that the average value of the resonant current i_{Lr} during a switching cycle is equal to zero.

For ZVS turn-on of switch S_1, the valley value of the magnetizing current has to be negative, $I_{Lm,valley} < 0$. Therefore, using (30), the magnetizing inductance is obtained as

$$L_m < \frac{N^2 V_o (1 - D_{max})}{2 I_{o,max} f_{sw}} = 39.4\,\mu\text{H} \quad . \quad (32)$$

After a few iterations of Simplis simulations for ZVS turn-on of switch S_1, $L_m = 36$ μH is selected.

The third design step is the selection of the components of the series resonant circuit L_r-C_r. During the conduction interval of the secondary-side rectifier, the waveforms of the resonant-inductor current i_{Lr} and resonant capacitor voltage v_{Cr}, shown in Fig. 6, are determined by Eqs. (16)-(22). According to the current waveforms in Fig. 6, the average value of current i_{SR} during a switching cycle can be expressed as

$$
\begin{aligned}
I_o T_{sw} &= \int_{T_{sw}} i_{SR}\, dt = N \int_{T_{sw}} (i_{Lm} - i_{Lr})\, dt \\
&= N \int_{(1-D)T_{sw}} (i_{Lm} - i_{Lr})\, dt = N\left[\frac{i_{Lr}(T_3)\cdot T_{r2}}{4} + \frac{I_{Lr,m}\cdot T_{r2}}{\pi} \right]
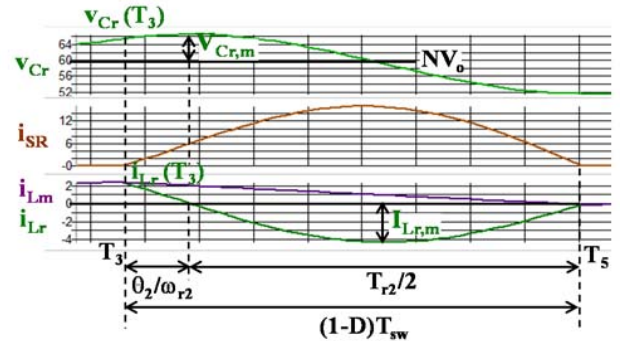\end{aligned} \quad , \quad (33)
$$

Fig. 6. Waveforms of resonant-inductor current i_{Lr} and resonant-capacitor voltage v_{Cr} during conduction interval of secondary-side rectifier.

where, it is recognized that the area enclosed by the difference of currents i_{Lm}-i_{Lr} in interval $(1-D)T_{sw}$ can be approximated as the sum of a triangle and a half sine wave. In (20) and (22), current $i_{Lr}(T_3)$ is equal to the peak value of the magnetizing current determined by (29), whereas, current $I_{Lr,m}$ can be obtained from (18) as

$$I_{Lr,m} = \frac{i_{Lr}(T_3)}{\sin(\theta_2)} \quad . \tag{34}$$

Angle θ_2 in (34) can be obtained by observing Fig. 6 as

$$\theta_2 = 2\pi \left[(1-D)\frac{T_{sw}}{T_{r2}} - \frac{1}{2} \right] \quad . \tag{35}$$

Combining (33)-(35), the following relationship can be obtained

$$\frac{i_{Lr}(T_3)}{\pi \cdot \sin\left\{ 2\pi \left[(1-D)\frac{T_{sw}}{T_{r2}} - \frac{1}{2} \right] \right\}} = \frac{I_o}{N} \cdot \frac{T_{sw}}{T_{r2}} - \frac{i_{Lr}(T_3)}{4} \quad . \tag{36}$$

Using (36), resonant period T_{r2} is obtained as $T_{r2} = 1.947$ μs. The value of L_r is typically 1%-2% of L_m. For example, selecting $L_r = 2\%$ of L_m, i.e. $L_r = 0.72$ μH, C_r is obtained as

$$C_r = \frac{T_{r2}^2}{4\pi^2 L_r} = 133 \text{ nF} \quad . \tag{37}$$

After ZVS design optimization in Simplis, $C_r = 180$ nF is selected.

The transformer is implemented by using planar core EQ25/LPT (3C96) with 6-layer PCB winding (7 primary turns sandwiched between 2 secondary turns. The measured leakage inductance of the transformer is $L_{lk} = 1.4\%$ of L_m, i.e. $L_r = 0.5$ μH, which is smaller than the value of $L_r = 0.72$ μH used in the simulations. Therefore, resonant capacitor C_r is implemented with an increased capacitance of 270 nF.

The primary-side switches are implemented with TPH3206 (600V, 150 mΩ) GaN HEMT devices from Transphorm and the secondary-side rectifier is implemented with BSC093N15 (150V, 9.3 mΩ) MOSFET from Infineon.

IV. LOSS ANALYSIS

The loss analysis includes the conduction and gate-drive losses of primary-side switches and secondary-side rectifier, winding and core losses of the transformer, and ESR-loss of the output filter capacitor at full load. Due to ZVS-turn-on of primary-side switches and, generally, low turn-off switching loss of GaN devices [4], the switching losses of primary-side switches can be neglected. Due to ZCS, the switching losses of secondary-side rectifier can be also neglected.

All conduction losses are calculated by using rms values of relevant currents obtained with Simplis simulations. The core loss of the transformer is calculated by using the core-loss calculation software from Ferroxcube [18], [19].

The circuit variables relevant for the loss calculations are summarized in Table I. In addition to the rms currents of primary-side switches S_1 and S_2, secondary-side synchronous rectifier SR, resonant inductor L_r, and output-filter capacitor C_o, Table I also includes the peak-to-peak value of the magnetizing inductor current, ΔI_{Lm}, the peak-to-peak value of the resonant capacitor voltage, ΔV_{Cr}, the peak-to-peak value of the magnetic flux density of the flyback transformer, ΔB, duty cycle D, and switching frequency f_{sw}. As shown in Table I, the switching frequency range for the input-voltage range of 87.5-375 V at full load is 200-457 kHz.

The breakdown of losses is summarized in Table II. It should be noted in Table II that the core loss of the flyback transformer significantly increases at higher input voltages. The calculated dc-dc efficiency from the output of the line-voltage rectifier to the load is also included in Table II and plotted in Fig. 7. It can be seen in Fig. 7 that the dc-dc efficiency decreases at higher input voltages, which is the result of the increased core loss of the transformer.

TABLE I – CIRCUIT VARIABLES RELEVANT FOR LOSS CALCULATION

V_{in} [V$_{dc}$]	87.5	170	325	375
$I_{S1,rms}$[A]	1.07	0.81	0.603	0.56
$I_{S2,rms}$[A]	1.82	1.29	1.474	1.5
$I_{Lr,rms}$[A]	2.1	1.53	1.606	1.617
$I_{SR,rms}$[A]	7.48	5.114	4.78	4.738
$I_{Co,rms}$[A]	6.7	3.874	3.415	3.366
ΔI_{Lm}[A]	2.34	2.94	3.215	3.257
ΔV_{cr}[V]	22	9.7	8.9	8.8
f_{sw}[kHz]	200	382	447	457
D	0.751	0.402	0.229	0.202
ΔB [mT]	134 $\binom{+115}{-19}$	169 $\binom{+140}{-29}$	184 $\binom{+149}{-35}$	187 $\binom{+150}{-37}$

TABLE II – BREAKDOWN OF LOSSES

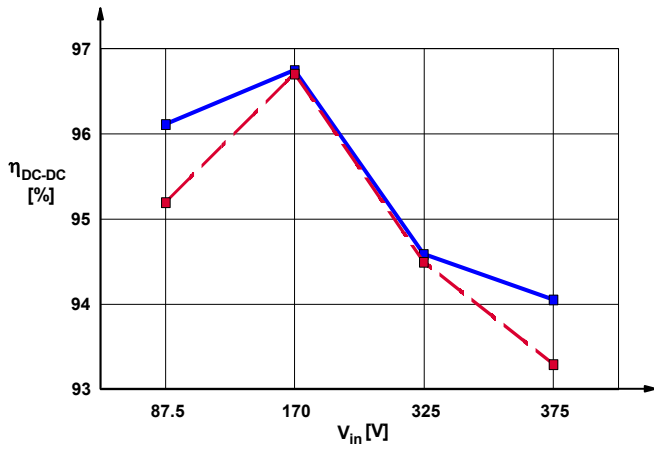| V_{in} [V$_{dc}$]	87.5	170	325	375
$P_{S1,cond}$ [mW]	258	148	82	71
$P_{S2,cond}$ [mW]	745	374	489	506
$P_{S1+S2,Qg}$ [mW]	30	57	67	68
$P_{SR,cond}$ [mW]	781	365	319	313
$P_{SR,Qg}$ [mW]	63	120	140	143
$P_{Co,esr}$ [mW]	180	60	47	45
P_{core} [mW]	157	856	2284	2736
$P_{cu,P}$ [mW]	132	70	77	78
$P_{Cu,S}$ [mW]	280	131	114	112
$P_{loss, Tr}$ [W]	0.569	1.057	2.475	2.926
$P_{loss, DC-DC}$ [W]	2.626	2.181	3.619	4.072
η_{DC-DC} [%]	96.12	96.75	94.73	94.11

Fig. 7 Calculated (solid line) and measured (dashed line) DC-DC efficiency at full load.

Fig. 8(b) Measured waveforms at V_{in}=170V and full load

V. EXPERIMENTAL RESULTS

Key measured waveforms at V_{in}=87.5 V, 170 V, 325 V, and 375 V, and full load are presented in Fig. 8. These waveforms nicely illustrate the ZVS turn-on of the primary-side switches, except at $V_{in,max}$ = 375 V, where switch S_1 turns on with a small voltage. The ZCS operation of the secondary-side synchronous rectifier can be also observed in Fig. 8. However, as shown in Fig. 8, the secondary-side synchronous rectifier current i_{SR} also contains current spikes at the turn-on and turn-off instants of the secondary-side rectifier, which is the result of the charging and discharging of the secondary-side rectifier parasitic capacitance, which was neglected in the simulations.

DC-DC efficiency measurements are shown in Fig. 7. The measured efficiency is in excellent agreement with the calculated efficiency at 170-V and 325-V input voltages. At $V_{in,min}$ = 87.5 V, the measured efficiency is lower than the measured efficiency due to the additional conduction losses in the transformer windings and terminations, which were neglected in the simulations. Finally, at $V_{in,max}$ = 375 V, the measured efficiency is slightly lower than the calculated efficiency, which is the result of the turn-on of switch S_1 with non-complete ZVS as shown in Fig. 8(d).
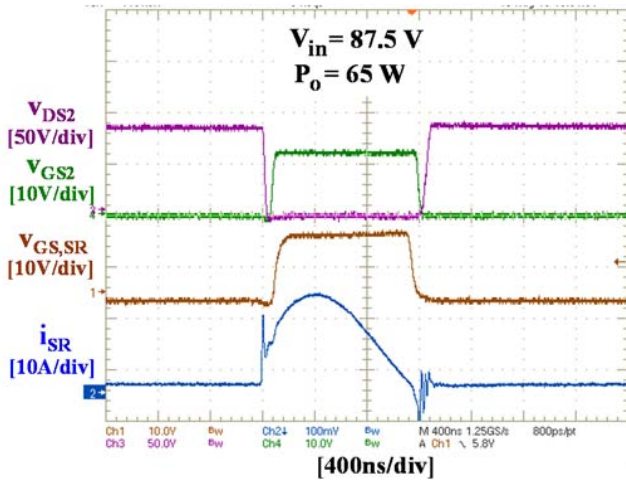

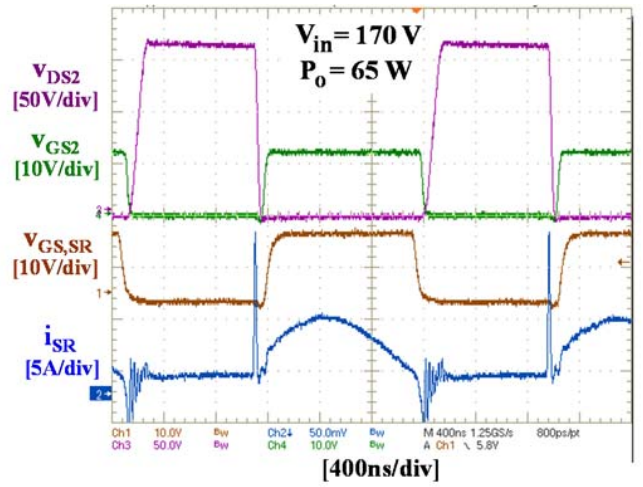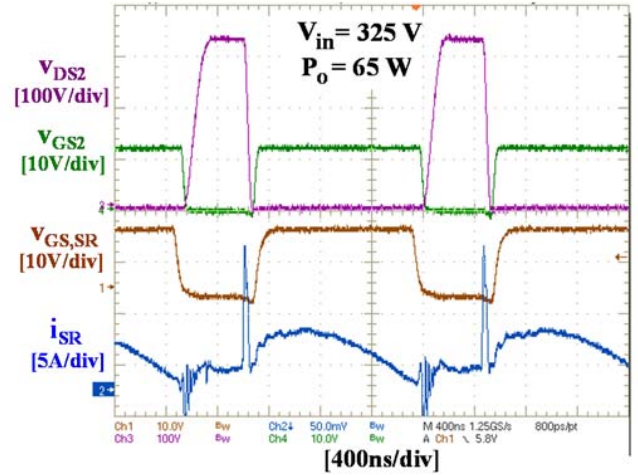Fig. 8(c) Measured waveforms at V_{in}=325V and full load.

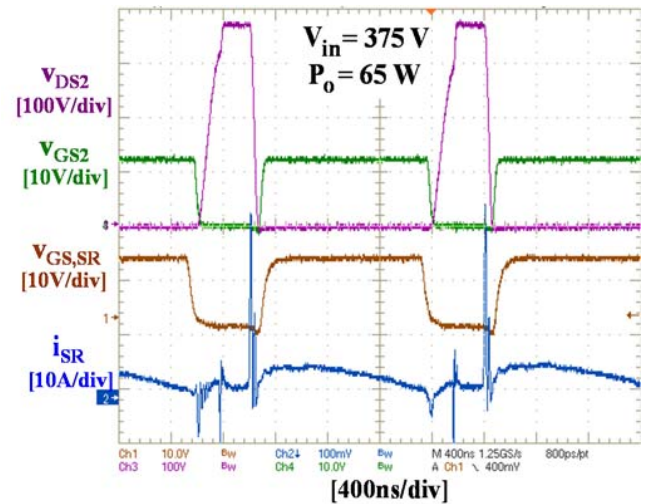Fig. 8(d) Measured waveforms at V_{in}=375V and full load.

Fig. 8(a) Measured waveforms at V_{in}=87.5V and full load.

The control circuit is implemented in open loop by generating the gate signals for the primary-side switches and the secondary-side synchronous rectifier through a DSP and a corresponding GUI software.

VI. SUMMARY

In this paper, a detailed analysis and design procedure of the AHB flyback converter for the universal line-voltage range is provided. The analysis of operation is illustrated by simulation waveforms obtained in Simplis. It is shown that the primary-side switches operate with zero-voltage switching (ZVS), whereas, the secondary-side rectifier operates with zero-current switching (ZCS), resulting in significantly reduced switching losses. The implementation of operation of the AHB flyback converter for a wide input-voltage range requires operation with variable switching frequency. In simulations, the control circuit is implemented with voltage-mode control and by sensing the zero crossing of the secondary-side rectifier current. Detailed derivation of design equations is also provided. The performance of the AHB flyback converter is evaluated by loss analysis based on simulation waveforms obtained in Simplis. The core loss of the transformer is calculated by using the core-loss calculation software from Ferroxcube [18]. It is shown that at higher input voltages, the core loss of the transformer significantly increases, resulting in reduced efficiency. Experimental waveforms and efficiency measurements obtained on a 65-W (19.5-V, 3.33-A) laboratory prototype of the AHB flyback converter for the universal-line-voltage range are also presented. The experimental control circuit is implemented in open loop by generating the gate signals for the primary-side switches and the secondary-side synchronous rectifier through a DSP and a corresponding GUI software.

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