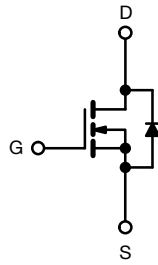
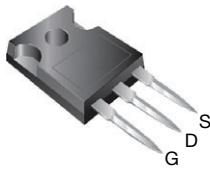


Power MOSFET

TO-247AC



N-Channel MOSFET

FEATURES

- Low figure-of-merit $R_{on} \times Q_g$
- 100 % avalanche tested
- High peak current capability
- dv/dt ruggedness
- Improved T_{rr}/Q_{rr}
- Improved gate charge
- High power dissipations capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.270
Q_g max. (nC)	76	
Q_{gs} (nC)	21	
Q_{gd} (nC)	34	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG20N50C-E3
Lead (Pb)-free and halogen-free	SiHG20N50C-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	500	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C) ^a	V_{GS} at 10 V	$T_C = 25$ °C	20	A
		$T_C = 100$ °C	11	
Pulsed drain current ^b	I_{DM}	80	A	
Linear derating factor		1.8	W/°C	
Single pulse avalanche energy ^c	E_{AS}	361	mJ	
Maximum power dissipation	P_D	250	W	
Reverse diode dv/dt ^d	dv/dt	5	V/ns	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For 10 s	300		

Notes

- Limited by maximum junction temperature
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.5$ mH, $R_g = 25$ Ω , $I_{AS} = 17$ A
- $I_{SD} \leq 18$ A, $di/dt \leq 380$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.5	



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.7	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.225	0.270	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 10 A	-	6.4	-	S
Dynamic						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	-	2451	2942	pF
Output capacitance	C _{oss}		-	300	360	
Reverse transfer capacitance	C _{rss}		-	26	32	
Total gate charge	Q _g	V _{GS} = 10 V, I _D = 18 A, V _{DS} = 400 V	-	65	76	nC
Gate-source charge	Q _{gs}		-	21	-	
Gate-drain charge	Q _{gd}		-	29	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 250 V, I _D = 18 A, R _g = 9.1 Ω	-	80	-	ns
Rise time	t _r		-	27	-	
Turn-off delay time	t _{d(off)}		-	32	-	
Fall time	t _f		-	44	-	
Gate input resistance	R _g	f = 1 MHz, open drain	-	1.1	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	20	A
Pulsed diode forward current	I _{SM}		-	-	80	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V	-	-	1.5	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S , di/dt = 100 A/μs, V _R = 35 V	-	503	-	ns
Reverse recovery charge	Q _{rr}		-	6.7	-	μC
Reverse recovery current	I _{RRM}		-	30	-	A

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

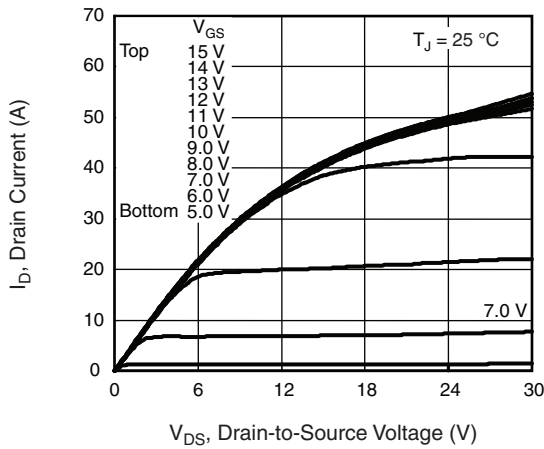


Fig. 1 - Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

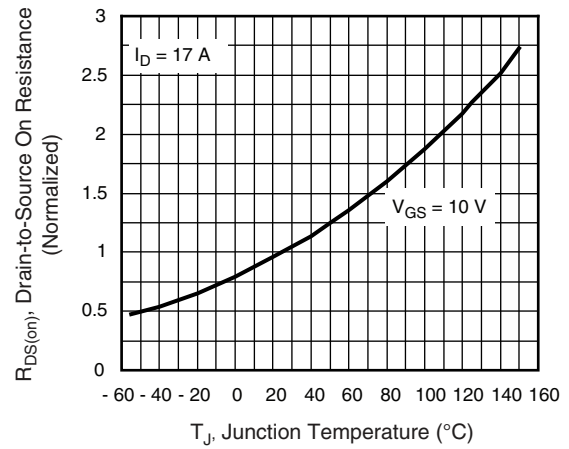


Fig. 4 - Normalized On-Resistance vs. Temperature

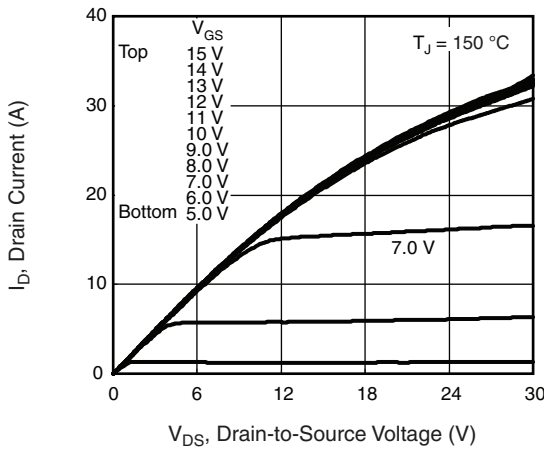


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

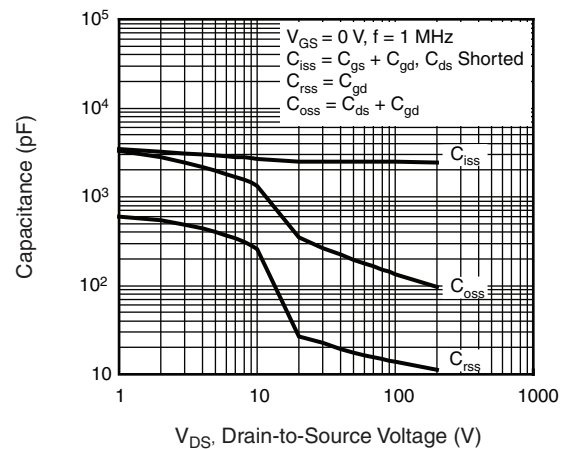


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

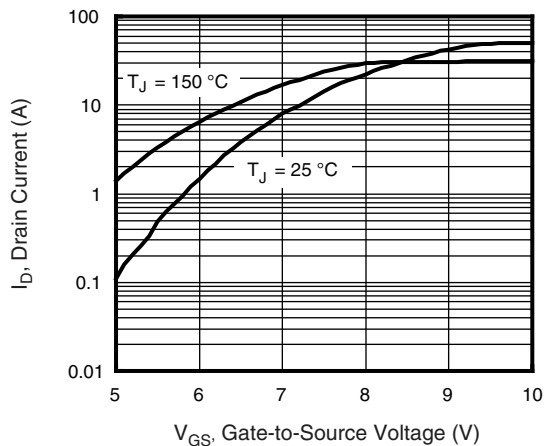


Fig. 3 - Typical Transfer Characteristics

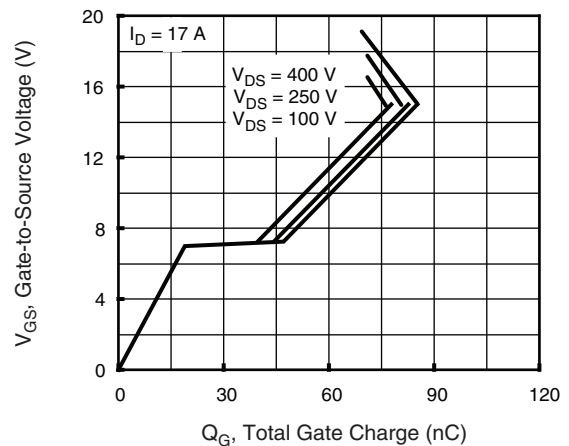


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

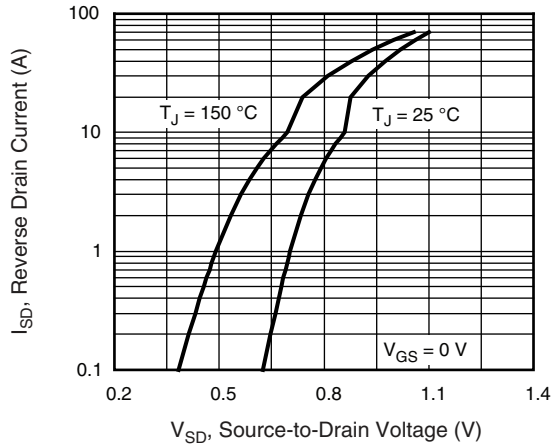


Fig. 7 - Typical Source-Drain Diode Forward Voltage

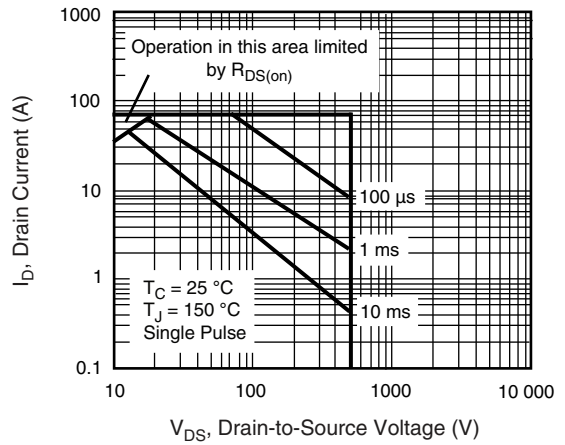


Fig. 8 - Maximum Safe Operating Area

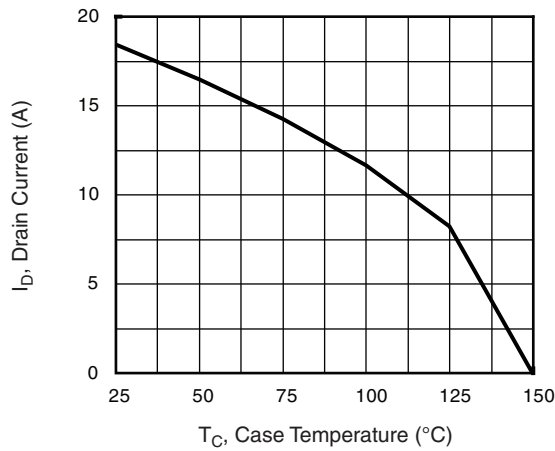


Fig. 9 - Maximum Drain Current vs. Case Temperature

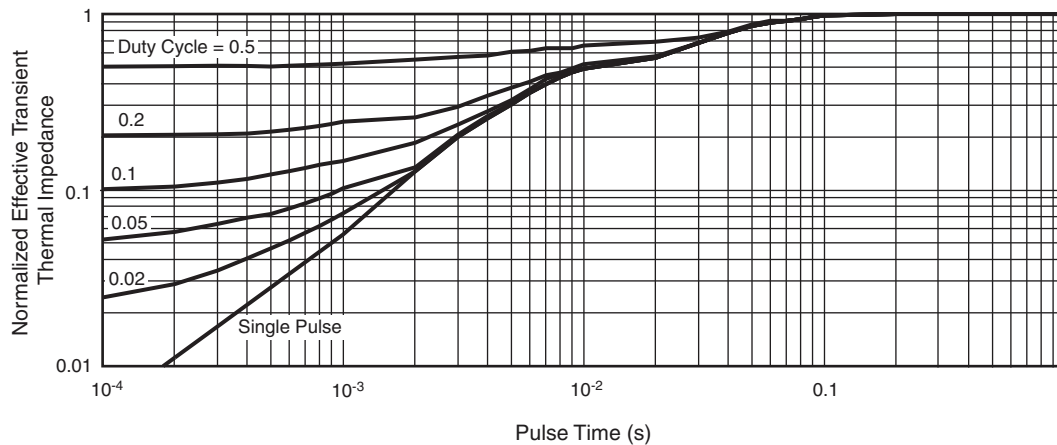


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (TO-247)

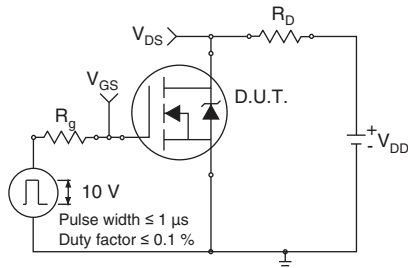


Fig. 11 - Switching Time Test Circuit

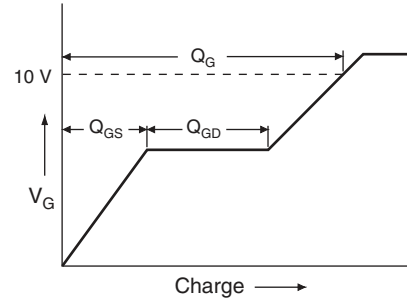


Fig. 15 - Basic Gate Charge Waveform

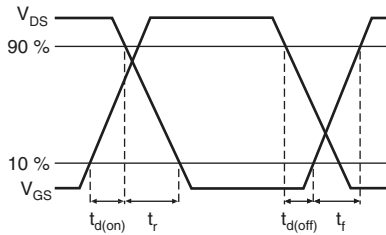


Fig. 12 - Switching Time Waveforms

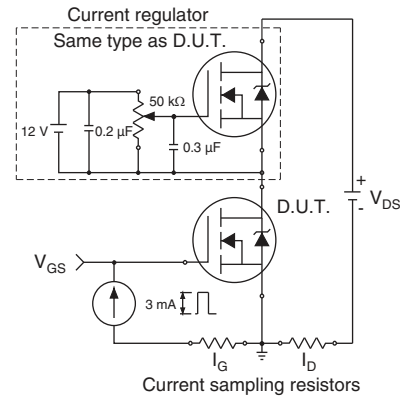


Fig. 16 - Gate Charge Test Circuit

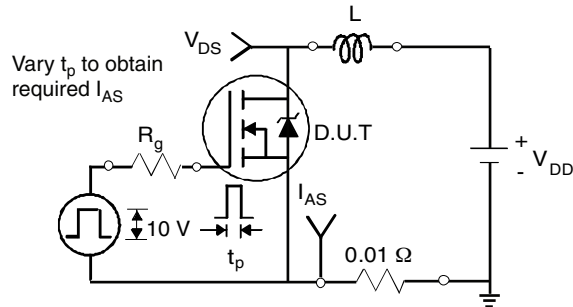


Fig. 13 - Unclamped Inductive Test Circuit

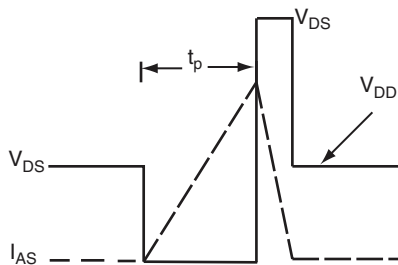
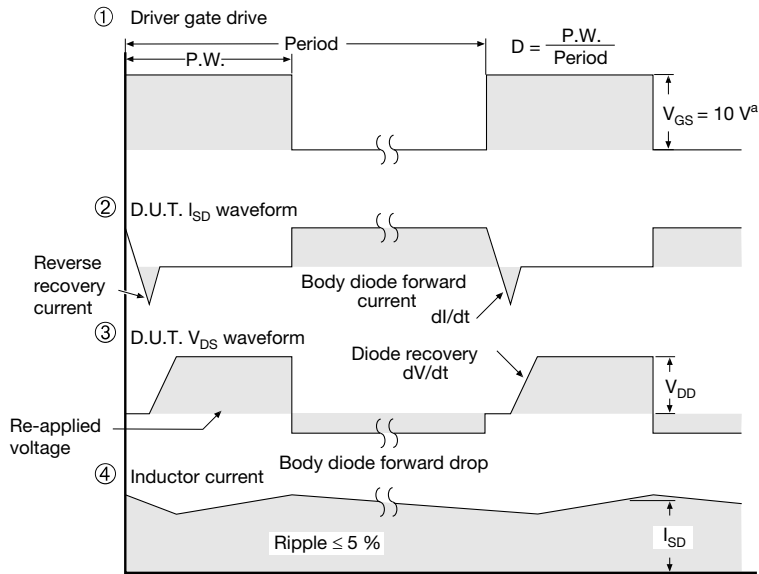
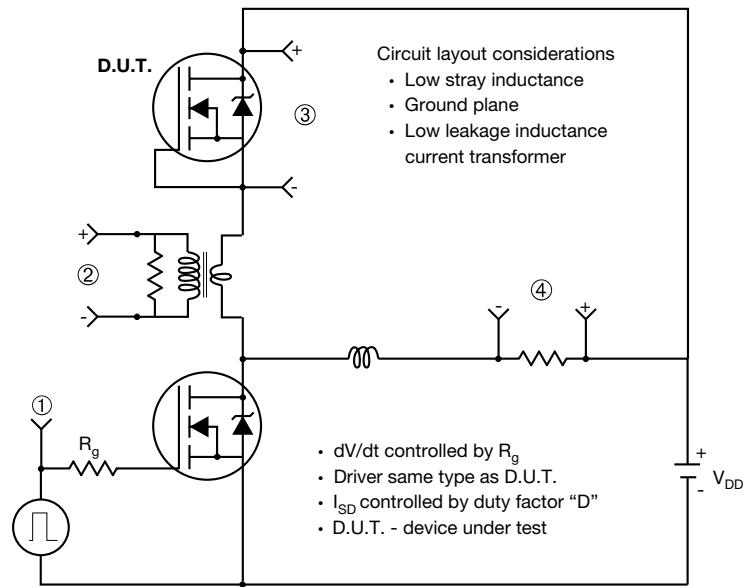


Fig. 14 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 17 - For N-Channel

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TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.





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