

Preliminary TOSHIBA CCD Image Sensor CCD (charge coupled device)

TCD2905CF

The TCD2905CF is a high sensitive and low dark current 5400 elements \times 6 line CCD color image sensor which includes CCD drive circuit and clamp circuit. The sensor is designed for scanner.

The device contains a row of 5400 elements \times 6 line staggered photodiodes which provide a 48 lines/mm (1200 dpi) across a A4 size paper. The device is operated by 5 V pulse and 12 V power supply.

Features

- Number of Image Sensing Elements: 5400 elements \times 6 line
- Image Sensing Element Size: 5.25 μ m by 5.25 μ m on 5.25 μ m
- Photo Sensing Region: High sensitive and low dark current PN photodiode
- Distanced Between Photodiode Array: 63 μ m (12 lines) R array – G array, G array – B array
10.5 μ m (2 lines) Odd array – Even array
- Clock: 2 phase (5 V)
- Power Supply: 12 V Power Supply Voltage
- Internal Circuit: Clamp Circuit
- Package: 22 pin Cerdip Package
- Color Filter: Red, Green, Blue

Maximum Ratings (Note1)

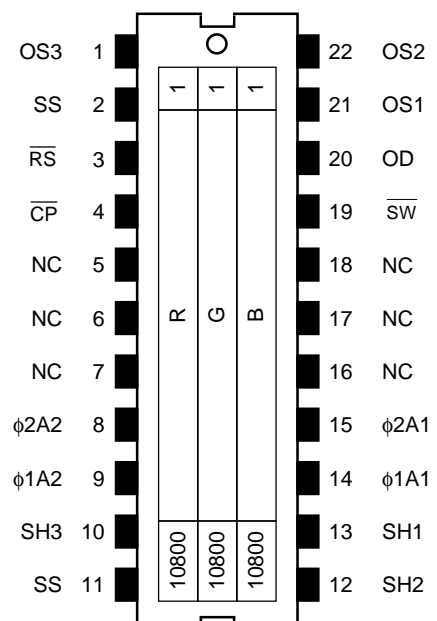
Characteristic	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi A}$	-0.3~8.0	V
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
Switch pulse voltage	V_{SW}		
Power supply voltage	V_{OD}	-0.3~15	V
Operating temperature	T_{opr}	0~60	°C
Storage temperature	T_{stg}	-25~85	°C

Note 1: All voltage are with respect to SS terminals (ground).

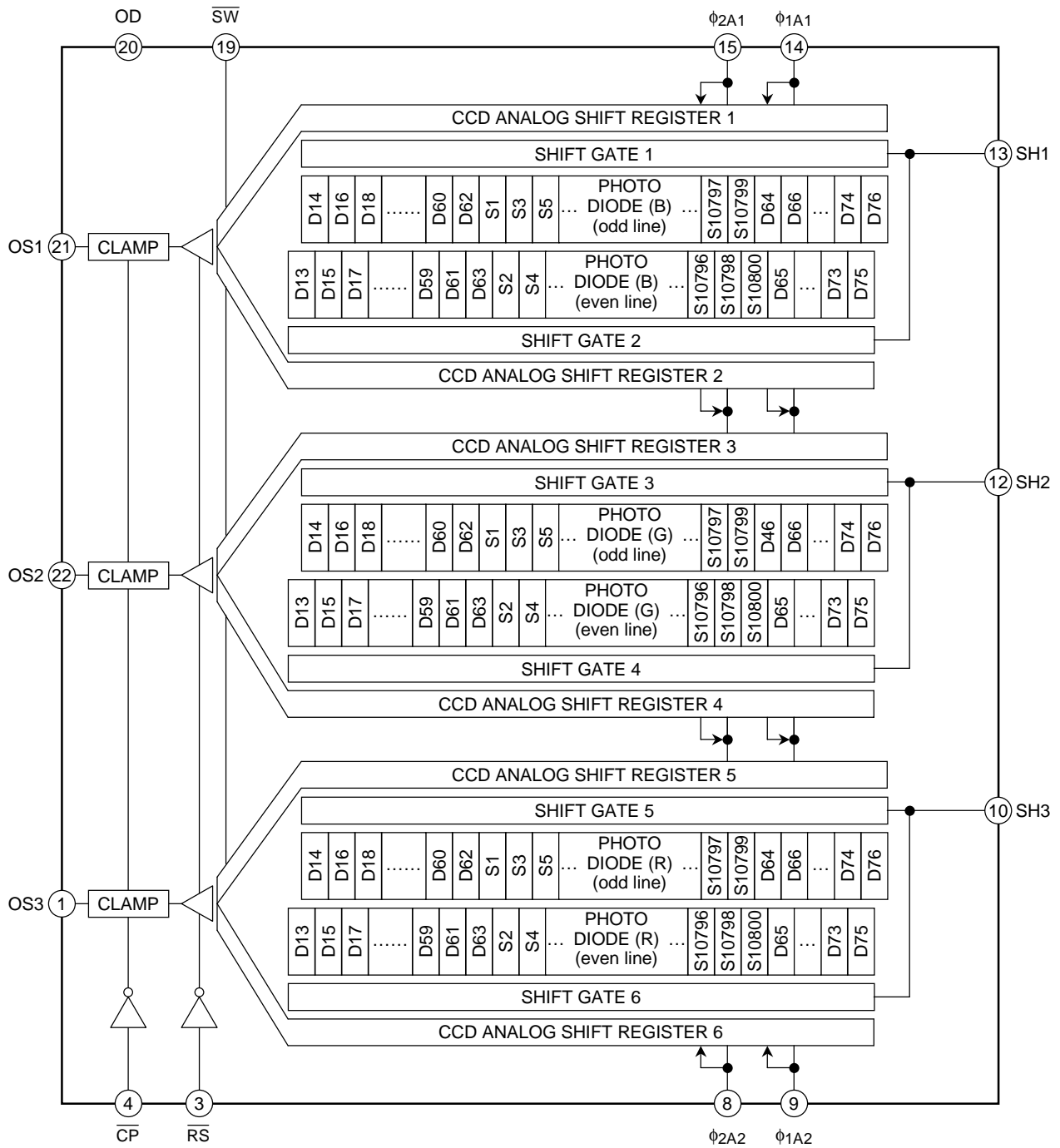


Weight: 1.6g (typ.)

Pin Connections (top view)



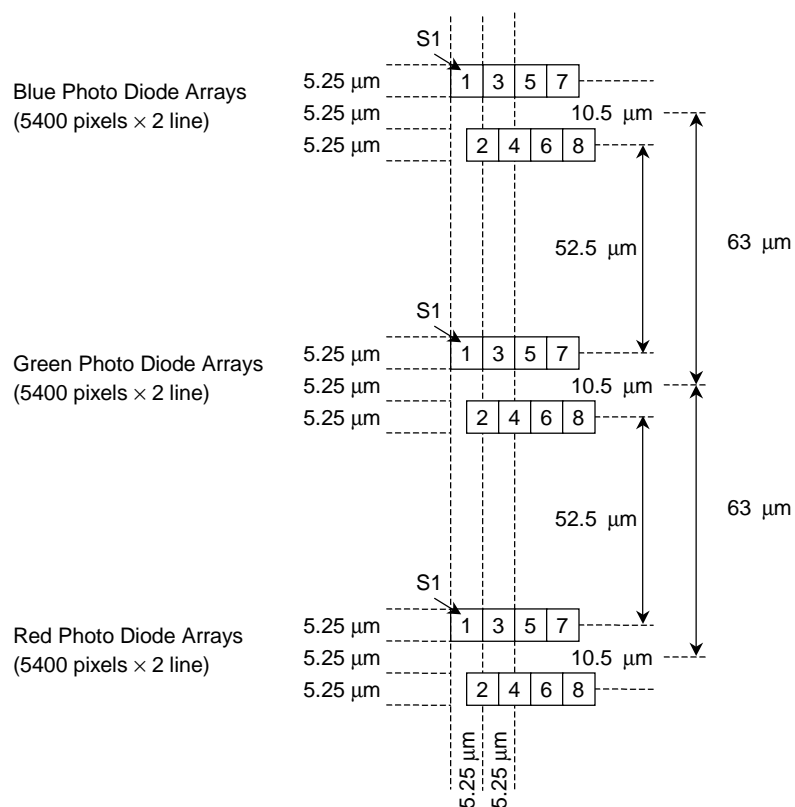
Block Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS3	Signal Output 3 (red)	12	SH2	Shift Gate 2
2	SS	Ground	13	SH1	Shift Gate 1
3	\overline{RS}	Reset Gate	14	$\phi 1A1$	Clock 1 (phase 1)
4	\overline{CP}	Clamp Gate	15	$\phi 2A1$	Clock 1 (phase 2)
5	NC	Non Connection	16	NC	Non Connection
6	NC	Non Connection	17	NC	Non Connection
7	NC	Non Connection	18	NC	Non Connection
8	$\phi 2A2$	Clock 2 (phase 2)	19	\overline{SW}	Switch Gate
9	$\phi 1A2$	Clock 2 (phase 1)	20	OD	Power
10	SH3	Shift Gate 3	21	OS1	Signal Output 1 (blue)
11	SS	Ground	22	OS2	Signal Output 2 (green)

Arrangement of The 1st Effective Pixel (S1)



Optical/Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{OD} = 12\text{ V}$, $V_{SW} = 5\text{ V}$, $V_\phi = V_{SH} = V_{RS} = V_{CP} = 5\text{ V}$ (pulse), $f_\phi = 1\text{ MHz}$, $f_{RS} = 2\text{ MHz}$, $t_{INT} = 11\text{ ms}$, light source = a light source + CM500S filter ($t = 1\text{ mm}$), load resistance = $100\text{ k}\Omega$)

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	3.2	4.7	6.2	V/lx·s	(Note2)
	Green	R (G)	4.4	6.4	8.4		
	Blue	R (B)	2.5	3.7	4.9		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note3)
		PRNU (3)	—	3	12	mV	(Note4)
Register imbalance		RI	—	1	—	%	(Note5)
Saturation output voltage		V_{SAT}	2.8	3.5	—	V	(Note6)
Saturation exposure		SE	0.33	0.54	—	lx·s	(Note7)
Dark signal voltage		V_{DRK}	—	0.5	2.0	mV	(Note8)
Dark signal non uniformity		DSNU	—	2.0	7.0	mV	(Note8)
DC power dissipation		PD	—	360	650	mW	
Total transfer efficiency		TTE	92	98	—	%	
Output impedance		Z_O	-	0.3	1.0	k Ω	
DC output voltage		V_{OS}	5.0	6.0	7.0	V	(Note9)
Reset noise		V_{RSN}	—	0.3	—	V	(Note9)
Random noise		$N_{D\sigma}$	—	0.9	—	mV	(Note10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta \bar{X}}{\bar{X}} \times 100 (\%)$$

Where \bar{X} is average of total signal output and $\Delta \bar{X}$ is the maximum deviation from \bar{X} . The amount of incident light is shown below.

Red = 1/2 • SE

Green = 1/2 • SE

Blue = 1/4 • SE

Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured at 5% of SE (typ.)

Note 5: Register imbalance is defined as follows.

$$\text{RI} = \frac{\sum_{n=1}^{10799} |x_n - \bar{x}|}{10799 \cdot \bar{x}} * 100 (\%)$$

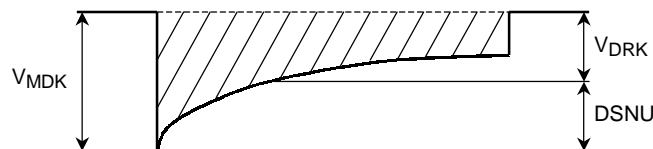
Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.

Note 7: Definition of SE

$$\text{SE} = \frac{V_{\text{SAT}}}{R_G} (\text{lx} \cdot \text{s})$$

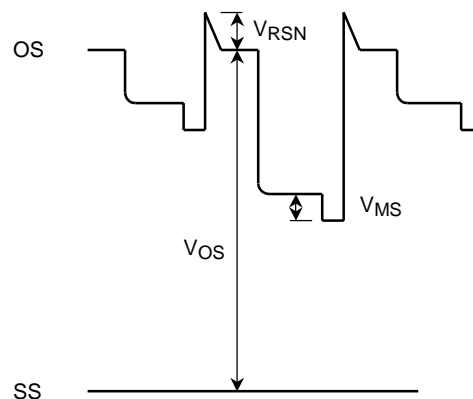
Note 8: V_{DRK} is defined as average dark signal voltage of all effective pixels.

DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.

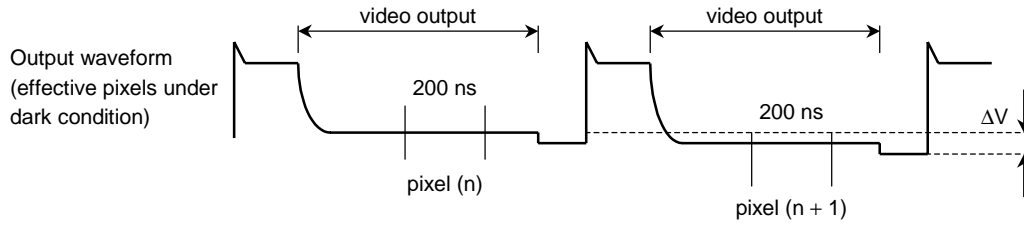


Note 9: DC signal output voltage is defined as follows.

Reset Noise Voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



- (1) Two adjacent pixels (pixel n and n + 1) after reference level clamp in one reading are fixed as measurement points.
- (2) Each of the output level at video output periods averaged over 200 ns period to get V (n) and V (n + 1).
- (3) V (n + 1) is subtracted from V (n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$
- (4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (\Delta V_i - \overline{\Delta V})^2}$$

- (5) Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
- (6) 10 sigma values are averaged.

$$\bar{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- (7) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$N_{D\sigma} = \frac{1}{\sqrt{2}} \bar{\sigma}$$

Operating Condition

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" Level	$V_{\phi A}$	4.5	5.0	5.5	V
	"L" Level		0	0	0.3	
Shift pulse voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V
	"L" Level		0	0	0.5	
Reset pulse voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V
	"L" Level		0	0	0.5	
Clamp pulse voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V
	"L" Level		0	0	0.5	
Switch pulse voltage	"H" Level	$V_{\overline{SW}}$	4.5	5.0	5.5	V
	"L" Level		0	0	0.5	
Power supply voltage		V_{OD}	11.4	12.0	12.6	V

Clock Characteristics (Ta = 25°C)

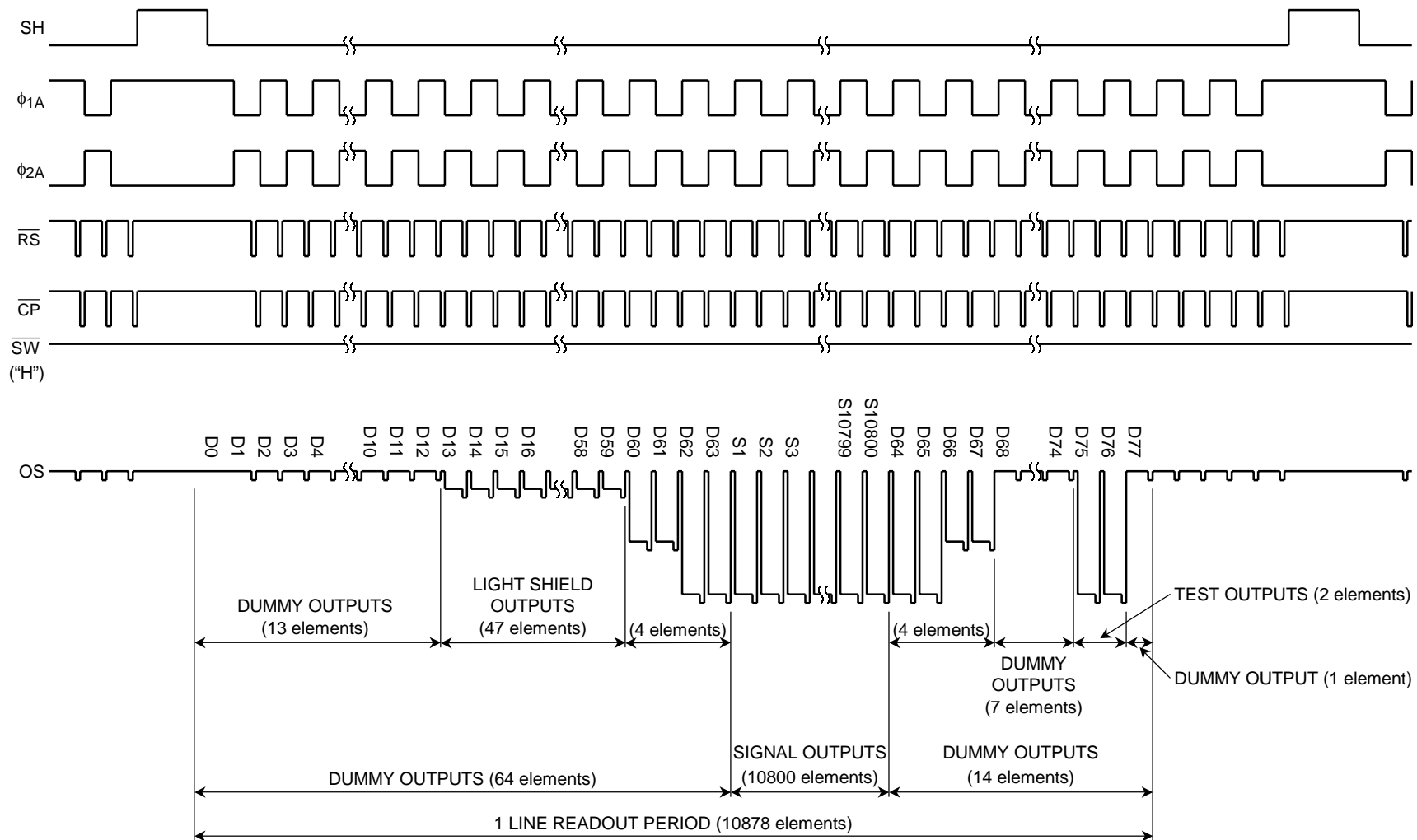
Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse frequency		$f_{\phi A}$	0.15	1.0	8.0	MHz
Reset pulse frequency		$f_{\overline{RS}}$	0.3	2.0	10.0	MHz
Clamp pulse frequency		$f_{\overline{CP}}$	0.3	2.0	10.0	MHz
Clock capacitance (Note 11)		$C_{\phi A}$	—	400	—	pF
Shift gate capacitance		C_{SH}	—	50	—	pF
Reset gate capacitance		$C_{\overline{RS}}$	—	10	—	pF
Clamp gate capacitance		$C_{\overline{CP}}$	—	10	—	pF
Switch gate capacitance		$C_{\overline{SW}}$	—	10	—	pF

Note 11: $V_{OD} = 12\text{ V}$

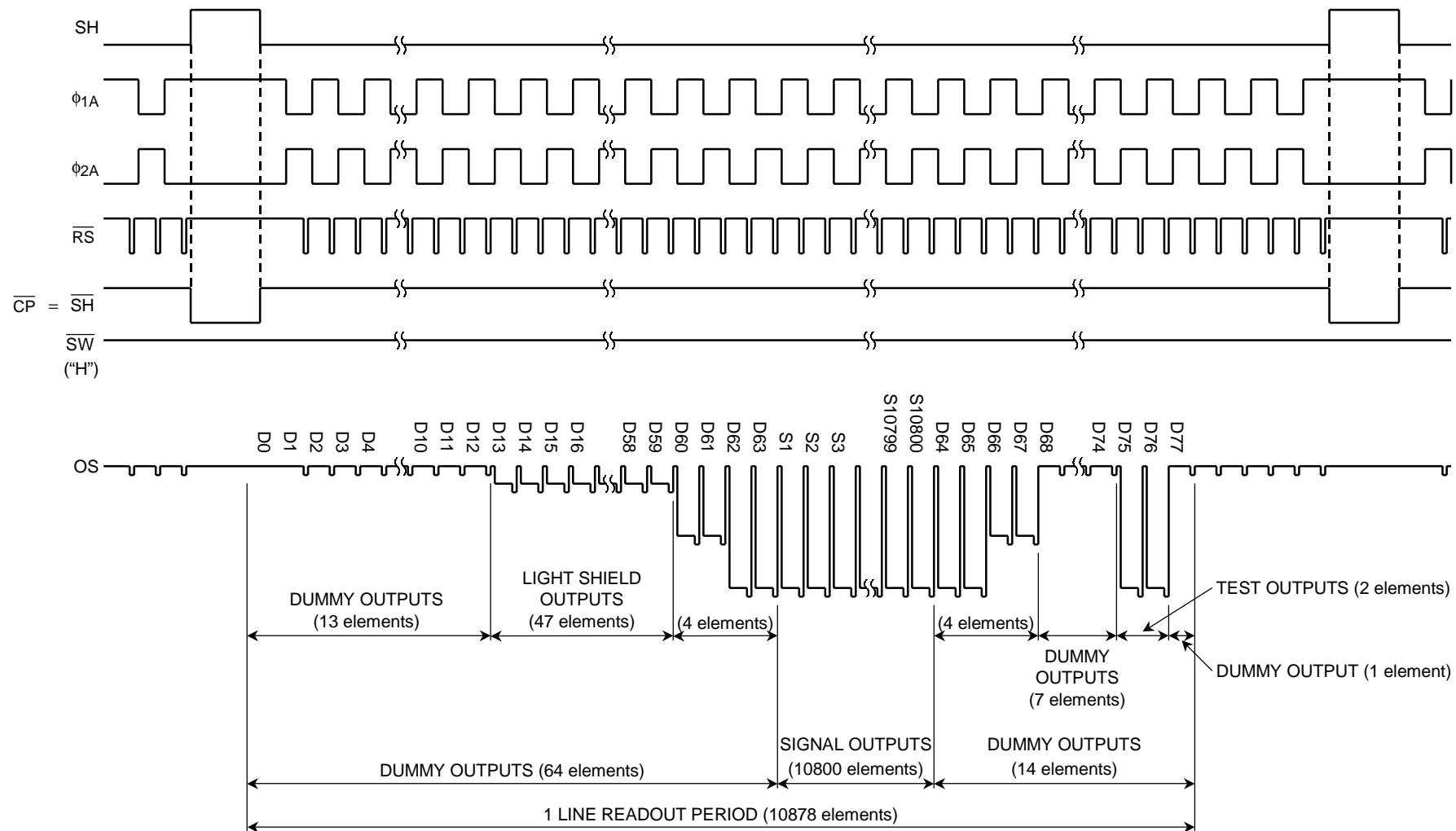
Clocking Mode

Mode		\overline{SW}	SH	$\phi 1A, \phi 2A$	\overline{RS}	\overline{CP}
Bit Clamp	1200DPI(Color)	"H"	Pulse	Pulse	Pulse	Pulse
	600DPI(Color)	"L"	Pulse	Pulse	Pulse	Pulse
Line Clamp	1200DPI(Color)	"H"	Pulse	Pulse	Pulse	\overline{SH} or "H"
	600DPI(Color)	"L"	Pulse	Pulse	Pulse	\overline{SH} or "H"

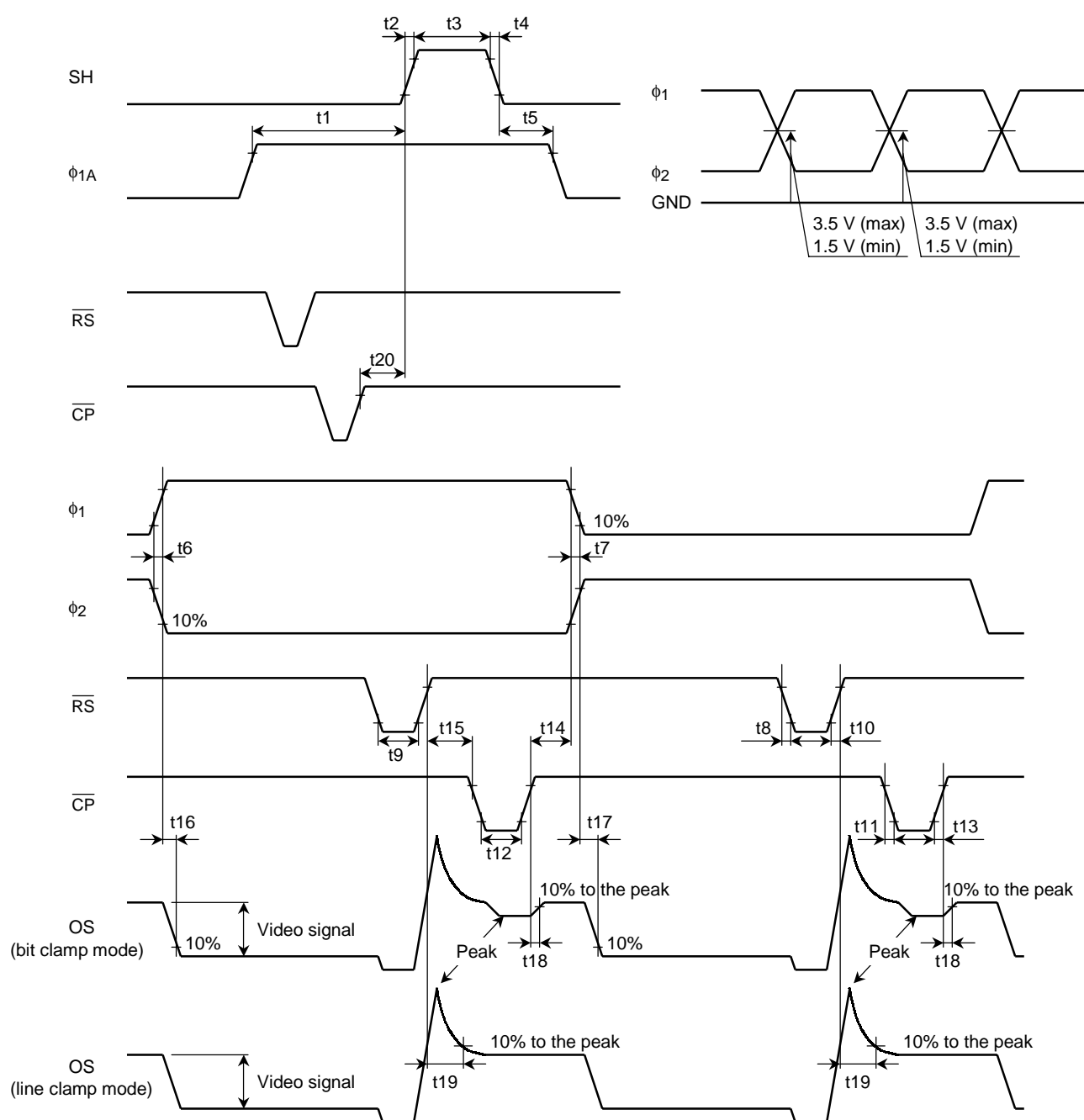
Timing Chart (bit clamp mode)



Timing Chart (line clamp mode)



Timing Requirements

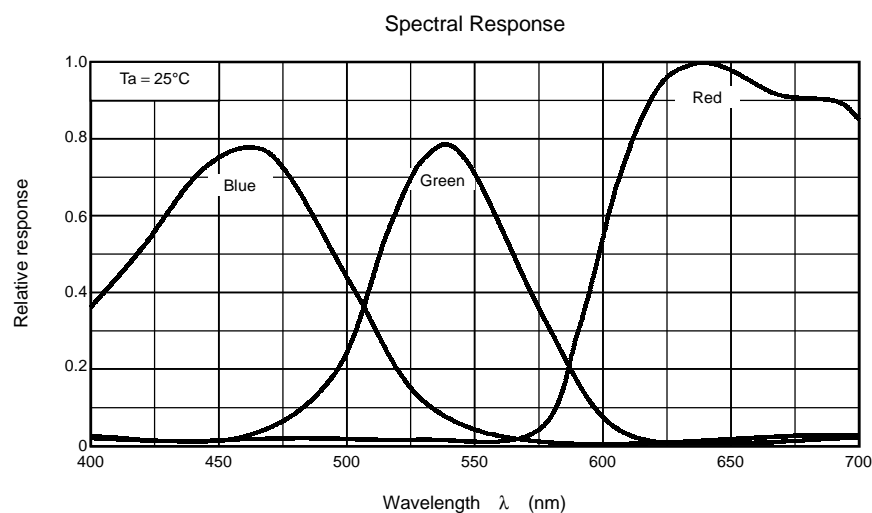


Characteristics	Symbol	Min	Typ. (Note 12)	Max	Unit
Pulse timing of SH and ϕ_1	t1	110	1000	—	ns
	t5	800	1000	—	
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	3000	5000	—	ns
ϕ_1 , ϕ_2 pulse rise time, fall time	t6, t7	0	50	—	ns
\overline{RS} pulse rise time, fall time	t8, t10	0	20	—	ns
\overline{RS} pulse width	t9	15	100	—	ns
\overline{CP} pulse rise time, fall time	t11, t13	0	20	—	ns
\overline{CP} pulse width	t12	25	100	—	ns
Pulse timing of ϕ_{1A} , ϕ_{2A} and \overline{CP}	t14	10	40	—	ns
Pulse timing of \overline{RS} and \overline{CP}	t15	0	100	—	ns
Video data delay time (Note 13)	t16, t17	—	20	—	ns
Reference level settle time	t18	—	20	—	ns
	t19	—	35	—	ns
Pulse timing of SH and \overline{CP}	t20	0	500	—	ns

Note 12: Typ. is the case of $f\phi = 1.0$ MHz.

Note 13: Load resistance is 100 k Ω .

Typical Spectral Response



The diagram illustrates a 12-bit digital-to-analog converter (DAC) circuit. The central component is a TCD2905CF shift register, which is a 12-bit serial-in/parallel-out (SIPO) shift register. It has 22 pins: 12 data pins (1-12), 4 control pins (13-16), and 6 status pins (17-22). The pins are labeled as follows: 1 (OS3), 2 (SS), 3 (RS), 4 (CP), 5 (NC), 6 (NC), 7 (NC), 8 (φ2A2), 9 (φ1A2), 10 (SH3), 11 (SS), 12 (SH2), 13 (SH1), 14 (φ1A1), 15 (φ2A1), 16 (NC), 17 (NC), 18 (NC), 19 (SW), 20 (OD), 21 (OS1), 22 (OS2).

The circuit is powered by a +12 V supply and a +5 V supply. The +12 V supply is connected to the OS1, OS2, and OS3 pins of the TCD2905CF. The +5 V supply is connected to the φ1A1, φ1A2, φ2A1, and φ2A2 pins of the TCD2905CF. The +5 V supply is also connected to the SW, SH1, SH2, SH3, CP, and RS pins of the TCD2905CF. The +5 V supply is also connected to the φ1A1, φ1A2, φ2A1, and φ2A2 pins of IC1 and IC2.

The TCD2905CF is connected to two 4-bit DACs, IC1 and IC2. IC1 is a 4-bit DAC with 4 pins: φ1A1, φ1A2, φ2A1, and φ2A2. IC2 is a 4-bit DAC with 4 pins: SW, SH1, SH2, and SH3. The outputs of IC1 and IC2 are connected to the φ1A1, φ1A2, φ2A1, and φ2A2 pins of the TCD2905CF. The outputs of IC1 and IC2 are also connected to the φ1A1, φ1A2, φ2A1, and φ2A2 pins of the TCD2905CF.

The circuit includes several resistors (R1, R2) and transistors (TR1, TR2, TR3) for signal conditioning and level shifting. The output of the DAC is a 12-bit digital signal, which is converted to an analog signal by the DACs. The output of the DAC is a 12-bit digital signal, which is converted to an analog signal by the DACs.

IC1, 2: TC74HC04AP
TR1, 2, 3: 2SC1815-Y
R1: 150 Ω
R2: 1500 Ω

Caution**1. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. **Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.**
- b. **Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.**
- c. **Ground the tools such as soldering iron, radio cutting pliers or pincer.**
It is not necessarily required to execute all precaution items for static electricity.
It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

3. Moisture-proof Packing

CCD surface mount products may have a haze on the inside of glass when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. However, since a haze will disappear if time passes even if a haze happens on the inside of glass, there is no problem in quality. If you are worrisome such a haze, please observe the following precautions:

- a. **This moisture barrier bag may be stored unopened 12 months at or below 30°C/90% RH.**
- b. **After opening this moisture proof bag, the packages should be assembled within 5 days in an environment less than 30°C/60% RH.**
- c. **If upon opening, the moisture indicator card shows humidity above 30% or the expiration date has passed, they may still be used with the addition of a bake of 3 hours at 125°C.**
After baking the packages, it should be assembled with 5 days in an environment less than 30°C/60% RH.
- d. **Expiration date; 12 months from sealing date, which is imprinted near the heat-seal.**

4. Ultrasonic Cleaning

Ultrasonic cleaning should not be used with such hermetically-sealed ceramic package as CCD because the bonding wires can become disconnected due to resonance during the cleaning process.

5. Mounting

In the case of solder mounting, the devices should be mounted with the window glass protective tape in order to avoid dust or dirt included in reflow machine.

6. Soldering Temperature Profile for Pb free

Good temperature profile for each soldering method is as follows. In addition, in case of the repair work accompanied by IC removal, since the degree of parallel may be spoiled with the left solder, please do not carry out and in case of the repair work not accompanied by IC removal, carry out with a soldering iron or , in reflow, carry out at once.

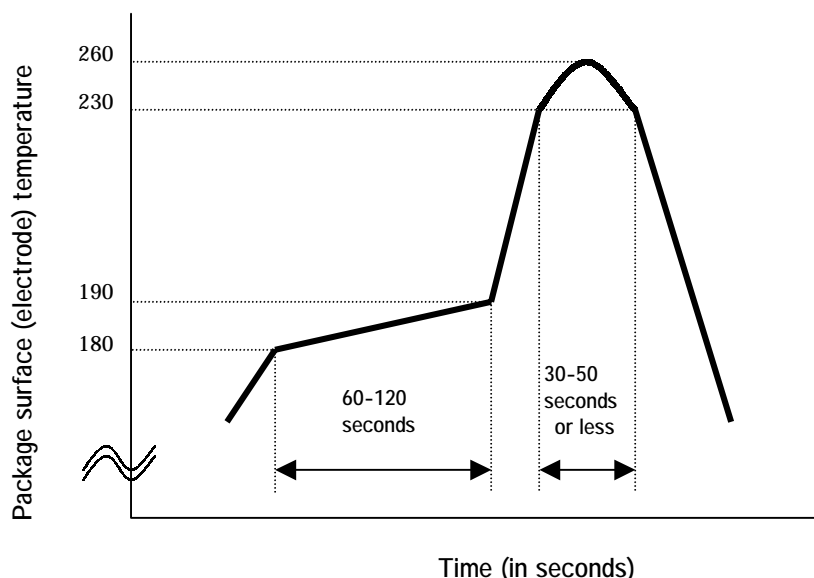
1. Using a soldering iron

Complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

2. Using long infrared rays reflow/hot air reflow

Complete the infrared ray reflow process within between 30 seconds and 50 seconds at a package surface (electrode) temperature of between 230°C and 260°C.

Refer to the following Figure for an example of a good temperature profile for long infrared rays or hot air reflow.



3. Window Glass Protective Tape

Although there is discoloration of the window glass protective tape by solder mounting, there is no problem in quality.

After solder mounting, if the window glass protective tape is removed, adhesives will remain in the glass surface. Since these adhesives appear as black flaws on the image, please wipe off it by a swab or cloth soaked in small amount of organic solution, such as alcohol (ethanol etc.), before including in a product.

4. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

Application Note

The TCD2905CF can be operated in two modes: Normal Readout Mode and Even Line Readout Mode. Each mode is selected by \overline{SW} terminal.

\overline{SW}	Mode	Application Example
H	Normal Readout Mode	1200 DPI/A4 Reading
L	Even Line Readout Mode	600 DPI/A4 Reading

Normal Readout Mode

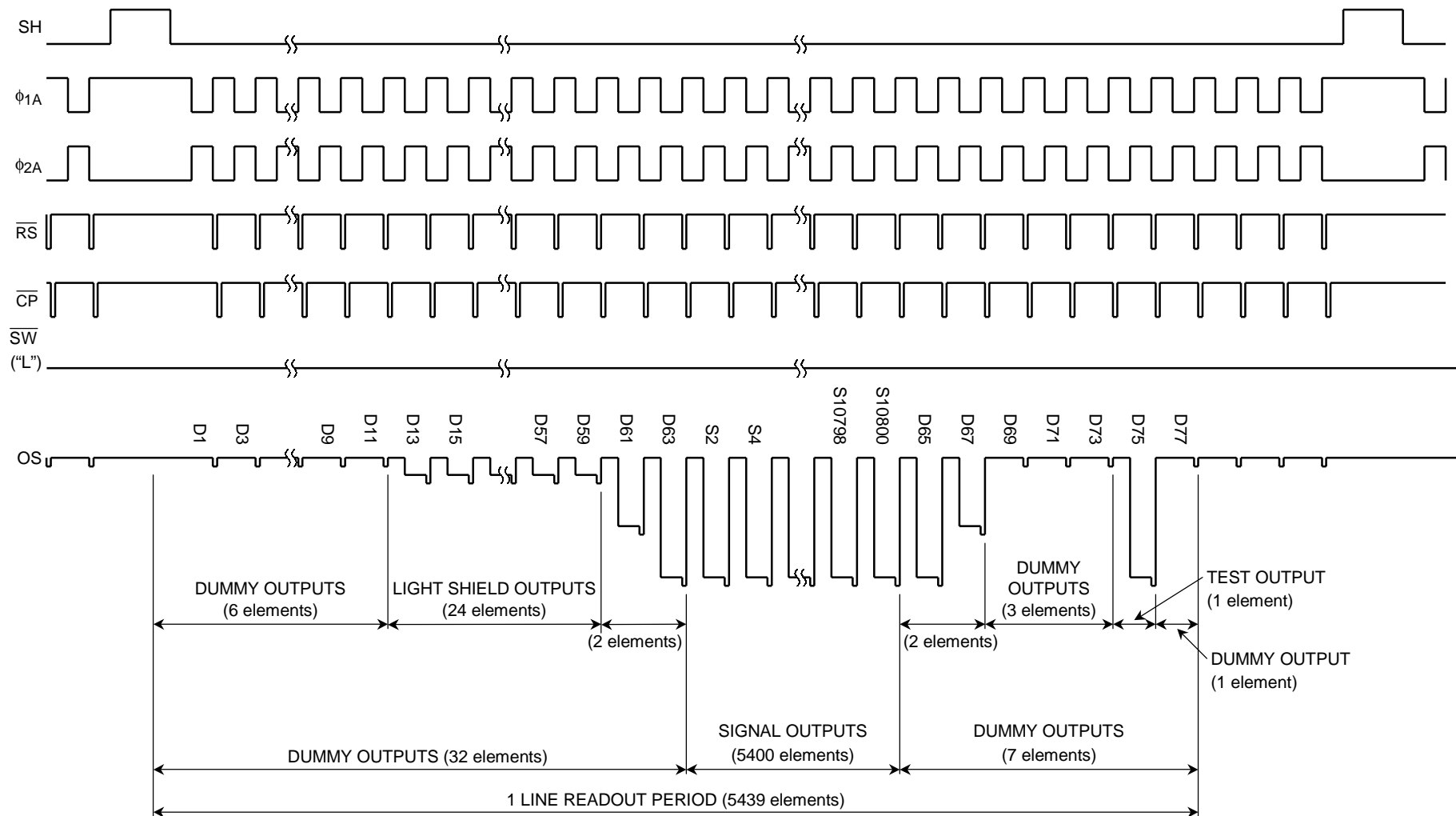
In Normal Readout Mode, the dummy and signal outputs in odd and even lines are read out. This mode provides 1200 DPI/A4 resolution. The timing for this mode is shown in page 7/21, 8/21 and 9/21.

Even Line Readout Mode

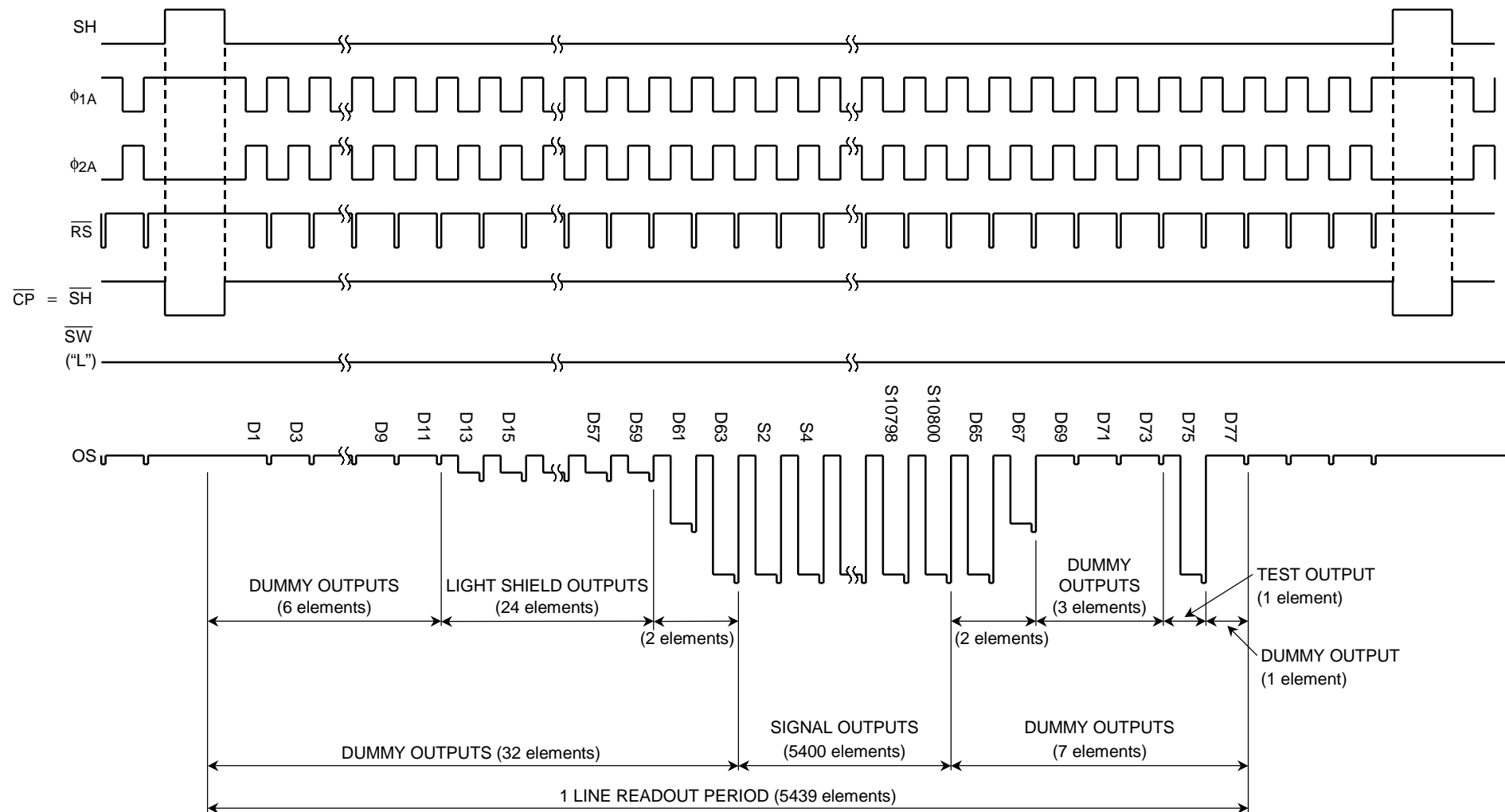
In Even Line Readout Mode, the dummy and signal outputs in even lines are read out. The dummy and signal outputs in odd lines cannot be read out in this mode. This mode provides 600 DPI/A4 resolution. Timing examples for 600 DPI/A4 reading using this mode are shown in page 15/21, 16/21 and 19/21 for reference.

In this mode, signal charges of adjacent pixels in even line can be merged at an output stage capacitor using intermittent reset drive. Timing examples for 300 DPI/A4 reading using this mode are shown in page 17/21, 18/21 and 20/21 for reference.

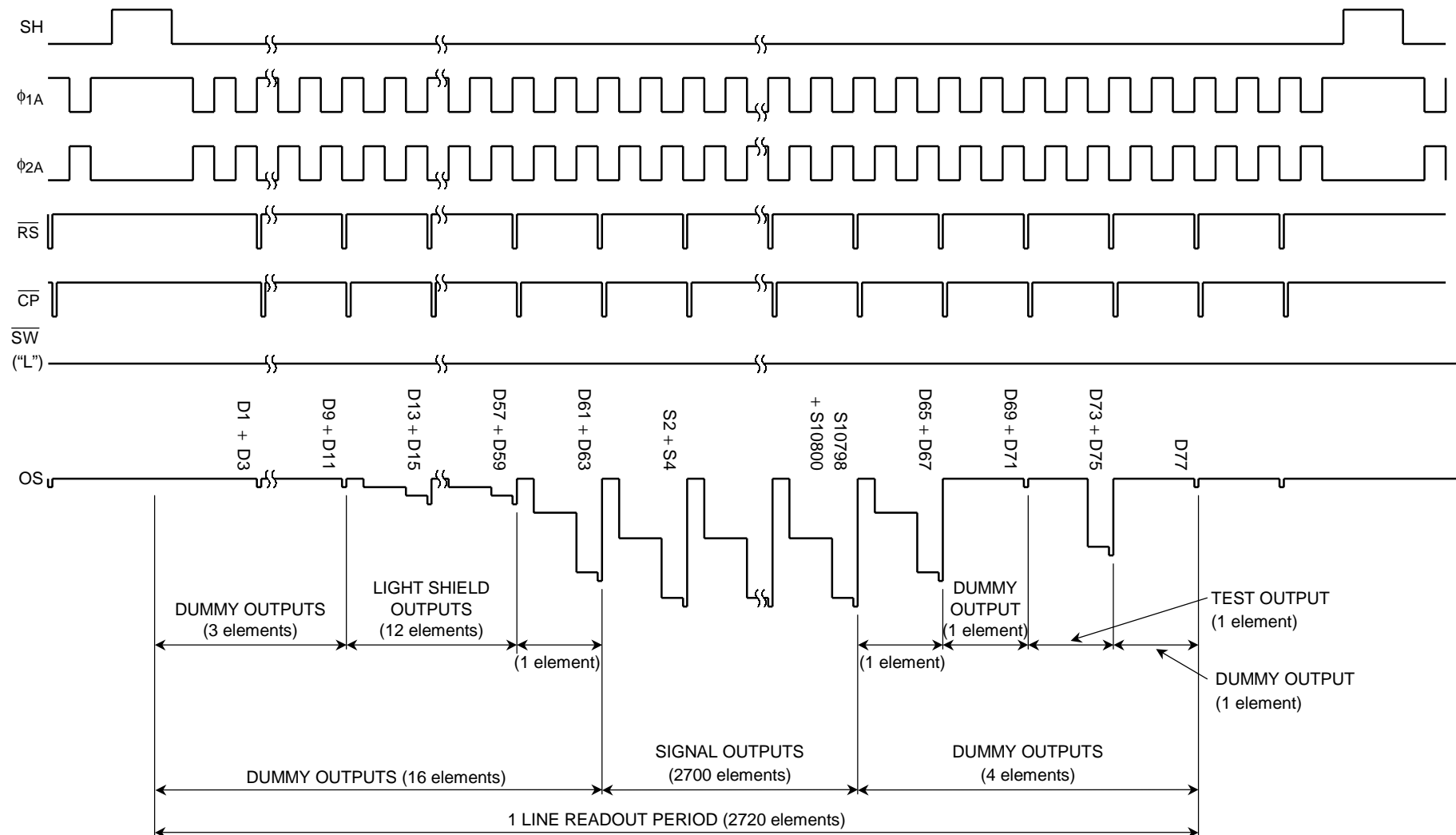
Timing Chart (600 dpi mode)



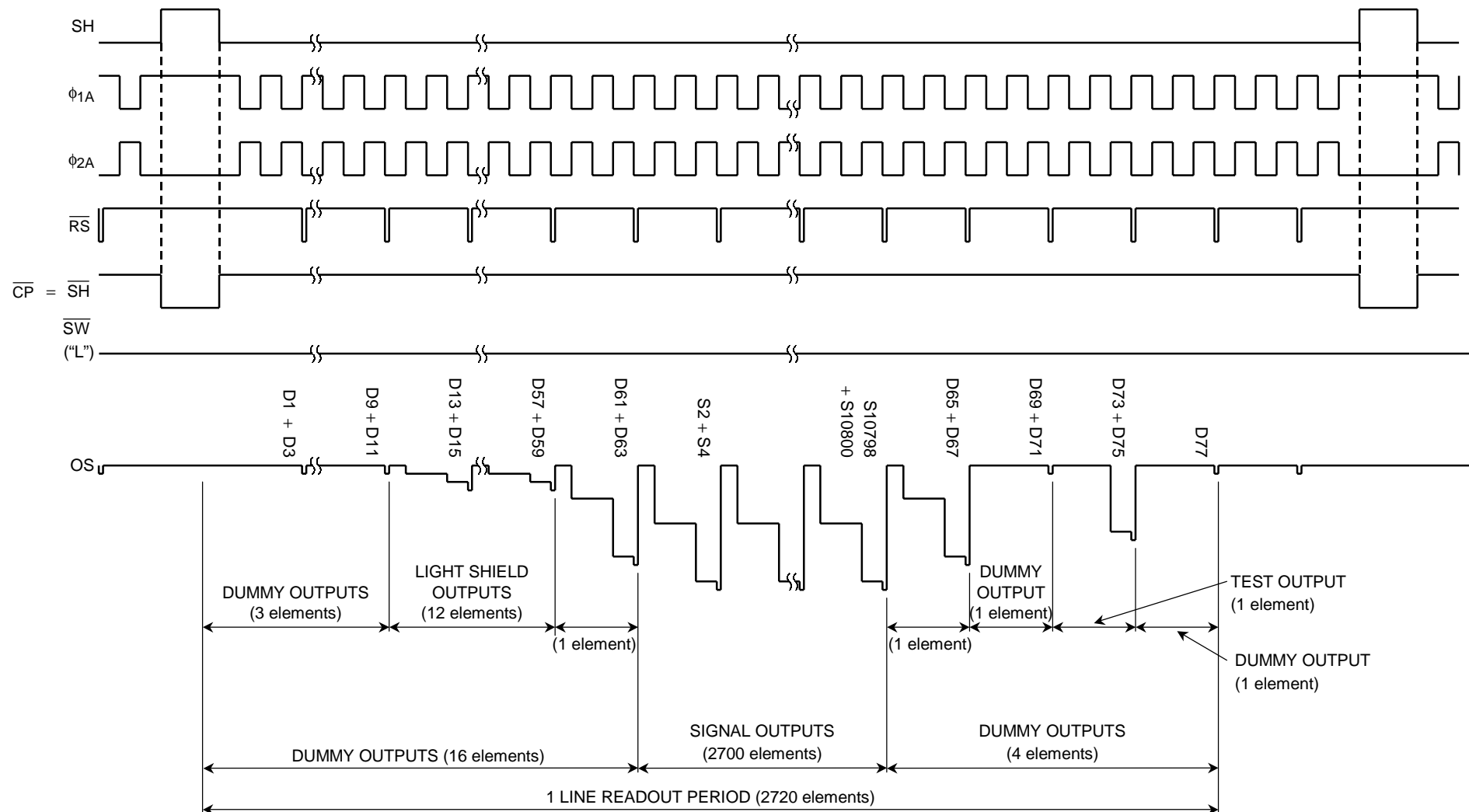
Timing Chart (600 dpi/line clamp mode)



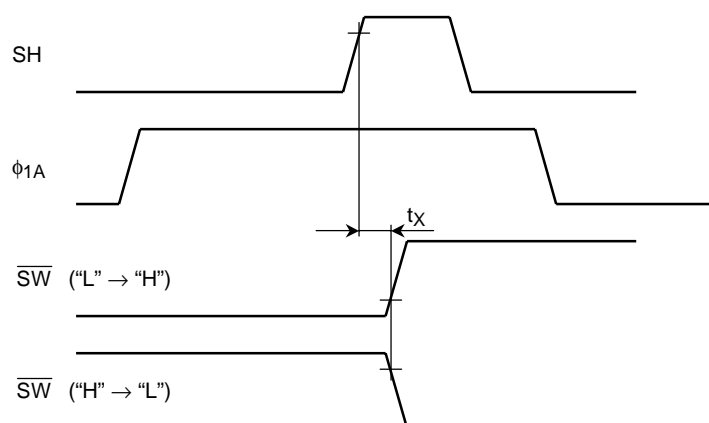
Timing Chart (300 dpi mode)



Timing Chart (300 dpi/line clamp mode)

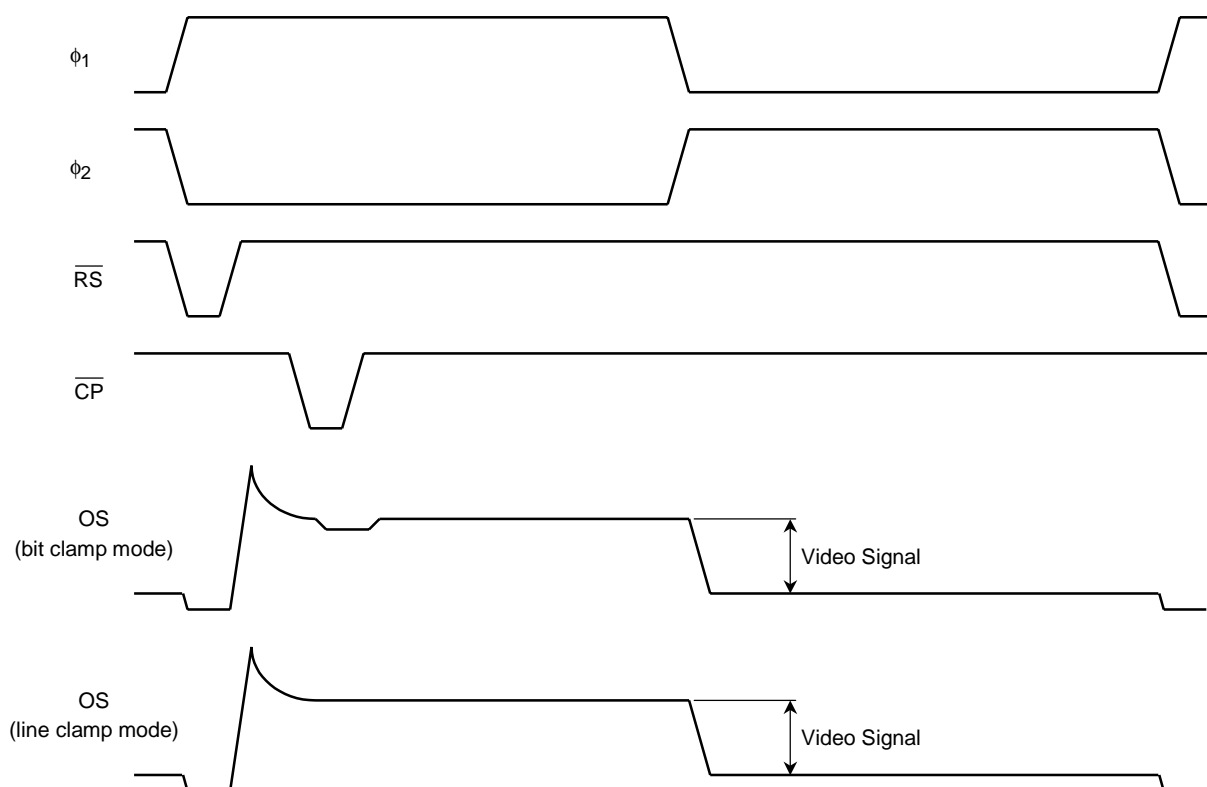


Timing Example

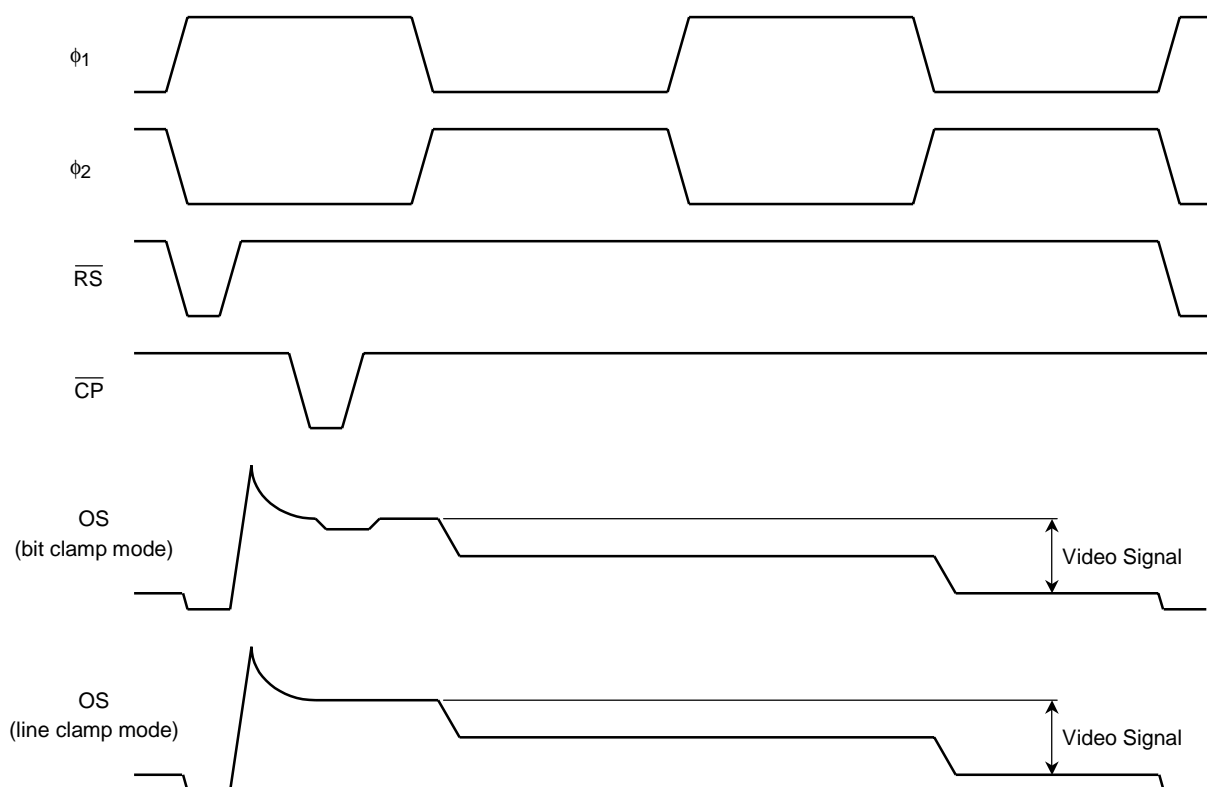


Characteristic	Symbol	Min	Typ.	Max	Unit
Pulse timing of SH and \overline{SW}	t_x	0	0	—	ns

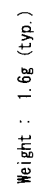
Timing Example (600 dpi mode: \overline{SW} = "L")



Timing Example (300 dpi mode: $\overline{SW} = "L"$)



Unit : mm



RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.