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## The Dark Side of Flyback Converters

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## Course Agenda

$\square$ The Flyback Converter
$\square$ The Parasitic Elements
$\square$ How These Parasitics Affect your Design?
$\square$ Current-Mode is the Most Popular Scheme
$\square$ Fixed or Variable Frequency?
$\square$ More Power than Needed
$\square$ The Frequency Response
$\square$ Compensating With the TL431

## What is the Subject?

$\square$ There has been numerous seminars on Flyback converters
Seminars are usually highly theoretical - link to the market?
Industrial requirements usually not covered: standby, over power...
This 3-hour seminar will shed lights on less covered topics:

* Why the converter delivers more power than expected? Solutions?
* Books talk about compensation with op amps, I have a TL431!
* The origin of the Right-Half Plane Zero, how do I deal with it?
* Quasi-resonant converters presence increases, how do they work?
> In a 3-hour course, we are just scratching the surface...!


## The Flyback, a Popular Structure

- The flyback converter is widely used in consumer products
$\checkmark$ Ease of design, low-cost, well-known structure
- Poor EMI signature, bulky transformer, practical up to 150 W

$\xrightarrow{\text { Charger }}$ flyback $\approx 3-5 \mathrm{~W}$

$$
\xrightarrow[\text { Netbook }]{\text { Notebok }} \text { flyback } \approx 40-180 \mathrm{~W}
$$

## An Isolated Buck-Boost

- The flyback converter is derived from the buck-boost cell

flyback
isolated ground referenced
- The addition of a transformer brings:

$+$

- Up or down scale $V_{i n}$
- Isolation
- Polarity change
- More than 1 output


## The Turn-on Event

The power switch turns on: current ramps up in $L_{p}, D$ is blocked


The current increases in the inductor in relationship to $V_{i n}$ and $L_{p}$
$\square$ The output capacitor supplies the load on its own

## Applying Volt-Second Balance, CCM

The power switch turns off: $D$ conducts, $V_{\text {out }}$ "flies" back

$$
\frac{V_{o u t}}{V_{\text {in }}}=\frac{N t_{\text {on }}}{t_{\text {off }}}=\frac{N D T_{s w}}{(1-D) T_{s w}}=\frac{N D}{1-D} \quad \text { dc transfer function in CCM }
$$

## Applying Volt-Second Balance, DCM

In DCM, when $L_{p}$ is fully depleted $D$ opens: $V_{\text {out }}$ reflection is lost

dc transfer function in DCM


From the buck-boost:
$\frac{V_{\text {out }}}{N V_{\text {in }}}=D \sqrt{\frac{R_{\text {load }}}{2 L_{p} N^{2} F_{s w}}}$

## Flyback, Typical Waveforms

Below is a simple flyback converter, without parasitics

$\square \mathrm{It}$ will run open loop for simplicity, $V_{\text {out }} \approx 8 \mathrm{~V}$

## Flyback, Typical Waveforms, CCM



## Flyback, Typical Waveforms, DCM



DCM flyback - no parasitics

## Energy Transfer in CCM and DCM

The primary inductance, $L_{p}$, stores and releases energy

$$
\begin{array}{ll}
E_{L_{p}, \text { valley }}=\frac{1}{2} L_{p} I_{\text {valley }}{ }^{2} & \text { Initially stored energy } \\
E_{L_{p}, \text { peak }}=\frac{1}{2} L_{p} I_{\text {peak }}{ }^{2} & \text { Stored energy at } t_{o n} \\
E_{L_{p}, \text { accu }}=\frac{1}{2} L_{p} I_{\text {peak }}{ }^{2}-\frac{1}{2} L_{p} I_{\text {valley }}{ }^{2}=\frac{1}{2} L_{p}\left(I_{p e a k}^{2}-I_{\text {valley }}{ }^{2}\right) \quad \text { Accumulated energy at } T_{s w}
\end{array}
$$

- Power (W) is energy (J) averaged over time (s):

$$
\begin{aligned}
& P_{\text {out }}=\frac{1}{2}\left(I_{\text {peak }}^{2}-I_{\text {valley }}{ }^{2}\right) L_{p} F_{s t} \eta^{\text {Cta, the efficiency }} \\
& P_{\text {out }}=\frac{1}{2} I_{\text {peak }}{ }^{2} L_{p} F_{\text {sw }} \eta
\end{aligned} \text { DCM, } I_{\text {valley }}=0
$$

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## Considering Parasitic Elements

The transformer and the MOSFET include parasitics


## Considering Parasitic Elements, CCM



## Considering Parasitic Elements, DCM



DCM mode - with parasitics

## Who Are the Stray Elements?

The study of the drain node reveals a $L C$ network


## The MOSFET C ${ }_{\text {oss }}$ is a Non-Linear Device

The capacitor value changes with its bias voltage


$$
\llbracket \square C_{O S S}\left(V_{D S}\right)=\frac{C_{D 0}}{\sqrt{\left(1+\frac{V_{D S}}{V_{0}}\right)}}
$$

$C_{D 0}$ is the cap. for $V_{D S}=V_{0}$


## As the Voltage Decreases, Coss Value Changes

- The brutal discharge generates switching losses


The energy lost is smaller with the non-linear variation!

## Using the Raw $\mathrm{C}_{\text {oss }}$ is an ... Overkill

Re-compute the capacitor from the MOSFET data-sheet

| Input Capacitance | $\mathrm{C}_{\text {iss }}$ | $\frac{\mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V},}{V_{D 0}}, \mathrm{v}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ | - | 1300 | - | pF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Reverse Transfer Capacitance | $\mathrm{Crss}^{\text {r }}$ |  | - | 130 | - |  |
| Output Capacitance | $\mathrm{C}_{\text {oss }}$ |  | - | 400 | - |  |

The classical equation gives:

$$
W=\frac{1}{2} C_{O S S} V_{D S}^{2}=0.5 \times 400 p \times 100^{2}=2 \mu \mathrm{~J} \text { or } 200 \mathrm{~mW} @ 100 \mathrm{kHz}
$$

The updated equation gives:


## The Leakage Inductance

The coupling in a transformer is not perfect

$\square$ Some induction lines couple in the air: leakage flux

## An Equivalent Transformer Model

- For a two-winding transformer, the model is simple:
$\checkmark$ Two leakage inductors
$\checkmark$ One magnetizing inductor


This is commonly known as the "Pl" model

## The Transformer Scales the Primary Current

In a perfect transformer, we have:


The turns ratio is usually normalized to the primary

$$
\left.\left.\begin{array}{l}
N_{p}: N_{s} \xrightarrow{\text { Divide by } N_{p}} \frac{N_{p}}{N_{p}}: \frac{N_{s}}{N_{p}} \xrightarrow{\longrightarrow} 1: N \\
N_{p}=100 \\
N_{s}=25
\end{array}\right\} 1: 0.25 \quad 1\right\} 250 \mathrm{~m}
$$

## The Leakage Term also Stores Energy

At turn-on, the primary current flows in both $l_{\text {leak }}$ and $L_{p}$

$\square$ During the on-time, both $L_{p}$ and $l_{\text {leak }}$ store energy

## Where does the Current Flow?

At turn-off, the energy stored in $L_{p}$ is dumped in the output cap.


The leakage inductor current fills up the drain lump capacitor

## Watch out for the Maximum Excursion!

$\square$ As the diode conducts, $V_{\text {out }}$ reflects over $L_{p}$


The voltage on the drain increases dangerously!

## We Need to Clamp that Voltage

$\square$ MOSFETs have a voltage limit they can fly up to: $B V_{D S S}$
$\square$ A clamping circuit has been installed to respect a margin


## Resetting the Leakage Inductance

$\square$ Because of the clamp action, a voltage appears across $l_{\text {leak }}$

$$
V_{l_{\text {leak }}}=V_{\text {clamp }}-\left(V_{\text {out }}+V_{f}\right)
$$



This voltage forces a reset of the leakage inductance

## Do we Need a Quick Reset?

When current flows in $l_{\text {leak }}$, it is diverted from the secondary


The leakage current delays the occurrence of the sec. current

## $l_{\text {leak }}$ Delays the Secondary Current

The leakage inductor reduces the peak secondary current


The "stolen" energy is dissipated as heat in the clamping network
$\square$ Less energy is transmitted to the secondary side

## A Reduced Secondary-Side Current

$\square$ We can calculate the leakage inductor reset time $\Delta t$


$$
\begin{gathered}
S_{l_{\text {leak }}}=\frac{V_{\text {clamp }}-\left(V_{\text {out }}+V_{f}\right)}{l_{\text {leak }}} \\
\Delta t=\frac{I_{\text {peak }}}{S_{\text {leak }}}=\frac{l_{\text {leak }} I_{\text {peak }}}{V_{\text {clamp }}-\left(V_{\text {out }}+V_{f}\right)} \\
\xrightarrow{N \neq 1} \Delta t=\frac{I_{\text {peak }}}{S_{\text {leak }}}=\frac{N l_{\text {leak }} I_{\text {peak }}}{N V_{\text {clamp }}-\left(V_{\text {out }}+V_{f}\right)} \\
I_{\text {sea }}=\frac{I_{\text {peak }}}{N}-S_{\text {seac }} \Delta t=\frac{I_{\text {peak }}}{N}\left(1-\frac{l_{\text {leak }}}{L_{p}} \frac{1}{V_{\text {out }}+V_{f}}\right)
\end{gathered}
$$

$$
\frac{l_{\text {leak }}}{L_{p}}=1.8 \%, \frac{N V_{\text {clamp }}}{V_{\text {out }}+V_{f}}=1.5 \quad \text { IT } \quad I_{\text {sec }}=\frac{I_{\text {peak }}}{N}-3.6 \%
$$

## Typical Example Simulation Results



## A Ringing Appears as the Diode Blocks

$\square$ As the clamp diode blocks, the drain returns to $V_{\text {in }}+\frac{V_{\text {out }}+V_{f}}{N}$


## The Primary Inductor also Rings in DCM

$\square$ When $L_{p}$ is reset, the capacitor voltage returns to $V_{\text {in }}$


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## How these Parasitics Affect your Design?

The leakage inductor induces a large spike at turn-off
$\square$ This voltage excursion must be kept under control

$\square$ The lump capacitor on the drain brings switching losses
$\square$ Is there a way to switch on again when discharged?



Synchronous switching
Variable frequency

## Protecting the Power MOSFET

$\square$ A vertical MOSFET features a buried parasitic NPN transistor
$\square$ The collector-base junction of this transistor forms the body-diode
This «diode» can accept to avalanche in certain conditions
$\square$ Do NOT use this diode as a Transient Voltage Suppressor
$\checkmark$ Adopt a safety coefficient $k_{D}$ when chosing the maximum $V_{D S}(t)$
$\checkmark 15 \%$ derating is usually selected

$$
k_{D}=0.85
$$

$$
B V_{D S S} \times k_{D}=600 \times 0.85=510 \mathrm{~V}
$$

$$
V_{\text {clamp }}=B V_{D S S} \times k_{D}-V_{o s}-V_{i n}=115 \mathrm{~V}
$$

Take $V_{o s}$ around $15-20 \mathrm{~V}$

source
$R C D$ clamp design entry

## Inclusion of a Safety Margin

The voltage on the drain swings up to $V_{\text {clamp }}$


Capture this waveform in worst-case conditions

## The Clamp Circuit Overshoots

The clamp diode forward transit time delays the clamping action

$\square$ This spike can be lethal to the power MOSFET

## Do not Reflect too Much Voltage

The reflected voltage affects the power dissipation in the clamp

$$
P_{V_{\text {clamp }}, a v g}=\frac{1}{2} F_{s w} L_{\text {leak }} I_{\text {peak }}^{2} \frac{k_{c}}{\left(k_{c}-1\right)} \quad k_{c}=\frac{V_{\text {clamp }}}{V_{r}}
$$



If $V_{\text {clamp }}$ is too close to $V_{r}$, dissipation occurs $\rightarrow k_{c}=1.3$ to 2

## Compute the Transformer Turns Ratio

The turns ratio affects the reflected voltage...

$$
V_{\text {clamp }} \geq k_{c} \frac{\left(V_{\text {out }}+V_{f}\right)}{N} \| N \geq \frac{k_{c}\left(V_{\text {out }}+V_{f}\right)}{V_{\text {clamp }}}
$$

But also the Peak Inverse Voltage of the secondary diode

$$
\text { PIV }=V_{\text {in }} N+V_{\text {out }}
$$



Choose a $100 \%$ derating factor

If $\mathrm{PIV}=100 \mathrm{~V}$
Then $\mathrm{BV}=200 \mathrm{~V}$


Always check the margins are not violated in any operating modes

## Select the Clamp Passive Elements

The clamp resistor depends on the maximum peak current


Watch for the peak current overshoot in fault!

## Clamp Current is Smaller

Lump capacitance charge at turn off depletes the leakage energy

$\Delta I=234 \mathrm{~mA}$
$1.13^{2}=1.28$
$(0.234 / 1.84)^{*} 100=13 \% \longrightarrow$ Power is reduced by 28\%

## The Leakage Inductor Rings

This ringing can be of high frequency and is radiated-EMI rich


It can also forward-bias the MOSFET body diode
$\square$ Damp it!

## Fighting Parasitic Ringing - part I

The installed resistor reduces the ringing on the drain


$$
Q=\frac{\omega_{0} l_{\text {leak }}}{R_{\text {damp }}}=1 \quad Z_{l_{\text {cekk }}} @ f_{0}=R_{\text {damp }}
$$

## Fighting Parasitic Ringing - part II

If the series resistor is not enough, install a damper


1. Measure the ringing: $f_{0}$
2. Evaluate leakage impedance at $f_{0}$

$$
Z_{l_{\text {leak }}}=2 \pi l_{\text {leak }} f_{0}
$$

3. Make $R_{\text {damp }}=Z_{l_{\text {leak }}}$
4. Try $C_{\text {damp }}=\frac{1^{\text {teak }}}{2 \pi f_{0} R}$
5. Tweak for power dissipation

Ray Ridley - Snubber design procedure

## Effects brought by clamping action






## What Diode to Select for the Clamp?

$\square$ A fast diode is a must: MUR160 is good fit


- Can a simple 1N4007 be used in a $R C D$ clamping network?
$\square$ The answer is yes for low power applications (below 20 W )
$\square$ The long recovery time naturally damps the leakage inductor


## Be Sure the Clamp Level does not Runaway

$\square$ Watch-out for clamp voltage variations, at start-up or in short-circuit
$\square$ The main problem comes from the propagation delay!


## Check the Clamp Voltage Variations



## A Zener or TVS to Hard Clamp the Voltage

- TVS do not suffer from voltage runaways in fault conditions


$\square$ The TVS improves the efficiency in standby but degrades EMI
* It costs around 5 cents...


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## What Control Scheme?

Two control scheme coexist, current-mode and voltage-mode


## Operating waveforms are identical



Ac -transfer functions differ

## Voltage-Mode Control

$\square$ Voltage mode uses a ramp to generate the duty-ratio
The error voltage directly adjusts the duty-ratio


## Voltage-Mode Control

## PROs

Does not need the inductor current information
> Can go to very small duty-ratio
CCM operation without sub-harmonic instabilities
$>$ No need for slope compensation, current limit unaffected

## CONs

No inherent input line feedforward (weak audio susceptibility)
> Cannot use small bulk capacitor, bad ripple rejection

- $2^{\text {nd }}$-order system in CCM: mode transition can be a problem
$\square$ Limited integrated circuit offer


## Peak-Current-Mode Control

- Current mode uses the inductor current information as a ramp

The error voltage adjusts the inductor peak current
$\square$ The duty-ratio is indirectly controlled


## Peak-Current-Mode Control

## PROs

Inherent pulse-by-pulse current limitation

- Natural input line rejection

Mode transition DCM to CCM is easy
$>$ Converter remains a $1^{\text {st }}$-order system at low frequency
$\square$ Widest offer on the market: a really popular technique!

## CONs

Leading Edge Blanking limits the minimum duty-ratio
$\square$ Requires slope compensation against sub-harmonic oscillations
> Additionnal ramp affects the available maximum peak current
$\square$ Current sense can sometimes be a problem (floating sense)

## A Dirty Inductor Current Signal

The inductor current is sensed with a resistor, a transformer... This information is affected by parasitics: false tripping possible!


## The LEB Cleanses the Signal

- A circuit blinds the controller at turn-on for a small time ( $\approx 250 \mathrm{~ns}$ )
$\square$ It conveys the signal afterwards: Leading Edge Blanking



## It Limits the Minimum Duty-Ratio

During the LEB duration, the controller is completely blind!
In output winding short-circuits, failures are likely to occur


## If the Primary Inductor is too Low...

$\square$ In short-circuit situations, you reflect the diode forward drop


If you hit the minimum on-time, you cannot limit the current!

## The Primary Current Runs out of Control

$\square$ The current current climbs cycle by cycle until smoke appears!



## Sub-Harmonic Oscillations

Ac analysis shows a first-order system at $f_{c} \ll F_{s w} / 2$
$>$ No $L C$ peaking anymore as in CCM voltage mode
> But a subharmonic peaking at $F_{s w} / 2$ now appears



Flyback power stage in CCM

## Instability Depends on Duty-Ratio

$\square$ The condition for instability is: CCM operation + duty-ratio > 50\%


## Instability Depends on Duty-Ratio

$\square$ With a duty-ratio below $50 \%$, perturbation naturally dies out ...


Duty-ratio $<50 \%$


Duty-ratio $>50 \%$

## The Cure is in the Ramp

Injecting a ramp on the feedback signal, damping is obtained


## A Model to Simulate a Flyback Converter

$\square$ A SPICE model can predict subharmonic instabilities


## Simulation Results of the CCM Flyback

$\square$ As ramp is injected, the double-pole $Q$ is damped
$\square$ Injecting more ramp turns the converter into voltage-mode



## Modern Circuits Include Slope Compensation

$\square$ A simple resistor in series with current sense resistor does the job


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## Modulation Strategies

The most popular modulation strategy is trailing-edge


Trailing edge modulation

Leading-edge modulation often appears in post-regulators


## Fixed Frequency Operation

$\square$ The vast majority of converters use fixed-frequency operation
$>$ Switching losses depend on frequency: high frequency, high losses!
$\rightarrow$ Capacitive losses are a brake to efficiency improvement
$>$ CCM operation induces high losses on the secondary diode
$>$ Potential shoot-trough hampers synchronous rectification
$>$ The Right Half-Plane Zero severely limits the available bandwidth


## The Right-Half-Plane Zero

$\square$ In a CCM flyback, $I_{\text {out }}$ is delivered during the off-time:


$\square$ If $D$ brutally increases, $D^{\prime}$ reduces and $I_{\text {out }}$ drops!
$\square$ What matters is the inductor current slew-rate $\longrightarrow\left\langle\frac{d v_{L}(t)}{d t}\right\rangle$

## Processing the Output Power Demand

$\square$ If $i_{L}(t)$ can rapidly change, $I_{\text {out }}$ increases when $D$ goes up


## Failing to Increase the Current in Time

If $i_{L}(t)$ is limited because of a big $L_{p}, I_{\text {out }}$ drops when $D$ increases


$$
d=58.3 \%
$$



## The RHPZ is a Positive Root

$\square$ Small-signal equations can help us to formalize it


Voltage mode or current mode, the RHPZ remains the same

## Simulating the RHPZ

To limit the effects of the RHPZ, limit the duty ratio slew-rate
Choose a crossover frequency equal to 20-30\% of RHPZ position

- A simple RHPZ can be easily simulated:



## A Zero Producing a Phase Lag

With a RHPZ we have a boost in gain but a lag in phase!


## Is There a RHPZ in DCM?

- A RHPZ also exists in DCM boost, buck-boost converters...


When $D_{1}$ increases, $\left[D_{1}, D_{2}\right]$ stays constant but $D_{3}$ shrinks

## Is There a RHPZ in DCM?

The triangle is simply shifted to the right by $\hat{d}_{1}$


The refueling time of the capacitor is delayed and a drop occurs

## Is There a RHPZ in DCM?

If $D$ increases, the diode current is delayed by $\hat{d}_{1}$




## A Large-Signal Model is Available

$\square$ Averaged models can predict the DCM RHPZ


## The Model Predicts it!

$\square$ Averaged models can predict the DCM RHPZ


## Going to Variable Frequency

$\square$ More converters are using variable-frequency operation
$\square$ This is known as Quasi-Square Wave Resonant mode: QR
$>$ Valley switching ensures extremely low capacitive losses
$>$ DCM operation saves losses on the secondary diode
$>$ Easier synchronous rectification
$>$ The Right Half-Plane Zero is pushed to high frequencies


## What is the Principle of Operation?

The drain-source signal is made of peaks and valleys
$\square$ A valley presence means:
> The drain is at a minimum level, capacitors are naturally discharged
$>$ The converter is operating in the discontinuous conduction mode


## A QR Circuit Does not Need a Clock

The system is a self-oscillating current-mode converter


## A Winding is Used to Detect Core Reset

When the flux returns to zero, the aux. voltage drops
$\square$ Discontinuous Mode is always maintained


## The Frequency Linearly Changes

$\square$ As the peak current and the on-slope vary, $T_{s w}$ changes


Excellent behavior in short-circuit conditions!

## The Excursion Can be Quite Large

$\square$ In heavy load low-line conditions, $F_{s w}$ decreases
$\square$ In light-load and high-line operations, $F_{s w}$ can go very high

$\square$ EMI and switching losses are at stake as $F_{s w}$ goes up
$\square$ Standby power obviously suffers from this condition

## In a Bounded System Discrete Jumps

$\square$ As the load gets lighter, the frequency goes to the sky
Modern controllers fold the frequency back with a VCO
$\square$ Problem, the only places to re-start are valleys: discrete jumps


## New Controllers Lock in the Valleys

To prevent the noise, the NCP1380 locks the valley
The current is allowed to move within a certain limit
When it exceeds this limit, the controller selects a new valley
$\square$ As the load gets lighter, a VCO takes over and reduce $F_{s w}$


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## What is The Problem?

$\square$ A converter is designed to operate on wide mains -85 to 265 V rms
It can deliver a maximum power before protection trips
$>$ The maximum power delivered at high line is larger than that at low line


85 V rms to 265 V rms


Increase load until protection trip.

## What Does the Standard Say?

There is a test called Limited Power Source, LPS
$\square$ The maximum power the converter can deliver must be clamped
$\square$ If clamped, the manufacturer can use inferior fire proofing materials

| Output Voltage <br> $V_{\text {out }}(\mathrm{V})$ |  | Output Current <br> $I_{\text {out }}$ | Apparent Power <br>  |
| :---: | :---: | :---: | :---: |
| $V_{\text {rms }}$ | $V_{\text {de }}$ |  | $S(\mathrm{VA})$ |

$19-\mathrm{V}$ adapter, $I_{\text {out }, \text { max }}=5 \mathrm{~A}$

IEC950 safety standard

## Why the Power Runs Away in a Flyback?

The inductor current slope increases at high line.

The controller takes time to react to an overcurrent situation.

The inductor current keeps growing until the MOSFET turns off.

The overshoot is larger at higher slopes (High $V_{i n}$ )


## The Effect in a DCM Converter

- A flyback converter operated in DCM obeys the formula:

$$
P_{\text {out }}=\frac{1}{2} L_{p} I_{\text {peak, max }}^{2} F_{s w} \eta
$$


$\square$ As $L_{p}$ and $F_{s w}$ are fixed, $I_{p e a k, \text { max }}$ changes with line input

$$
I_{\text {peak }, \text { max }, L L}=\frac{V_{\text {sense }}}{R_{\text {sense }}}+\frac{V_{\text {in }, L L}}{L_{p}} t_{\text {prop }} \quad I_{\text {peak }, \text { max }, H L}=\frac{V_{\text {sense }}}{R_{\text {sense }}}+\frac{V_{\text {in }, H L}}{L_{p}} t_{\text {prop }}
$$

Low line
High line

$$
\frac{\Delta I_{\text {peak }}}{I_{\text {peak, max }, H L}}=\frac{V_{\text {in, HL }}-V_{\text {in,LLL }}}{\frac{L_{p} V_{\text {sense }}}{t_{\text {prop }} R_{\text {sense }}}+V_{\text {in, LL }}} \quad \xrightarrow[(1.13)^{2}=1.28]{\longrightarrow}
$$

A 13.5\% overshoot translates in a $28 \%$ power increase
( $\eta$ is considered constant over the range)

## The Power Increases at High Line

$\square L_{p}=250 \mu \mathrm{H}, V_{\text {sense }}=1 \mathrm{~V}, t_{\text {prop }}=350 \mathrm{~ns}, V_{\text {in, } L L}=120, \mathrm{~V}_{\text {in }, H L}=370 \mathrm{~V}, R_{\text {sense }}=$ $0.33 \Omega, F_{s w}=65 \mathrm{kHz}$


In this example, the converter stays DCM on the whole range.

## How to Compensate the Runaway?

How do we compensate this excess of power?
$>$ we reduce the maximum peak current at high line
$>$ this is called Over Power Protection - OPP



How to calculate the compensated high-line current?

* Equate low-line power with high-line power and solve for $I_{\text {peak }}$

$$
P_{\text {out }, \text { max }, H L}=\frac{1}{2} L_{p} I_{\text {peak }, \text { max }, H L}{ }^{2} F_{s w} \eta_{H L}
$$

## Reducing the Peak Current

The final inductor peak current must equal:

$$
I_{\text {peact, max }, H L}=\sqrt{\frac{2 P_{\text {out, max }, L L}}{L_{p} F_{s m} \eta_{H L}}}
$$

$\square$ The compensated setpoint must subtract the prop. delay

$$
\frac{V_{\text {sense }}}{R_{\text {sense }}}=I_{\text {peak , max }, H L}-\frac{V_{\text {in,HL}}}{L_{p}} t_{\text {prop }}
$$

The amplitude of the sensed voltage must reduce by:

$$
\Delta V=V_{\text {sense }}-\left(I_{\text {peak }, \text { max }, H L}-\frac{V_{i n, H L}}{L_{p}} t_{\text {prop }}\right) R_{\text {sense }}
$$

## For What Final Result?

Thanks to the OPP, the power stays under control


## The CCM Case is a Different Picture

In DCM, the valley current is zero, the stored energy is:

$$
E=\frac{1}{2} L_{p} I_{p e a k, \max }^{2}
$$

> The peak current runaway, alone, affects the transmitted power
In CCM, the valley current changes the formula:

$$
E=\frac{1}{2} L_{p}\left(I_{\text {peak }, \max }^{2}-I_{\text {valley }}^{2}\right)
$$



## The Converter Changes its Operating Mode

In fault mode, the converter operates in deep CCM at low line
$\square$ As the input voltage increases, the valley current decreases


## Computing the Transmitted Power in CCM

$\square$ First, we write the $t_{o n}$ and $t_{o f f}$ equations in CCM


$$
I_{\text {peak }}=\underset{\text { valley }}{I_{\text {(1) }}}+\frac{V_{\text {in }}}{L_{p}} t_{o n} \quad I_{\text {valley }}=I_{\text {peak }}-\frac{\left(V_{\text {out }}+V_{f}\right)}{N L_{p}} t_{o f f} \quad T_{s w}=t_{o n}+t_{o f f}
$$

## Solving for the Valley Current

$\square$ By combining the 3 equations, we have:

$$
t_{o n}=\frac{L_{p}\left(I_{\text {peak }}-I_{\text {valley }}\right)}{V_{i n}} \quad t_{o f f}=T_{s w}-t_{o n}=T_{s w}-\frac{L_{p}\left(I_{\text {peak }}-I_{\text {valley }}\right)}{V_{i n}}
$$

$\square$ Replace $t_{o f f}$ in (2):

$$
I_{\text {valley }}=I_{\text {peak }}-\frac{\left(V_{f}+V_{\text {out }}\right)\left(I_{\text {valley }} L_{p}-I_{\text {peak }} L_{p}+T_{\text {sw }} V_{\text {in }}\right)}{L_{p} N V_{\text {in }}}
$$

$\square$ Solve for $I_{\text {valley }}$ :

## Identifying the Operating Mode

Having the ripple on hand, we can confirm the mode:


## Evaluating the Power in CCM

$\square L_{p}=600 \mu \mathrm{H}, V_{\text {sense }}=1 \mathrm{~V}, t_{\text {prop }}=350 \mathrm{~ns}, V_{\text {in, } L L}=120, \mathrm{~V}_{\text {in }, H L}=370 \mathrm{~V}, R_{\text {sense }}=0.33 \Omega, F_{\text {sw }}=65 \mathrm{kHz}$

$$
\begin{aligned}
P_{\max , L L} & =\frac{1}{2} L_{p}\left(I_{\text {peak }, \max , L L}^{2}-I_{\text {valley }, L L}^{2}\right) F_{s w} \eta_{L L} \approx 76 \mathrm{~W} \\
P_{\max , H L} & =\frac{1}{2} L_{p}\left({I_{p e a k, \max , H L}}^{2}-{I_{v a l l e y, H L}}^{2}\right) F_{s w} \eta_{H L}=104 \mathrm{~W}
\end{aligned}
$$



## Reducing the Peak Current at High Line

If we lower the peak at high line, the ripple remains the same


We can re-write the flyback power formula to include the ripple

$$
P_{\text {max }, H L}=\frac{1}{2} L_{p}(I_{\text {peak }, \text { max }, H L}{ }^{2}-(\underbrace{I_{\text {peak, , max }, H L}-\Delta I_{L, H L}}_{\text {oin DCM }})^{2}) F_{s w} \eta_{H L}
$$

## We Want to Limit the High-Line Power

We can force the high-line power to match that of low line

$$
P_{\text {max }, L L}=\frac{1}{2} L_{p}\left(I_{\text {peak }, \text { max }, H L}{ }^{2}-\left(I_{\text {peak, ,max }, H L}-\Delta I_{L, H L}\right)^{2}\right) F_{s w} \eta_{H L}
$$

I From there, we can extract the compensated peak current value

$$
I_{\text {peal, }, \text { max }, H L}=\frac{F_{s w} L_{p} \eta_{H H} \Delta I_{L, H L}^{2}+2 P_{\max , L L}}{2 F_{s w} L_{p} \eta_{H L} \Delta I_{L, H L}}
$$

$\square$ As this is the new setpoint, prop. delay contribution must be removed

$$
\Delta V=V_{\text {sense }}-\left(I_{\text {peak }, \text { max }, H L}-\frac{V_{i n, H L}}{L_{p}} t_{\text {prop }}\right) R_{\text {sense }}
$$

I After compensation, the peak current setpoint at high line becomes

$$
I_{\text {peak }, \text { max }, \text { HL }}=\frac{V_{\text {sense }}-\Delta V}{R_{\text {sense }}}+\frac{V_{i n, H L}}{L_{p}} t_{\text {prop }}
$$

## What is the Final Result?

The high line power now respects the LPS limit


## What Practical Solutions?

$\square$ There are several possibilities to reduce the peak current

1. Offset the current sense signal in the CS pin:

2. Reduce the peak limit as $V_{\text {in }}$ increases


- easy to do
- affects the no-load stand-by power
- affects light-load efficiency
- implemented at IC level
- does not affect the noload stand-by power
- does not affect lightload efficiency


## Build an Offset on the CS Pin

- This offset must be proportional to the input voltage


Both options degrade light-load operation because of the offset

## OPP Implementation in the NCP1250

The NCP1250 implement a non-dissipative OPP circuitry

$\square$ The auxiliary swings to $-V_{i n}$ and reduces the setpoint $\rightarrow$ OPP

## Checking the Results

Let us check on a real 19-V adapter built with the NCP1250

$$
\begin{aligned}
& L_{p}=600 \mu \mathrm{H}, V_{\text {sense }}=1 \mathrm{~V}, t_{\text {prop }}=350 \mathrm{~ns}, V_{\text {in }, L L}=120, \mathrm{~V}_{\text {in, }, \mathrm{HL}}=370 \mathrm{~V} \\
& R_{\text {sense }}=0.33 \Omega, F_{\text {sw }}=65 \mathrm{kHz}, V_{\text {clamp }}=90 \mathrm{~V}, l_{l}=2.2 \mu \mathrm{H}, N=0.25
\end{aligned}
$$



Without any OPP compensation, we have:

$$
I_{\text {out }, \text { max }, L L}=4.1 \mathrm{~A} \quad I_{\text {out , max }, H L}=5.7 \mathrm{~A}
$$

$\square$ Once OPP has been implemented:
$P_{\text {out }, L L} \approx 72 \mathrm{~W}$ so $I_{\text {out }, L L}=3.8 \mathrm{~A} \quad P_{\text {out }, H L} \approx 78 \mathrm{~W}$ so $I_{\text {out }, H L}=4.1 \mathrm{~A}$

## Course Agenda

$\square$ The Flyback Converter
$\square$ The Parasitic Elements
$\square$ How These Parasitics Affect your Design?
$\square$ Current-Mode is the Most Popular Scheme
$\square$ Fixed or Variable Frequency?
$\square$ More Power than Needed
$\square$ The Frequency Response
$\square$ Compensating With the TL431

## Small-Signal Analysis

Loop instability is a common issue in production
D Due to time pressure, designers often use trial and error
$>$ no indication on design margins
$>$ offenders are ignored, robustness is at stake


* Understand and counteract their variations when building $G(s)$


## There are Two Options

Analytical analysis of the power stage:
$\checkmark$ best to see where the offenders are hidden (ESR, opto pole etc.)
$\checkmark$ equations are complex but litterature abounds

* transfer function are for DCM or CCM
* difficult to predict transient response
$\square$ SPICE models:
$\checkmark$ easy-to-implement averaged models
$\checkmark$ can work in ac or transient mode
$\checkmark$ easily transition between CCM and DCM
* do not explictly disclose the position of poles and zeros


A measurement on the bench is mandatory, whatever you choose!

## Analytical Analysis

Y You must first characterize the "plant" transfer function
$>$ what are your power stage ac characteristics?


$$
H(s)=\frac{V_{\text {out }}(s)}{v_{c}(s)}
$$

Current-mode control

$$
H(s)=\frac{V_{\text {out }}(s)}{d(s)}
$$

Voltage-mode control

## How do we Stabilize a Converter?

We need a high gain at dc for a low static error
We want a sufficiently high crossover frequency for response speed
$>$ Shape the compensator $\mathrm{G}(\mathrm{s})$ to build phase and gain margins!


## How much phase margin to chose?

$\square$ a $Q$ factor of 0.5 (critical response) implies a $\varphi_{m}$ of $76^{\circ}$
$\square$ a $45^{\circ} \varphi_{m}$ corresponds to a $Q$ of 1.2: oscillatory response!


phase margin depends on the needed response: fast, no overshoot...
$\square$ good practice is to shoot for $60^{\circ}$ and make sure $\varphi_{m}$ always $>45^{\circ}$

## What Compensator Types do we Need?

$\square$ There are basically 3 compensator types:
$>$ type 1, 1 pole at the origin, no phase boost
$>$ type 2, 1 pole at the origin, 1 zero, 1 pole. Phase boost up to $90^{\circ}$
$>$ type 3,1 pole at the origin, 1 zero pair, 1 pole pair. Boost up to $180^{\circ}$


Type 1


Type 2


Type 3

## Fixed-Frequency Current-Mode

First, check the operating mode, CCM or DCM?
$L_{p, \text { corit }}=\frac{R_{\text {ioad }}}{2 F_{\text {sw }} N^{2}}\left(\frac{V_{\text {in }}}{V_{\text {in }}+\frac{V_{\text {out }}}{N}}\right)^{2} L_{p}>L_{p, \text { crit }}$ ? Yes, CCM else DCM
$\square$ Assume CCM, compute the duty-ratio: $D=\frac{V_{\text {out }}}{V_{\text {out }}+N V_{\text {in }}}$
$\square$ Compute $M$ and $\tau_{L}: M=\frac{V_{\text {out }}}{N V_{\text {in }}} \tau_{L}=\frac{2 L_{p} N^{2}}{R_{\text {toad }} T_{\text {sw }}}$
$\square$ Evaluate the dc gain and poles/zeros positions:

$$
G_{0}=\frac{R_{\text {load }}}{R_{\text {sense }} G_{F B} N} \frac{1}{\frac{(1-D)^{2}}{\tau_{L}}+2 M+1}
$$

## Fixed-Frequency Current-Mode

$\square$ Compute the poles/zeros positions:

$$
f_{z_{1}}=\frac{1}{2 \pi R_{\text {ESR }} C_{\text {out }}} \quad f_{z_{2}}=\frac{(1-D)^{2} R_{\text {load }}}{2 \pi D L_{p} N^{2}} \quad f_{p_{1}}=\frac{\frac{(1-D)^{3}}{\tau_{L}}+1+D}{2 \pi R_{\text {load }} C_{\text {out }}}
$$

- Check the quality coefficient at $F_{s w} / 2$

$$
S_{n}=\frac{V_{\text {in }}}{L_{p}} R_{\text {sense }} \quad \begin{gathered}
S_{e}=\left(M_{c}-1\right) S_{n} \\
1=\text { no compensation }
\end{gathered} \quad Q_{p}=\frac{1}{\pi\left(M_{c}(1-D)-0.5\right)}
$$

$\square$ Apply to formula to plot the ac response:
$\begin{aligned} & H(s) \approx G_{0}\left(1+\frac{s}{\omega_{z 1}}\right)\left(1-\frac{s}{\omega_{z 2}}\right) \\ & 3^{\text {rd }} \text { order } \longrightarrow\left(1+\frac{s}{\omega_{p 1}}\right) 1 \\ & 1+\frac{s}{\omega_{n} Q_{p}}+\frac{s^{2}}{\omega_{n}{ }^{2}}\end{aligned}$

$$
M_{c}=1+\frac{S_{e}}{S_{n}} \quad \omega_{n}=\frac{\pi}{T_{s w}}
$$

## Fixed-Frequency Current-Mode

$\square$ Extract the magnitude and the argument definitions

$$
\begin{gathered}
|H(f)|=20 \log _{10}\left[\begin{array}{c}
\left.G_{0} \frac{\sqrt{1+\left(\frac{f}{f_{z_{1}}}\right)^{2}} \sqrt{1+\left(\frac{f}{f_{2}}\right)^{2}}}{\sqrt{1+\left(\frac{f}{f_{p_{1}}}\right)^{2}}} \frac{1}{\sqrt{\left(1-\left(\frac{f}{f_{n}}\right)^{2}\right)^{2}+\left(\frac{f}{f_{n} Q_{p}}\right)^{2}}}\right] \\
\arg H(f)=\tan ^{-1}\left(\frac{f}{f_{z_{1}}}\right)-\tan ^{-1}\left(\frac{f}{f_{z_{2}}}\right)-\tan ^{-1}\left(\frac{f}{f_{p_{1}}}\right)-\tan ^{-1}\left(\frac{f}{f_{n} Q_{p}} \frac{1}{1-\left(\frac{f}{f_{n}}\right)^{2}}\right) \\
\text { RHPZ }
\end{array} .\right.
\end{gathered}
$$

$\square$ Plot them with Mathcad ${ }^{\circledR}$ for instance.

## Fixed-Frequency Current-Mode

Extract the information at the selected crossover frequency


## Fixed-Frequency Current-Mode

The compensation strategy is the following:

- compensate the gain loss at $f_{c}$ so that: $|G(3 \mathrm{kHz})|=+16.3 \mathrm{~dB}$
- evaluate the boost in phase at $f_{c}$ to get phase $70^{\circ}$ margin:

$$
\text { Boost }=\mathrm{PM}-\operatorname{argH}\left(f_{c}\right)-90=3.15^{\circ}
$$

Boost $=0$ select type 1 - origin pole
$\longrightarrow$ Boost $<90^{\circ}$ select type 2 - origin pole, 1 pole, 1 zero

- k-factor can be used to place the pole and the zero

$$
\begin{array}{ll}
k=\tan \left(\frac{\text { boost }}{2}+45\right) \approx 1 \longrightarrow \text { poles and zeros are coincident } \\
f_{p k 1}=k f_{c}=1 \times 3 k=3 \mathrm{kHz} & f_{z k 1}=\frac{f_{c}}{k}=\frac{3 k}{1}=3 \mathrm{kHz}
\end{array}
$$

## Fixed-Frequency Current-Mode

$\square$ Plot the compensator transfer function


## Fixed-Frequency Current-Mode

$\square$ Plot the loop gain transfer function and check the margins

$\square$ Sweep ESR, $C_{\text {out }}, R_{\text {load }}$ and verify the results

## Fixed-Frequency Current-Mode

In case the converter transitions to DCM, update the equation!
(
$>$ Yes, analytical analysis is long and tedious.
$>$ But, it teaches where the threats are and how to deal with!

## Variable-Frequency Current-Mode

Observing the waveforms helps us to derive an average model



It gives birth to a large-signal model


$$
\begin{aligned}
V_{c} & =\frac{2 R_{i} P_{\text {out }}\left(V_{\text {out }}+N V_{\text {in }}\right)}{V_{\text {in }} V_{\text {out }}} \\
T_{\text {sw }} & =\frac{V_{c} L_{p}}{R_{i}}\left(\frac{1}{V_{\text {in }}}+\frac{N}{V_{\text {out }}}\right) \\
d_{1} & =\frac{2 P_{\text {out }} R_{i}}{V_{c} V_{\text {in }}}
\end{aligned}
$$

## Variable-Frequency Current-Mode

L Linearization is needed to get a small-signal model
Implement this small-signal model in a flyback configuration

http://cbasso.pagesperso-orange.fr/Spice.htm

## Variable-Frequency Current-Mode

$\square$ Derive the transfer function and isolate poles and zeros
$\frac{\hat{v}_{\text {out }}(s)}{\hat{v}_{c}(s)}=G_{0} \frac{\left(1+\frac{s}{s_{z 1}}\right)\left(1-\frac{s}{s_{z 2}}\right)}{{ }_{\text {st order }} \longrightarrow\left(1+\frac{s}{s_{p 1}}\right)}$
$G_{0}=\frac{R_{\text {load }} D i v}{2 N R_{i}\left(\frac{2 V_{\text {out }}}{N V_{\text {in }}}+1\right)}$
$\square$ Then plot the function


$$
\begin{aligned}
& f_{p_{1}}=\frac{1}{2 \pi R_{\text {oad }} C_{\text {out }}} \frac{2 M+1}{M+1} \\
& f_{z_{1}}=\frac{1}{2 \pi R_{\text {ESR }} C_{\text {out }}}
\end{aligned}
$$

$$
f_{z_{z}}=\frac{R_{\text {lad }}}{2 \pi N^{2} L_{p}} \frac{1}{M(1+M)}
$$



Tailor $G(s)$ to get the desired $f_{c}$

## Use a SPICE Model to Stabilize the Converter



## Unveil the Transfer Function in a Second



## Course Agenda

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## How is regulation performed?

$\square$ Text books only describe op amps in compensators...


The market reality is different: the TL431 rules!


## The TL431 Programmable Zener

The TL431 is the most popular choice in nowadays designs
It associates an open-collector op amp and a reference voltage
$\square$ The internal circuitry is self-supplied from the cathode current
When the R node exceeds 2.5 V , it sinks current from its cathode


The TL431 is a shunt regulator

## A Rabbit and a (French) Snail...

$\square$ The TL431 lends itself very well to optocoupler control

$\square R_{L E D}$ must leave enough headroom over the TL431: upper limit!

## Understanding the Fast Lane Drawback

This LED resistor is a design limiting factor in low output voltages:

$$
R_{L E D, \text { max }} \leq \frac{V_{\text {out }}-V_{f}-V_{T L 431, \text { min }}}{V_{d d}-V_{C E, \text { sat }}+I_{\text {bias }} \mathrm{CTR}_{\text {min }} R_{\text {pullup }}} R_{\text {pullup }} \mathrm{CTR}_{\text {min }}
$$

When the capacitor $C_{1}$ is a short-circuit, $R_{L E D}$ fixes the fast lane gain


## The Static Gain Limit

Let us assume the following design:

$$
\begin{array}{lc}
V_{\text {out }}=5 \mathrm{~V} & R_{L E D, \max } \leq \frac{5-1-2.5}{4.8-0.3+1 \mathrm{~m} \times 0.3 \times 20 \mathrm{k}} \times 20 \mathrm{k} \times 0.3 \\
V_{f}=1 \mathrm{~V} \\
V_{T L 431, \min }=2.5 \mathrm{~V} & \\
V_{\text {dd }}=4.8 \mathrm{~V} & \\
V_{\text {CE,sat }}=300 \mathrm{mV} & R_{L E D, \text { max }} \leq 857 \Omega \\
I_{\text {bias }}=1 \mathrm{~mA} \\
\mathrm{CTR}_{\min }=0.3 \\
R_{\text {pullup }}=20 \mathrm{k} \Omega & G_{0}>\operatorname{CTR} \frac{R_{\text {pullupp }}}{R_{L E D}}>0.3 \frac{20}{0.857}>7 \text { or } \approx 17 \mathrm{~dB}
\end{array}
$$

In designs where $R_{L E D}$ fixes the gain, $G_{0}$ cannot be below 17 dB
$\xrightarrow{\longrightarrow}$ You cannot "amplify" by less than 17 dB

## Forbidden Compensation Areas

Y You must identify the areas where compensation is possible


## Injecting Bias Current

Make sure enough current always biases the TL431
$\square$ If not, its open-loop suffers - a 10-dB difference can be observed!



## Small-Signal Analysis

The TL431 is an open-collector op amp with a reference voltage $\square$ Neglecting the LED dynamic resistance, we have:


## Creating a High-Frequency Pole

In the previous equation we have:
$\checkmark$ a static gain $G_{0}=\operatorname{CTR} \frac{R_{\text {pulup }}}{R_{\text {LED }}}$
$\checkmark$ a $0-\mathrm{dB}$ origin pole frequency $\omega_{p o}=\frac{1}{C_{1} R_{u p p e r}}$
$\checkmark$ a zero $\omega_{\bar{z}_{1}}=\frac{1}{R_{\text {upper }} C_{1}}$
$\square$ We are missing a pole for the type 2 !


Type 2 transfer function

## Understanding the Optocoupler Pole

The optocoupler also features a parasitic capacitor
$>$ it comes in parallel with $C_{2}$ and must be accounted for


## Extracting the Pole

The optocoupler must be characterized to know where its pole is


$\square$ Adjust $V_{\text {bias }}$ to have $V_{F B}$ at 2-3 V to be in linear region, then ac sweep
The pole in this example is found at 4 kHz

$$
C_{\text {opto }}=\frac{1}{2 \pi R_{\text {pullup }} f_{\text {pole }}}=\frac{1}{6.28 \times 20 k \times 4 k} \approx 2 \mathrm{nF}
$$



## The TL431 in a Type 1 Compensator

To make a type 1 (origin pole only) neutralize the zero and the pole

$$
\begin{aligned}
& \frac{V_{F B}(s)}{V_{\text {out }}(s)}=-\frac{R_{\text {pullup }} \mathrm{CTR}}{R_{L E D}}\left[\frac{1+s R_{\text {upper }} C_{1}}{s R_{\text {upper }} C_{1}\left(1+s R_{\text {pullup }} C_{2}\right)}\right]
\end{aligned}
$$

$$
\begin{aligned}
& \omega_{p o}=\frac{\mathrm{CTR}}{C_{2} R_{L E D}} \| C_{2}=\frac{\mathrm{CTR}}{2 \pi f_{p o} R_{\text {LED }}}
\end{aligned}
$$

O Once neutralized, you are left with an integrator

$$
G(s)=\frac{1}{\frac{s}{\omega_{p o}}} \rightarrow\left|G\left(f_{c}\right)\right|=\frac{f_{p o}}{f_{c}} \rightarrow f_{p o}=G_{f_{c}} f_{c} \longrightarrow C_{2}=\frac{\mathrm{CTR}}{2 \pi G_{f_{c}} f_{c} R_{L E D}}
$$

## A Type 1 Design Example

$\square$ We want a $5-\mathrm{dB}$ gain at 5 kHz to stabilize the $5-\mathrm{V}$ converter

$$
\begin{aligned}
& V_{\text {out }}=5 \mathrm{~V} \\
& V_{f}=1 \mathrm{~V} \\
& V_{T L 431, \text { min }}=2.5 \mathrm{~V} \\
& V_{d d}=4.8 \mathrm{~V} \\
& V_{C E, s t}=300 \mathrm{mV} \\
& I_{\text {bias }}=1 \mathrm{~mA} \\
& \mathrm{CTR}_{\text {min }}=0.3 \\
& R_{\text {pullup }}=20 \mathrm{k} \Omega \\
& \left.\begin{array}{l}
G_{f c}=10^{\frac{5}{20}}=1.77 \\
f_{c}=5 \mathrm{kHz}
\end{array}\right\} C_{2}=\frac{\mathrm{CTR}}{2 \pi G_{f_{c}} f_{c} R_{L E D}}=\frac{0.3}{6.28 \times 1.77 \times 5 \mathrm{k} \times 728} \approx 7.4 \mathrm{nF} \\
& C_{\text {opto }}=2 \mathrm{nF} \\
& \xrightarrow{\longrightarrow} \longrightarrow C=7.4 n-2 n=5.4 \mathrm{nF} \quad C_{1}=\frac{R_{\text {pullup }}}{R_{\text {upper }}} C_{2} \approx 14.7 \mathrm{nF}
\end{aligned}
$$

## Simulation of the Type 1

$\square$ SPICE can simulate the design - automate elements calculations...


## Type 1 Simulation Results

The pullup resistor is $1 \mathrm{k} \Omega$ and the target now reaches 5 dB


## The TL431 in a Type 2 Compensator

Our first equation was already a type 2 definition, we are all set!

$\square$ Just make sure the optocoupler contribution is involved...

## Deriving Component Values for the Type 2

$\square$ You need to provide a $15-\mathrm{dB}$ gain at 5 kHz with a $50^{\circ}$ boost

$$
\begin{aligned}
& f_{p}=\left[\tan (\text { boost })+\sqrt{\tan ^{2}(\text { boost })+1}\right] f_{c}=2.74 \times 5 \mathrm{k}=13.7 \mathrm{kHz} \\
& f_{z}=f_{c}^{2} / f_{p}=25 \mathrm{k} / 13.7 \mathrm{k} \approx 1.8 \mathrm{kHz} \quad G_{0}=\operatorname{CTR} \frac{R_{\text {pullup }}}{R_{L E D}}=10^{15 / 20}=5.62
\end{aligned}
$$

With a $250-\mu \mathrm{A}$ bridge current, the divider resistor is made of:

$$
R_{\text {lower }}=2.5 / 250 u=10 \mathrm{k} \Omega \quad R_{1}=(12-2.5) / 250 u=38 \mathrm{k} \Omega
$$

The pole and zero respectively depend on $R_{\text {pullup }}$ and $R_{1}$ :

$$
C_{2}=1 / 2 \pi f_{p} R_{\text {pullup }}=581 \mathrm{pF} \quad C_{1}=1 / 2 \pi f_{z} R_{1}=2.3 \mathrm{nF}
$$

$\square$ The LED resistor depends on the needed mid-band gain:

$$
R_{L E D}=\frac{R_{\text {pullup }} \mathrm{CTR}}{G_{0}}=1.06 \mathrm{k} \Omega \xrightarrow{\mathrm{ok}} \quad R_{L E D, \text { max }} \leq 4.85 \mathrm{k} \Omega
$$

## Checking the Optocoupler Contribution

The optocoupler is still at a $4-\mathrm{kHz}$ frequency:


- Type 2 pole capacitor calculation requires a $581-\mathrm{pF}$ cap.!
$\square \square$ The bandwidth cannot be reached, reduce $f_{c}$ !
$\square$ For noise purposes, we want a minimum of 100 pF for $C$
With a total capacitance of 2.1 nF , the highest pole can be:

$$
f_{\text {pole }}=\frac{1}{2 \pi R_{\text {pullup }} C}=\frac{1}{6.28 \times 20 k \times 2.1 n}=3.8 \mathrm{kHz}
$$

$\square$ For a $50^{\circ}$ phase boost and a $3.8-\mathrm{kHz}$ pole, the crossover must be:

$$
f_{c}=\frac{f_{p}}{\tan (\text { boost })+\sqrt{\tan ^{2}(\text { boost })+1}} \approx 1.4 \mathrm{kHz}
$$

## Placing the Zero in the Transfer Function

The zero is then simply obtained:

$$
f_{z}=\frac{f_{c}^{2}}{f_{p}}=516 \mathrm{~Hz}
$$

We can re-derive the component values and check they are ok

$$
C_{2}=1 / 2 \pi f_{p} R_{\text {pullup }}=2.1 \mathrm{nF} \quad C_{1}=1 / 2 \pi f_{z} R_{1}=8.1 \mathrm{nF}
$$

- Given the 2-nF optocoupler capacitor, we just add 100 pF

In this example, $R_{L E D, \max }$ is $4.85 \mathrm{k} \Omega$
$G_{0}>\operatorname{CTR} \frac{R_{\text {pulupp }}}{R_{L E D}}>0.3 \frac{20}{4.85}>1.2$ or $\approx 1.8 \mathrm{~dB}$
$\square$ You cannot use this type 2 if an attenuation is required at $f_{c}$ !

## TL431 type 2 Design Example

$\square$ The $1-\mathrm{dB}$ gain difference is linked to $R_{d}$ and the bias current


ON Semiconductor ${ }^{\circledR}$

## Design Example 1 - a Single-Stage PFC

The single-stage PFC is often used in LED applications
It combines isolation, current-regulation and power factor correction
$\square$ Here, a constant on-time BCM controler, the NCP1608, is used


## Design Example 1 - a Single-Stage PFC

O Once the converter elements are known, ac-sweep the circuit $\square$ Select a crossover low enough to reject the ripple, e.g. 20 Hz



## Design Example 1 - a Single-Stage PFC

Given the low phase lag, a type 1 can be chosen
$>$ Use the type 2 with fast lane removal where $f_{p}$ and $f_{z}$ are coincident




## Design Example 1 - a Single-Stage PFC

- A transient simulation helps to test the system stability



$V_{i n}=100 \mathrm{~V} \mathrm{rms}$


## Design Example 2: a DCM Flyback Converter

- We want to stabilize a 20-W DCM adapter
- $V_{\text {in }}=85$ to 265 V rms, $V_{\text {out }}=12 \mathrm{~V} / 1.7 \mathrm{~A}$
- $F_{s w}=65 \mathrm{kHz}, R_{\text {pullup }}=20 \mathrm{k} \Omega$
- Optocoupler is SFH-615A, pole is at 6 kHz
- Cross over target is 1 kHz
] Selected controller: NCP1216

1. Obtain a power stage open-loop Bode plot, $H(s)$
2. Look for gain and phase values at cross over
3. Compensate gain and build phase at cross over, $G(s)$
4. Run a loop gain analysis to check for margins, $T(s)$
5. Test transient responses in various conditions

## Design Example 2: a DCM Flyback Converter

- Capture a SPICE schematic with an averaged model

- Look for the bias points values: $V_{\text {out }}=12 \mathrm{~V}$, ok


## Design Example 2: a DCM Flyback Converter

- Observe the open-loop Bode plot and select $f_{c}: 1 \mathrm{kHz}$



## Design example 2: a DCM flyback converter

$\square$ Apply $k$ factor or other method, get $f_{z}$ and $f_{p}$
$>f_{z}=3.5 \mathrm{kHz} f_{p}=4.5 \mathrm{kHz}$


## Design example 2: a DCM Flyback Converter

. Check loop gain and watch phase margin at $f_{c}$


## Design Example 2: a DCM Flyback Converter

- Sweep ESR values and check margins again



## Conclusion

$\square$ The flyback converter hides several parasitic elements
$\square$ Understanding where they hide and how they move is key!
$\square$ Despite CM overwhelming presence, QR designs grow
$\square$ CM is a $3^{\text {rd }}$-order system whereas QR is $1^{\text {st }}$ order
$\square$ TL431 lends itself well for compensation, watch the optocoupler!
$\square$ SPICE eases and speed-up the design
$\square$ Always check theoretical assumptions with bench measurement


