1 kW 48 V to 12 V telecom quarter-brick fixed-frequency LLC with XDPP1100 digital controller

Using digital controller XDPP1100-Q024, OptiMOS™ 6 80 V ISC033N08NM6 with 3.3 mΩ max. and OptiMOS™ 5 25 V IQE006NE2LM5 with 0.65 mΩ max.

About this document

Feedback

Scope and purpose

This document presents the design and performance of a highly efficient 1 kW fixed-frequency LLC quarter-brick converter for 48 V intermediate bus converter applications. The reference board has an input voltage range of 42~60 V DC and output voltage range of 10~15 V DC, achieving a power density of 564 W/in^3 (34.6 W/cm^3) and 97.3 percent peak efficiency. The board is capable of 80 A output current without heatsinks. A higher power level is attainable if heatsinks are mounted. The board also achieves excellent EMI performance due to the soft-switching of the LLC converter.

The LLC quarter-brick converter incorporates a primary full-bridge with OptiMOS™ 6 80 V MOSFET (ISC033N08NM6) with 3 mΩ max. , and a secondary full-bridge with OptiMOS™ 5 25 V MOSFET (**IQE006NE2LM5**) with 0.65 mΩ max. as synchronous rectifiers (SRs). The superior characteristics of Infineon's power transistors result in very low losses and hence enable high power capability with enhanced efficiency and power density. Both the primary and secondary MOSFETs are driven by EiceDRIVER™ gate driver 2EDL8124G. Infineon's digital power controller **XDPP1100-Q024**, the industry's smallest digital controller with PMBus interface, is used in the design, providing utmost flexibility in efficiency optimization, soft-start implementation and enhanced protection.

The reference board follows the standard DOSA mechanical outline for high-current quarter-bricks. It is designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components.

Intended audience

This application note is intended for power supply design engineers.

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1 Introduction and design considerations

Intermediate-bus converters (IBCs) have been widely used in telecom, data center, server and other industrial applications. The trend in IBCs has been toward increased power density with optimized cost. High efficiency is a key factor in increasing power density, because heat dissipation must be minimized. Furthermore, higher efficiency directly reduces the ownership cost during the lifetime of the converter.

IBCs provide galvanic isolation and convert 48 V bus voltage to an intermediate low-level voltage to power the downstream point-of-load voltage regulators. The optimal IBC can be fully regulated, semi-regulated or unregulated, depending on the system requirements for voltage variation range. Unregulated IBCs, also considered as DC transformers (DCX), typically achieve higher efficiency and higher power density, favorable in applications with narrow input voltage range. LLC resonant topology is a suitable candidate for unregulated intermediate bus conversion, which allows the converter to always operate at resonance, achieving optimal performance over the whole load and voltage range.

This document describes the design and performance of a 1 kW fixed-frequency LLC quarter-brick converter. It is unregulated and has a conversion ratio of about 4:1. It operates from an input voltage range of 42~60 V DC to an output voltage range of 10~15 V DC. The reference board utilizes Infineon's advanced semiconductor technologies, which enables a power density of 564 W/in^3 (34.6 W/cm^3) and 97.3 percent peak efficiency. The board is capable of 80 A output current without heatsinks. Excellent EMI performance can be achieved due to the soft-switching of the LLC converter. The board follows the standard DOSA mechanical outline for high-current quarter-bricks.

OptiMOS™ 6 80 V MOSFETs (ISC033N08NM6) is used in the primary full-bridge of the LLC quarter-brick converter. Infineon's OptiMOS™ 6 power MOSFETs utilize thin-wafer technology, offering next-generation, cutting-edge innovation, and best-in-class performance. Compared to alternative products, this family has reduced on-state resistance and improved figure-of-merit (FOM - $R_{DS(on)}$ x Q_g and Q_{gd}), allowing designers to increase efficiency and reduce system cost.[1]

OptiMOS™ 5 25 V MOSFETs (IQE006NE2LM5) is used in the secondary full-bridge as SRs. This device comes in an innovative source-down PQFN 3.3x3.3 mm package, setting an industry benchmark in MOSFET performance. The source-down technology results in major reduction of $R_{DS(on)}$ by up to 30 percent compared to current technology. The thermal resistance between junction and case is significantly improved compared to the current PQFN packages. Reduced parasitics, improved PCB losses, as well as superior thermal performance, also add significant value to contemporary engineering designs.[2]

EiceDRIVER™ gate driver 2EDL8124G is used to drive both the primary and secondary MOSFETs. 2EDL8124G is a level-shift high-side low-side dual-channel driver with 4 A source current capability. It takes in differential inputs with built-in hysteresis for enhanced noise immunity, and the inherent shoot-through protection ensures the robustness of the system.[3]

Infineon's digital power controller XDPP1100-Q024 is used in the design, providing utmost flexibility in efficiency optimization, soft-start implementation and enhanced protection. XDPP1100-Q024 is the industry's smallest digital power controller with PMBus interface, offered in a 24-pin VQFN 4x4 mm package. The device features many optimized power processing blocks and pre-programmed peripherals to enhance the performance of isolated DC-DC converters, reduce external components and minimize firmware development effort.

Introduction and design considerations

The controller also provides accurate telemetry and power management bus (PMBus 1.3) interface for system communication, advanced power conversion and monitoring. A combination of high-performance AFE, state machine-based digital control loop and an ARM® Cortex® M0 integrated in a single chip makes the XDPP1100 a highly integrated, fully programmable and fastest-time-to-market technology for modern high-end power systems, employed in telecom infrastructure, 48 V server motherboards, data center and industrial 4.0 applications.[4] Infineon offers support tools such as a complementary graphical user interface (GUI) that allows customers to configure and monitor key parameters for the XDPP1100. In addition, developers have full control of their application and firmware development process. Infineon enables designers to develop and compile their customized firmware in any commonly used ARM®-based development environment.

For further information on Infineon semiconductors see the **Infineon** website, as well as the Infineon **evaluation board** search tool, and the websites for the different implemented components:

- **OptiMOS™** power MOSFETs
- **Gate driver ICs**
- **XDP™ digital power controller**

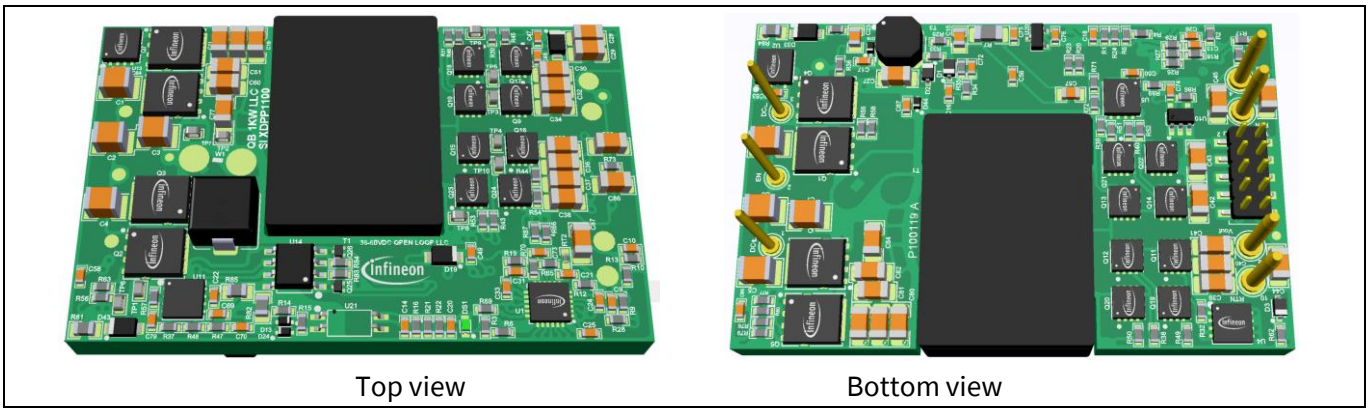


Figure 1 Infineon 1 kW fixed-frequency LLC quarter-brick converter reference board outline

1.1 System description

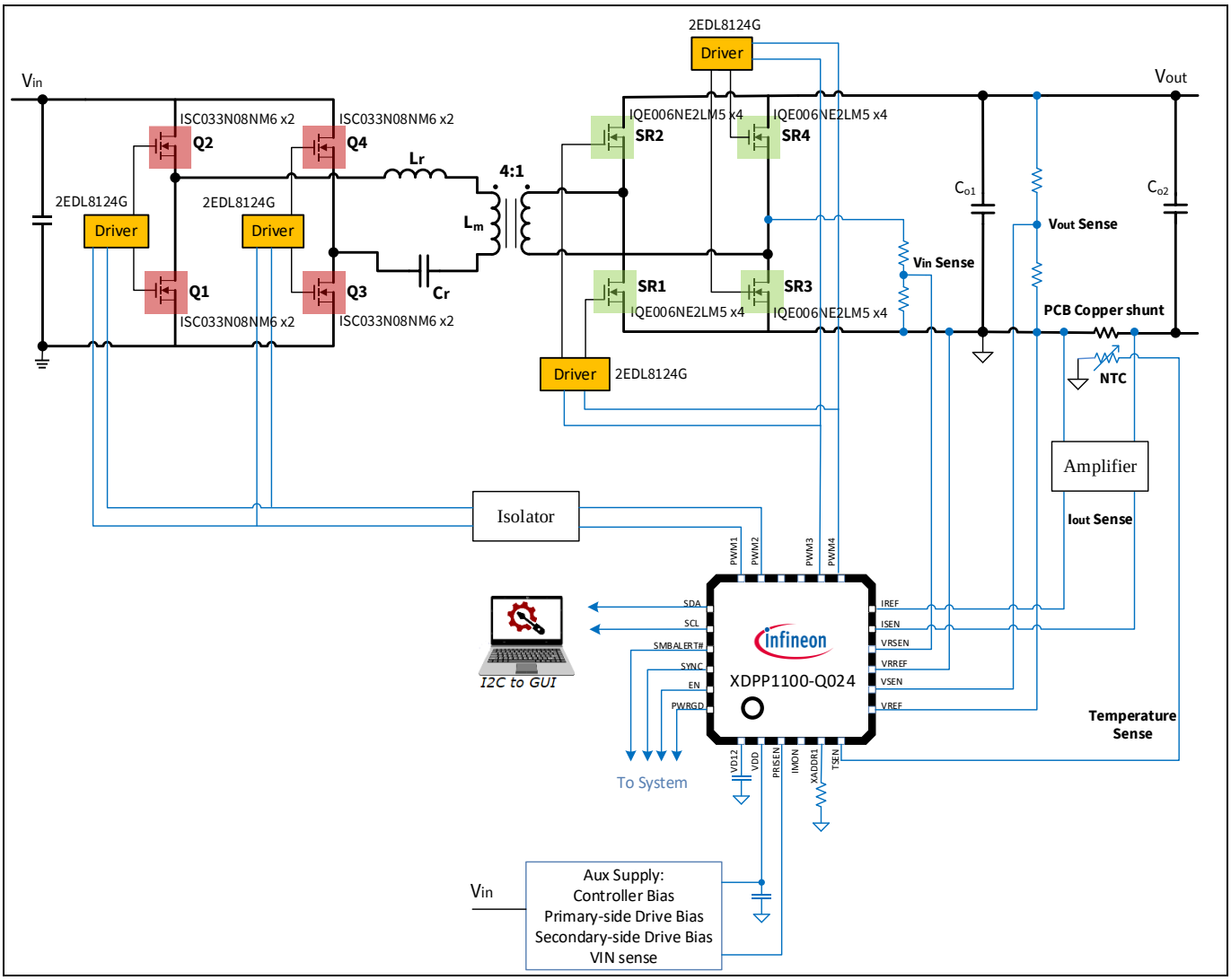


Figure 2 Infineon 1 kW fixed-frequency LLC quarter-brick converter – simplified block diagram

A block diagram of the LLC quarter-brick converter is shown in **Figure 2**. The converter consists of a primary full-bridge, a secondary full-bridge, a resonant inductor L_r, a resonant capacitor C_r and a 4:1 planar transformer. It has an input voltage range of 42~60 V DC and an output voltage range of 10~15 V DC. This converter is unregulated and operates at resonance with a fixed switching frequency. It achieves zero-voltage switching (ZVS) of all switches over the whole load and voltage range. The voltage stresses of primary FETs and secondary FETs equal the input voltage and output voltage, respectively, without ringing. Hence the 80 V MOSFET ISC033N08NM6 is used in the primary and the 25 V MOSFET IQE006NE2LM5 is used in the secondary. ISC033N08NM6 has an excellent FOM and superior switching performance. The low output capacitance reduces the required magnetizing current for ZVS operation in the LLC converter, minimizing conduction losses. IQE006NE2LM5 has an industry-leading $R_{DS(on)}$, significantly lowering the conduction losses of SRs in the LLC converter. The reduced form factor (PQFN 3.3x3.3 mm footprint) enables more FETs to be paralleled in a given space, which further reduces conduction losses and offers superior thermal management.

Introduction and design considerations

The industry's smallest digital power controller XDPP1100-Q024 is used in the design to enhance the performance, reduce external components and minimize firmware development effort. The XDPP1100-Q024 plays an important role in the fixed-frequency LLC quarter-brick converter. First, with the digital controller, the SR timing can be optimized for best efficiency. Second, the digital controller can easily implement a duty-cycle/frequency hybrid soft-start, which greatly reduces current stress during start-up. Third, the digital controller provides enhanced protections for the converter, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), and output short-circuit protection (SCP). The functions of the digital controller will be illustrated in detail in Sections 1.3, 1.4 and 1.5.

1.2 Design of resonant tank

The switching frequency f_{sw} is selected to be 310 kHz for optimal efficiency. With a fixed switching frequency, the LLC converter operates at resonance over the whole input voltage and load range. The voltage gain of the resonant tank is around 1. The design of the tank follows Eq. 1.

$$\frac{1}{2\pi\sqrt{(L_r+L_k)C_r}} = f_{sw} \quad \text{Eq. 1}$$

As no regulation is required, the values of L_r and C_r are not so critical for operation as they would be in a regulated LLC converter. From the efficiency point of view, a small L_r is preferred, as a small L_r results in small core size and low core losses. On the other hand, a too-small L_r poses challenges for start-up and short circuit protection. A certain inductance is still needed to lower the current stress during start-up and limit the current rising rate for short-circuit protection. As a compromise, 85 nH inductor LP02-800-1S is selected in this design. Note that leakage inductance L_k of the transformer adds to the total resonant inductance. As a planar transformer is implemented in the design, it gives very low and highly repeatable leakage inductance (approximately 50 nH). Resonant capacitor C_r can be calculated from Eq. 1. In practice, the exact value of C_r can be found by tuning the resonant waveforms. In this design, C_r is chosen to be 1.89 µF.

In order to achieve ZVS, magnetizing inductance L_m of the transformer needs to be small so that the magnetizing current is large enough to completely charge/discharge the output capacitance of primary FETs within the dead-time. Then the bode-diode conducts and hence ZVS can be achieved. The switching transition is shown in **Figure 3**. The calculation of maximum L_m for ZVS operation is provided in **Figure 4**.

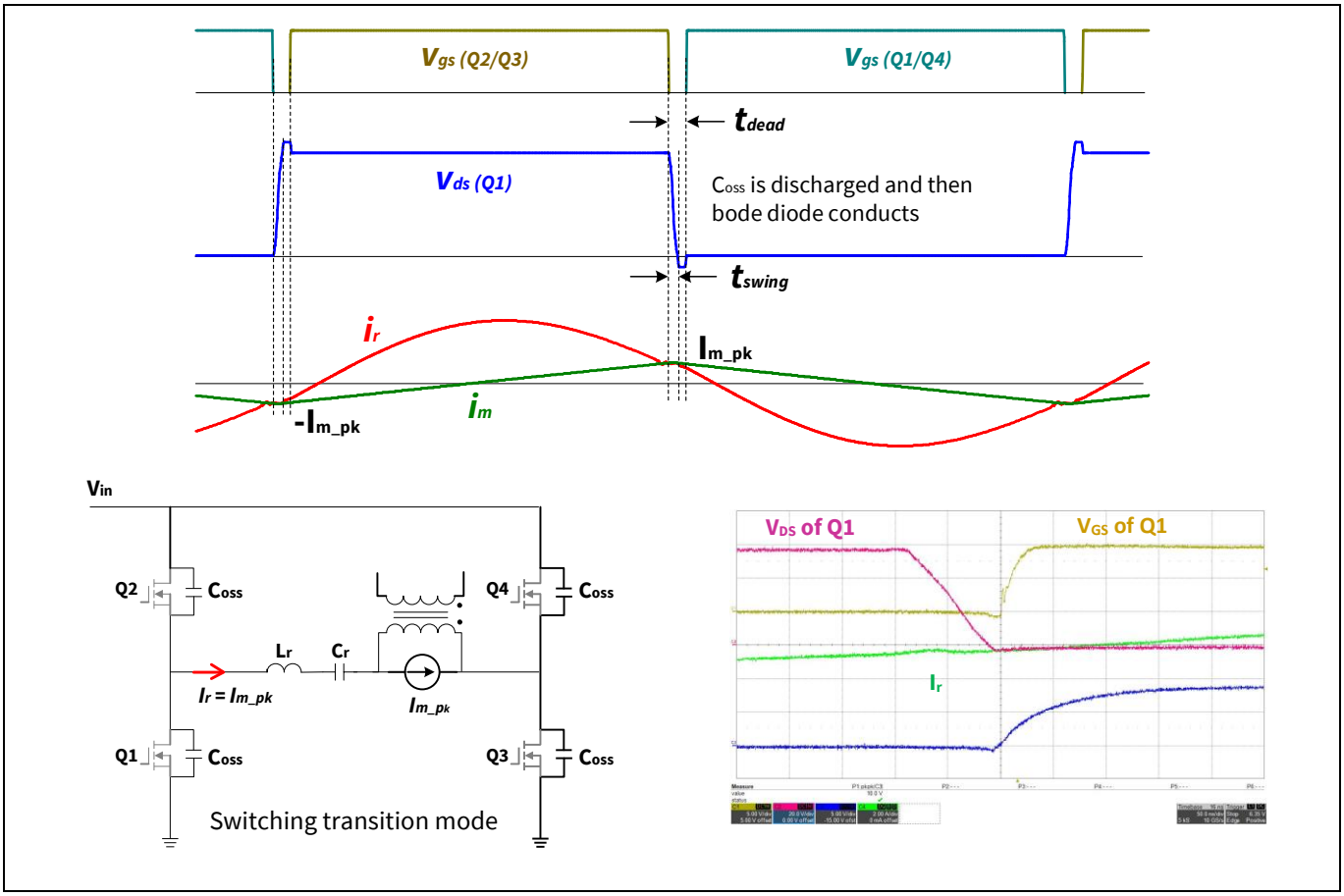


Figure 3 Switching transition

According to the magnetizing current waveform, I_{m_pk} can be calculated as follows:

$$nV_o = L_m \cdot \frac{2I_{m\_pk}}{0.5T_{sw}} \quad \Rightarrow \quad I_{m\_pk} = \frac{nV_o}{4L_m \cdot f_{sw}} \qquad \text{Eq. 2}$$

During the switching transition, C_{oss} is discharged/charged from V_{in} to zero by I_{m_pk} as follows:

$$I_{m\_pk} = 2m \cdot C_{ossAvg} \cdot \frac{V_{in}}{t_{swing}} \quad \Rightarrow \quad t_{swing} = \frac{2m \cdot C_{ossAvg} \cdot V_{in}}{I_{m\_pk}} \qquad \text{Eq. 3}$$

The dead-time must be larger than v_{ds} swing time, so that bode-diode can conduct to ensure ZVS.

$$t_{dead} > t_{swing} \qquad \text{Eq. 4}$$

Combining Eq. 2 to Eq. 4, the maximum L_m can be calculated by:

$$L_m < \frac{t_{dead} \cdot nV_o}{8m \cdot C_{ossAvg} \cdot f_{sw} \cdot V_{in}} = \frac{t_{dead}}{8m \cdot C_{ossAvg} \cdot f_{sw}} \qquad \text{Eq. 5}$$

where it is assumed $nV_o = V_{in}$ for ~100 percent efficiency

where C_{ossAvg} is average output capacitance of each FET during voltage swing, and m is the number of FETs in parallel.

Note: As C_{oss} varies with drain-source voltage, the average value of C_{oss} during voltage swing should be used.

In this design, t_{dead} = 80 ns, f_{sw} = 310 kHz, m = 2, $C_{ossAvg} \approx$ 1500 pF. According to Eq. 5, $L_m <$ 10.7 µH.

Figure 4 Calculation of maximum magnetizing inductance

The selection of dead-time has some trade-off considerations. If the dead-time is too small, higher magnetizing current is needed to charge/discharge C_{oss}, increasing conduction losses. If the dead-time is too large, effective duty-cycle is reduced, increasing circulating losses without power delivery, especially in high-frequency designs.

In this design, dead-time is selected to be 80 ns. Two ISC033N08NM6 MOSFETs are used in parallel at the primary for lower conduction losses. The average C_{oss} of each ISC033N08NM6 during v_{ds} voltage swing from V_{in} to 0 is approximately 1500 pF, which can be found in **Figure 5** from the datasheet of ISC033N08NM6. According to calculations in **Figure 4**, L_m needs to be smaller than 10.7 µH. A magnetizing inductance of 9 µH is finally chosen in the design, which is obtained by adding two layers of polyimide film tape (5 mil gap) between the transformer cores.

The voltage gain curves of the resonant tank based on this design are plotted in **Figure 6**. It verifies that the voltage gain of the tank is around 1 across the whole load range, with quite a wide tolerance to switching frequency.

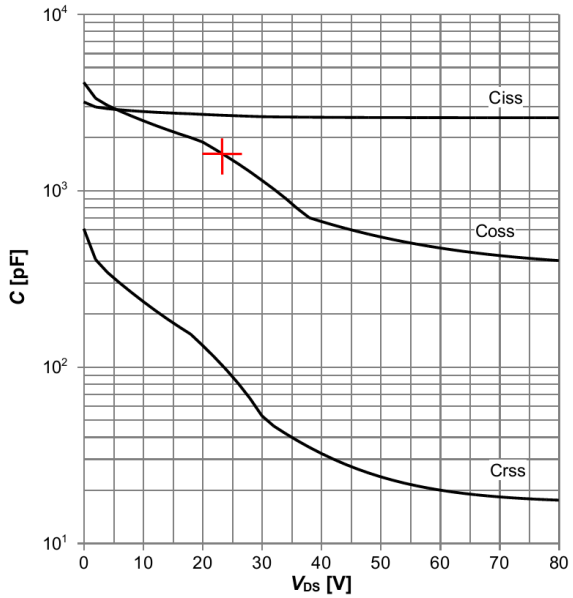


Figure 5 Capacitance curves of primary MOSFET ISC033N08NM6

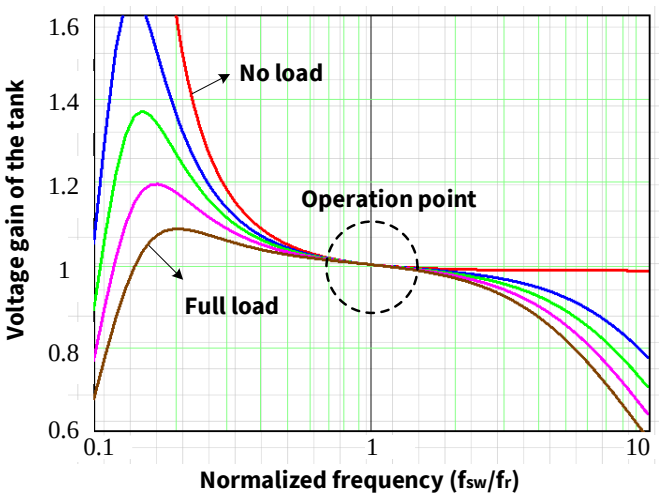


Figure 6 The voltage gain curves of the resonant tank in this fixed-frequency LLC converter

1.3 SR timing

The primary gate signals have 50 percent duty-cycle with dead-time. The secondary SR timing is critical for efficiency optimization. Typically multiple SR FETs are used in parallel to minimize conduction losses. As multiple FETs are paralleled and driven by a single driver, the gate signals are rising/falling much slower than primary FETs. Then the SR gate falling edge must be earlier than the primary gate falling edge, to ensure that SRs can be turned off earlier than primary FETs. Furthermore, a certain blanking time (about 30 ns) is necessary between the real turn-off of the SRs (the point when V_{GS} falls below the gate threshold voltage) and the real turn-off the primary FETs, to make sure no negative currents flow through SRs. Besides, as an optocoupler is used to isolate the primary PWM signals from the secondary, the isolation delay of the optocoupler must be taken into account when the digital controller generates PWM signals. An ideal timing diagram of the fixed-frequency LLC converter is shown in **Figure 7**.

The use of Infineon's digital controller XDPP1100-Q024 can easily satisfy the above timing requirements in the LLC quarter-brick converter. XDPP1100 is highly flexible in PWM configuration. The rising-edge and falling-edge delay of each PWM can be programmed independently. **Figure 8** shows the PMBus command in the GUI to configure the rising and falling edge of the primary and secondary PWMs. The maximum delay time can be set to 318.75 ns with a resolution of 1.25 ns. The active PMWs are highlighted in color.

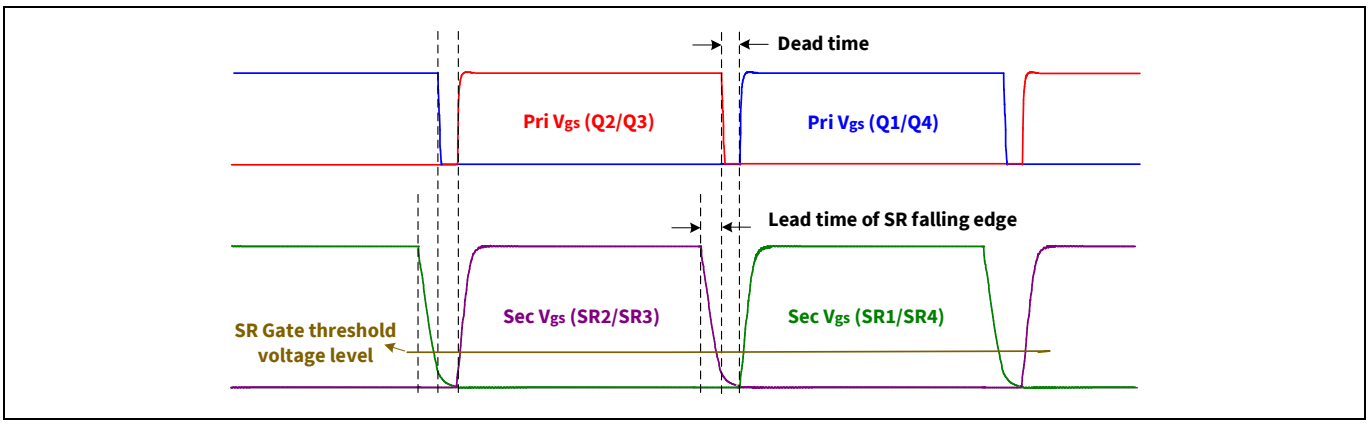


Figure 7 Ideal timing diagram of the fixed-frequency LLC quarter-brick converter

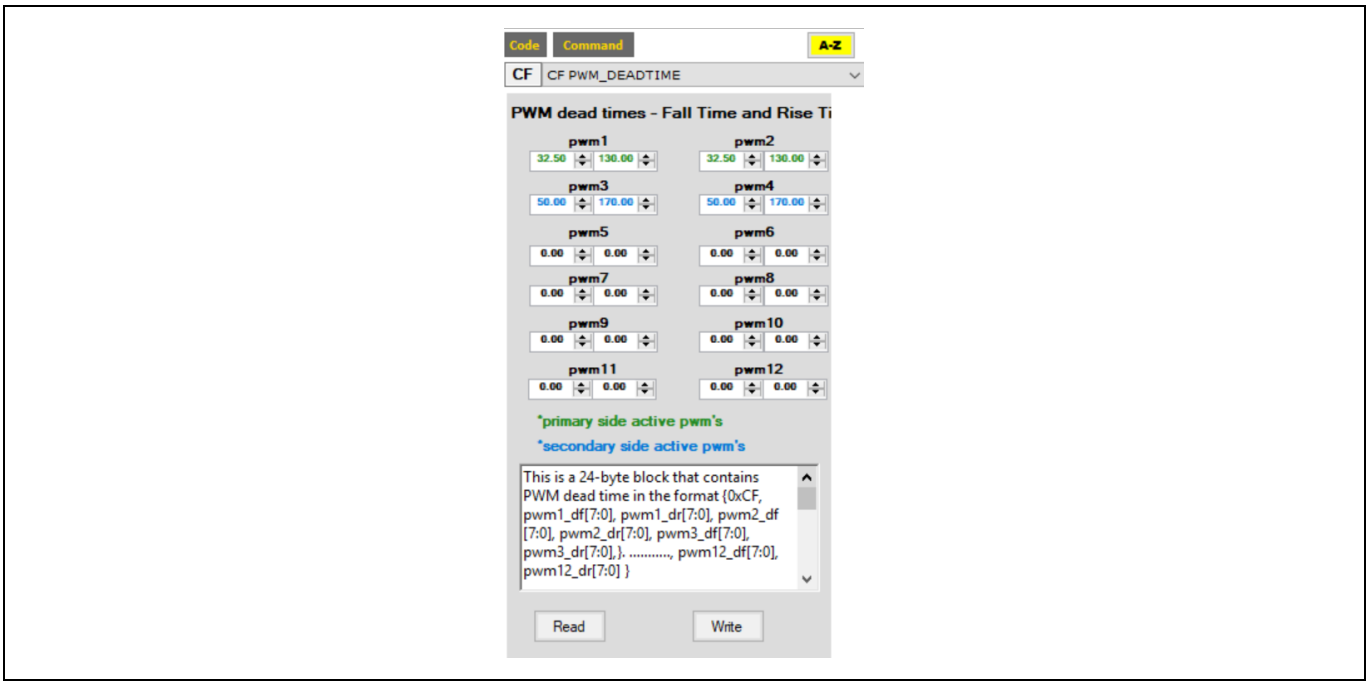


Figure 8 PWM rising-edge and falling-edge configuration in digital controller XDPP1100

1.4 Soft-start

Soft-start is needed to establish the output voltage progressively in order to prevent high current stress. One common method is to start up by sweeping switching frequency from an initial high value down to the resonant point. The maximum switching frequency of the converter is limited by hardware (especially by the driving capability of the bias supply). If the allowed maximum frequency is not high enough (over 3~4 times resonant frequency), a large inrush current can still occur, since the voltage gain is not low enough at the beginning.

Another method for soft-start is to ramp up duty-cycle from 0 to nearly 50 percent (with dead-time) at resonant frequency. The LLC converter operates in PWM mode, and high initial inrush current can be avoided. As resonant inductance is typically small, the converter may still suffer from very high peak current when operating at resonant frequency, especially at start-up under harsh constant-current load conditions. High current stress may also cause large ringings on V_{DS} of the FETs in PWM-mode operation, increasing the voltage stress during start-up.

In this design, a duty-cycle/frequency hybrid soft-start is presented. The duty-cycle ramps up from 0 to nearly 50 percent (with dead-time) at a higher switching frequency (e.g., 500 kHz). Then duty-cycle is fixed at nearly 50 percent, and switching frequency decreases gradually from the high value to the resonant frequency (310 kHz). As the converter operates in PWM mode at a higher switching frequency, the peak current can be greatly reduced. The PWM sequence of the duty-cycle/frequency hybrid soft-start is shown in **Figure 9**.

With the XDPP1100-Q024 digital controller, the duty-cycle/frequency hybrid soft-start can be easily implemented. A customized firmware patch for the start-up procedure has been developed and can be loaded into the one-time programmable (OTP) memory. The start-up parameters, like the maximum switching frequency, duty-cycle ramp time and frequency decrease time, can be configured by the MFR PMBus command, which can be imported into the GUI using the “Load PMBus Spread Sheet” button. The PMBus spreadsheet can be found in the GUI installation folder.

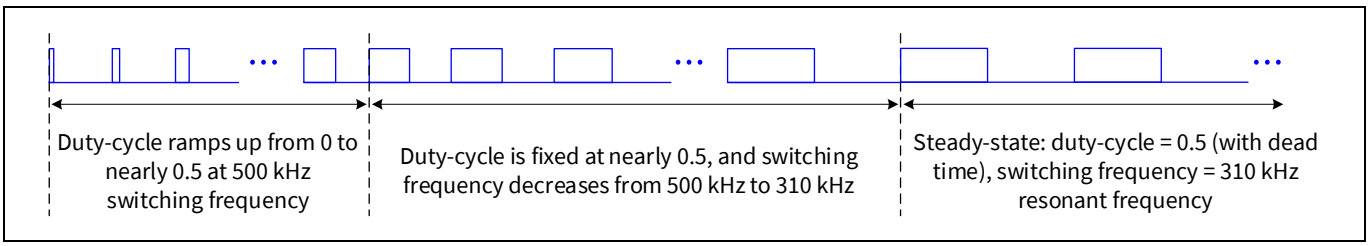


Figure 9 PWM sequence of the duty-cycle/frequency hybrid soft-start

1.5 Fault protections

The XDPP1100-Q024 digital controller has two 11-bit voltage sense ADCs with 50 MHz sampling rate, one 9-bit current sense (CS) ADC with 25 MHz clocking speed, and a 9-bit general-purpose telemetry ADC which consists of four channels and can be configured to digitize voltage, current, impedance and temperature. These dedicated hardware peripherals of XDPP1100-Q024 make it possible to provide enhanced protections for the LLC quarter-brick converter.

The XDPP1100-Q024 controller is located on the secondary side and senses the input voltage, the output voltage and the output current, as can be seen in **Figure 2**. The output voltage is sensed directly by resistor-dividers. The input voltage is sensed from the transformer secondary side at the switching node V_{rect} and computed based on resistor-divider ratio and transformer turns ratio. This eliminates the use of an isolated op-amp or other types of isolator for input voltage sensing. The output current is sensed through a PCB copper shunt with amplifier. The temperature of the PCB copper shunt is also sensed by a NTC thermistor and used for CS temperature compensation. The temperature compensation is to eliminate the copper resistance drift overtemperature to enable accurate output current telemetry across the full temperature range.

Introduction and design considerations

Three levels of OCP are configured in the LLC quarter-brick converter. The first-level OCP is provided by IOUT_OC_FAULT, which is based on the averaged output current after a low-pass filter. It has the slowest response, and the fault threshold IOUT_OC_FAULT_LIMIT should be set lowest. The second-level OCP is provided by IOUT_OC_FAST_FAULT. It is based on the averaged output current but without filter. It has a faster response and the fault threshold IOUT_OC_FAST_FAULT_LIMIT should be set higher than IOUT_OC_FAULT_LIMIT. The third-level OCP is provided by the registers for SCP. SCP fault trips when the sensed output current goes above the SCP threshold (isp0_scp_thresh) for a single ADC sample. It has the fastest response, and the SCP threshold should be set the highest.

Besides the three-level OCP, the LLC quarter-brick converter also has output OVP/UVP and input OVP/UVP. The XDPP1100 fault detection is implemented in hardware (HW) and the fault response is managed by firmware (FW). The combination of HW and FW provides fast protection with flexible fault response. Further details about the configuration and additional functionalities of fault protections can be found in the **XDPP1100 application note**.[5]

2 Power board information

2.1 Specification

The specification of the 1 kW fixed-frequency LLC quarter-brick converter is shown in **Table 1**.

Table 1 Specification

Parameter	Min.	Typ.	Max.	Unit
Input voltage range (V_{in})	42	48	60	V DC
V_{in} turn-on threshold	34			V
V_{in} turn-off threshold	32			V
Input current (at 100 percent load)		20		A
Output voltage range (V_{out})	10	12	15	V DC
Output current (I_{out})		80		A DC
Output power		960	1200	W
Output voltage ripple (peak-to-peak at full load, measured with 1800 µF tantalum capacitor)			300	mV p-p
Dynamic load response (50 percent to 100 percent load-transient at 1 A/µs slew rate, measured with 1800 µF tantalum capacitor) - Output voltage deviation - Settling time			 680 200	 mV p-p µs
Recommended output capacitor	1000		10000	µF
Efficiency (V_{in} = 48 V DC) at 25°C: - 25 percent load - 50 percent load - 75 percent load - 100 percent load		 97.0 97.3 96.9 96.2		 %
Switching frequency		310		kHz
Air flow		600		LFM
Operating temperature (ambient)	-40		50	°C

2.2 Schematic

Figure 10 and **Figure 11** show the schematics of the power stage and control circuit of the 1 kW fixed-frequency LLC quarter-brick converter. Two OptiMOS™ 6 80 V MOSFETs ISC033N08NM6 with 3.3 mΩ are used in parallel in the primary full-bridge and driven by a single 2EDL8124G driver at each branch. Four OptiMOS™ 5 25 V MOSFETs IQE006NE2LM5 with 0.65 mΩ are used in parallel in the secondary full-bridge and driven by a single 2EDL8124G driver at each branch.

The XDPP1100-Q024 digital controller is used for PWM generation and soft-start implementation as well as telemetry and protection. Voltage ADC VSEN/VREF is used for output voltage sense. The other voltage ADC VRSEN/VRREF is used for input voltage sense through the transformer secondary winding. A high-speed current ADC ISEN/IREF is used for output CS. TSEN is used for temperature sense of the PCB copper shunt for CS temperature compensation.

Power board information

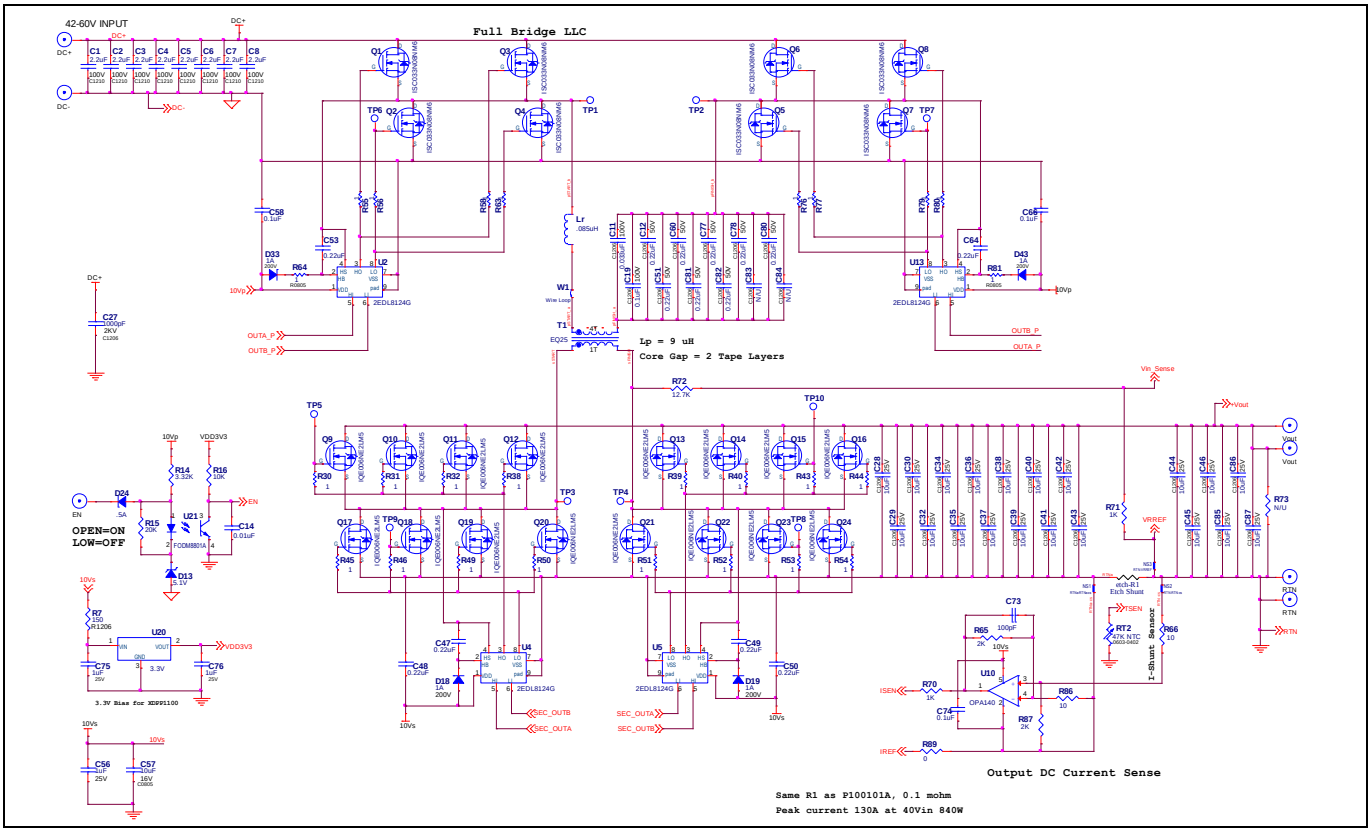


Figure 10 Power stage schematic

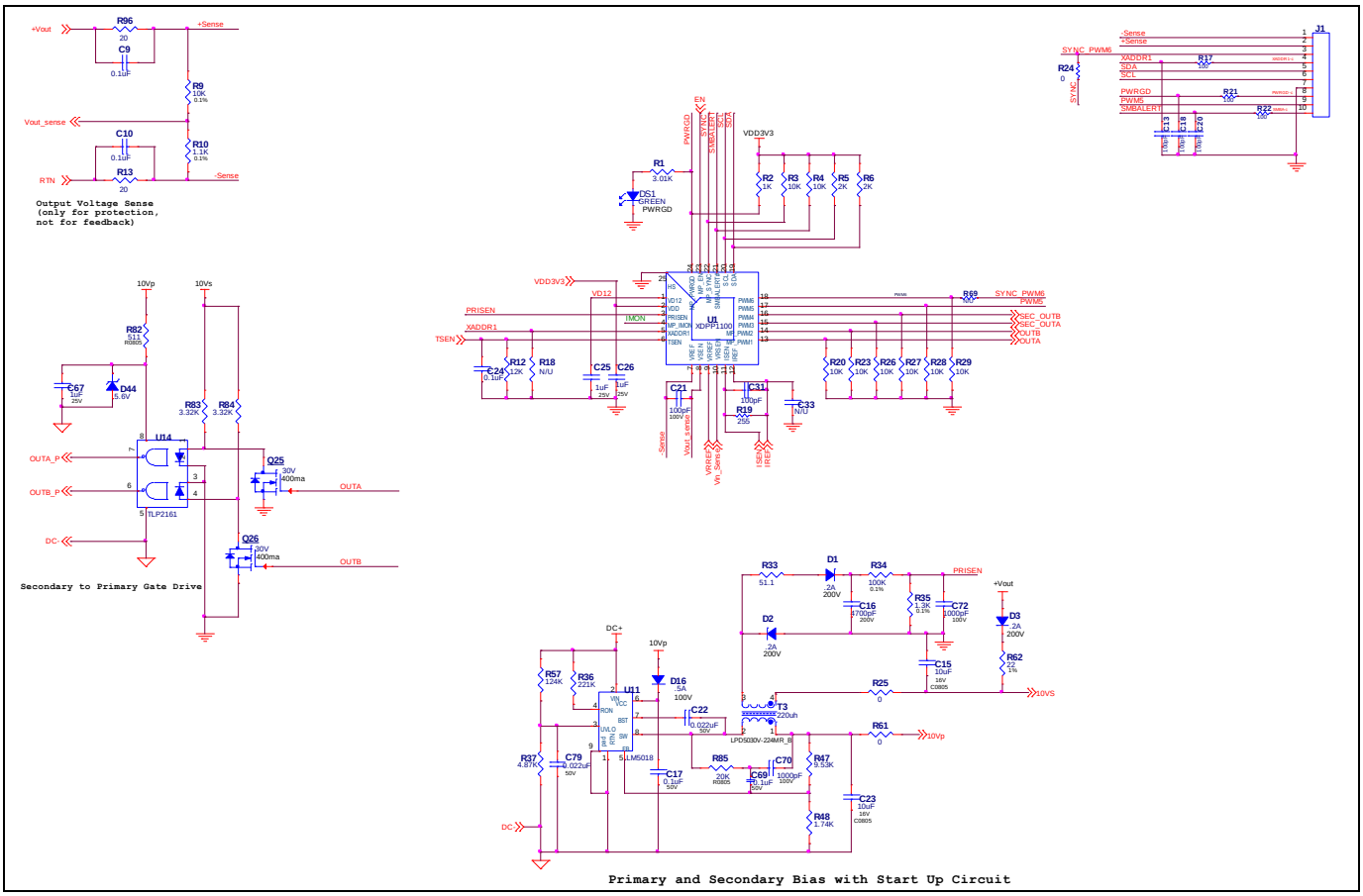


Figure 11 Control and bias circuit schematic

Power board information

Figure 12 and **Figure 13** give the top and bottom-side PCB reference drawings showing part locations for each component. Measurement test points are also highlighted in the reference drawings.

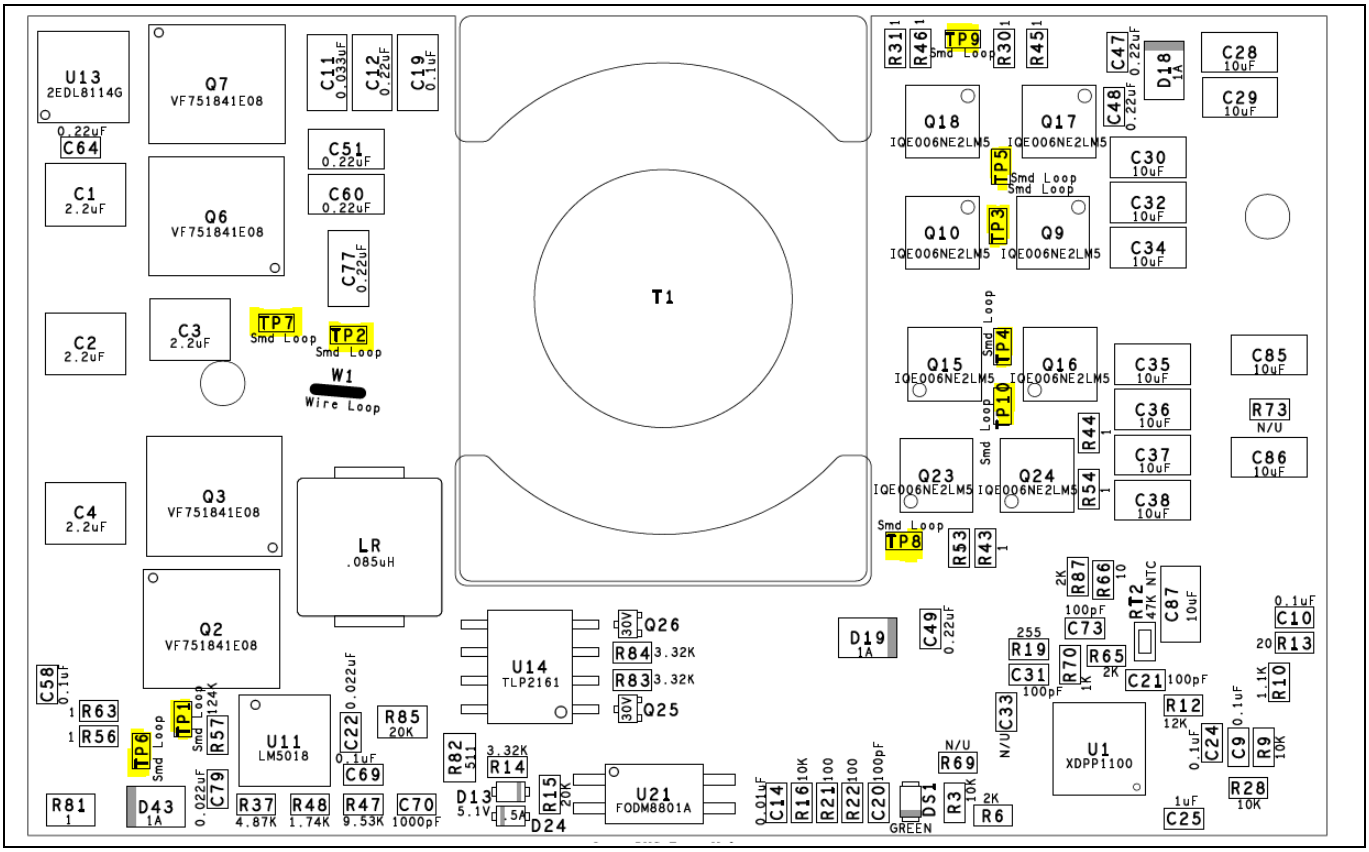


Figure 12 Assembly reference – top side of PCB

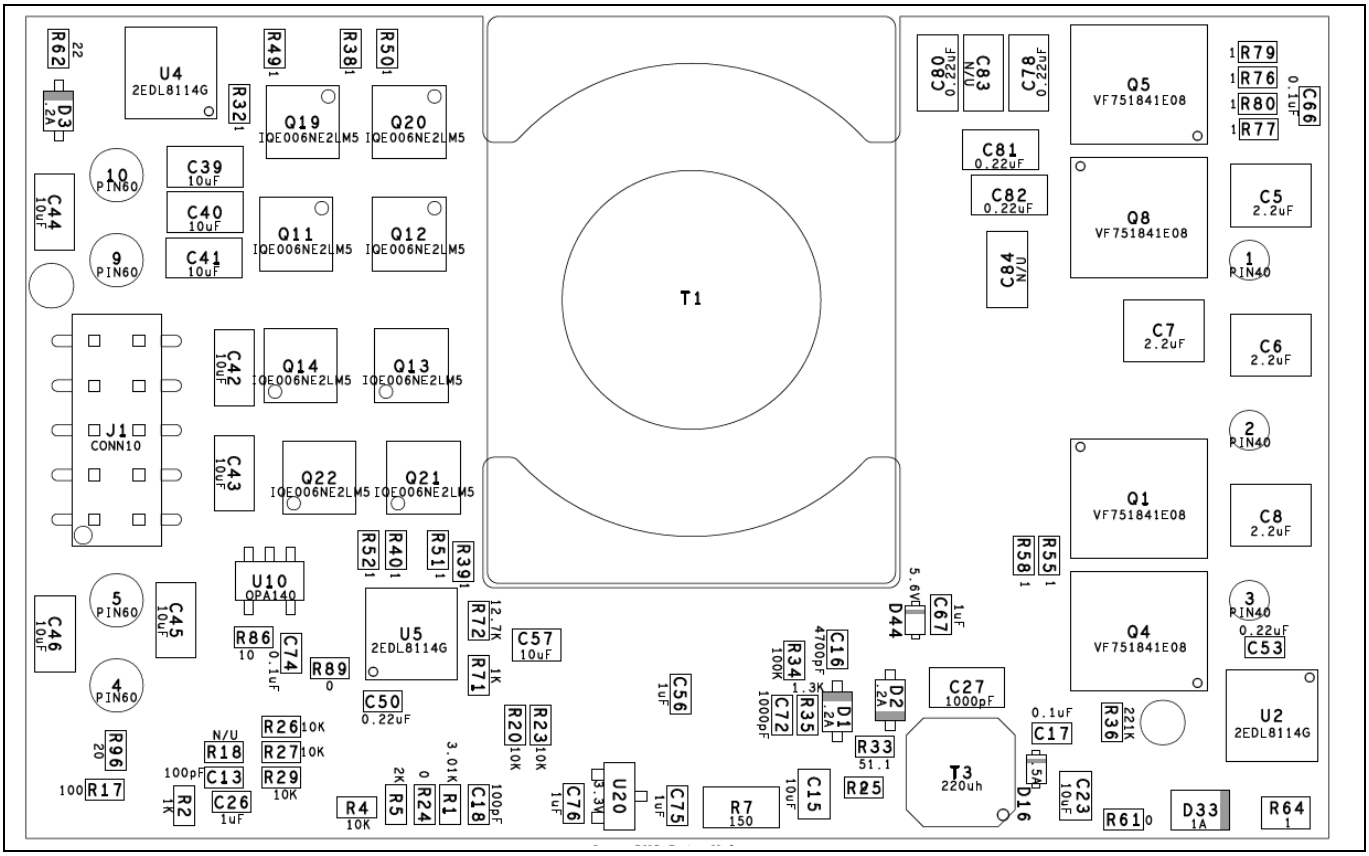


Figure 13 Assembly reference – bottom side of PCB

2.3 Transformer

The transformer has a conversion ratio of four primary turns to one secondary turn with a planar construction. The core geometry is an EQ25 + plate with ferrite material 3F36 from the manufacturer Ferroxcube. The primary winding is composed of four PCB layers in series while the secondary winding is composed of ten PCB layers in parallel. The primary windings have been interleaved with the secondary windings for minimum leakage inductance and proximity losses. A detailed description of the construction can be seen in **Figure 14**.

In this design, a magnetizing inductance of 9 µH is needed for ZVS. Two layers of TestEquity TST22-0250 polyimide film tape (5 mil gap in total) have been added between the EQ25 core and the plate in order to obtain the required inductance.

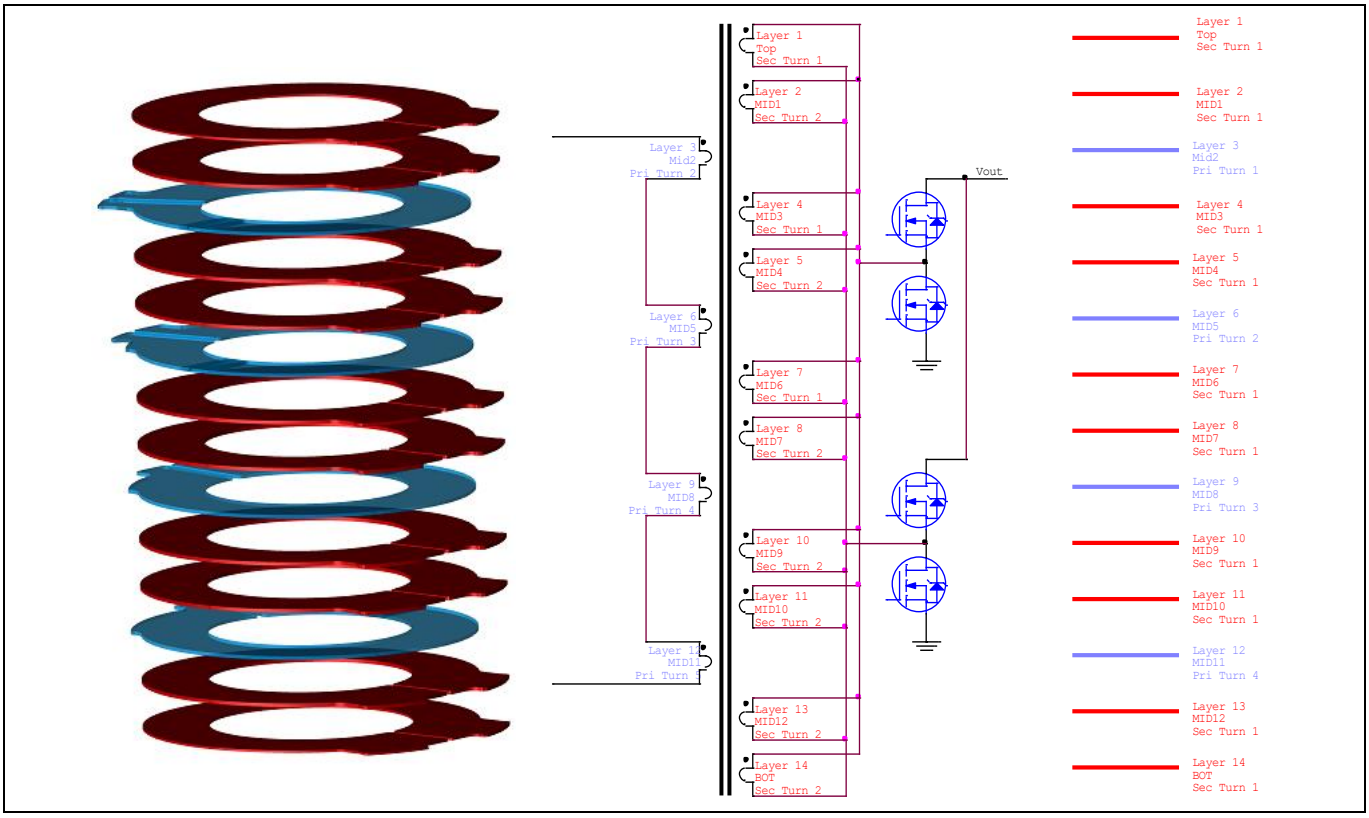
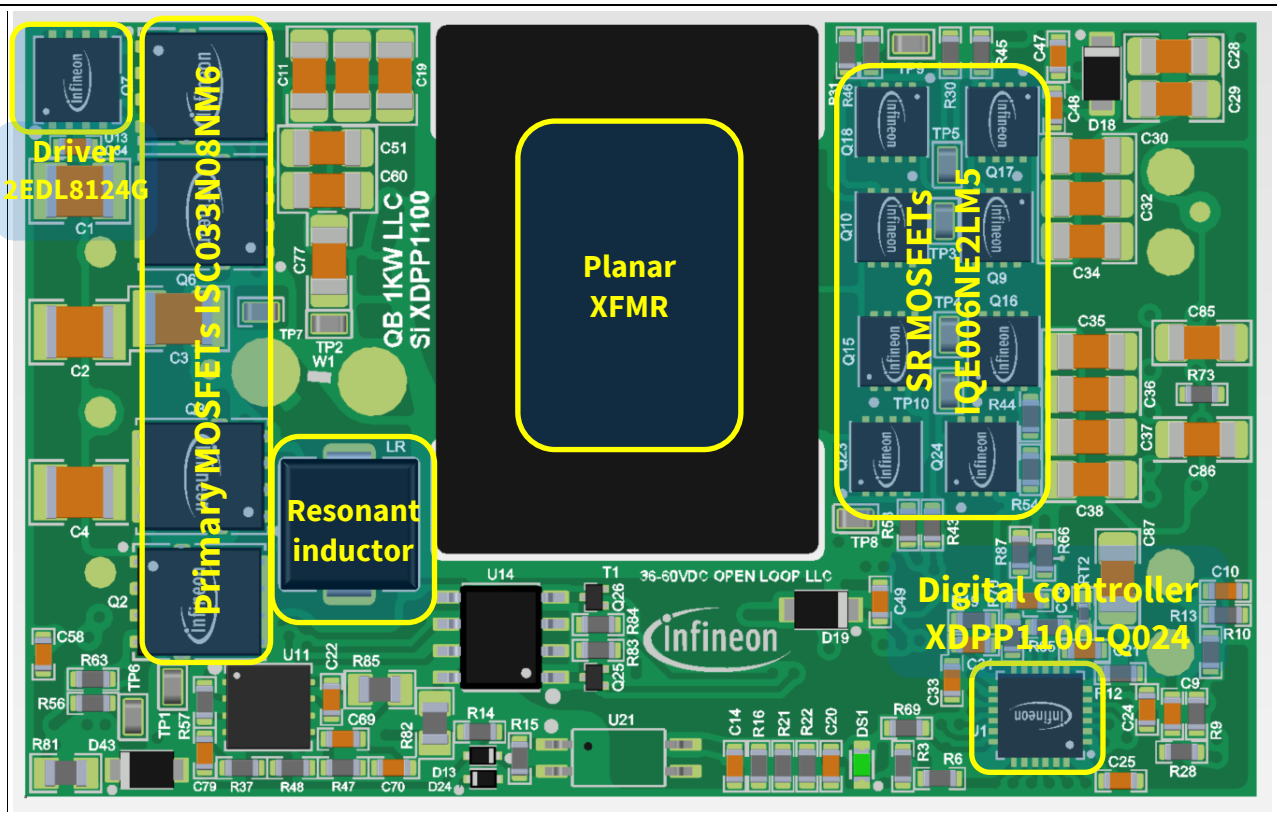


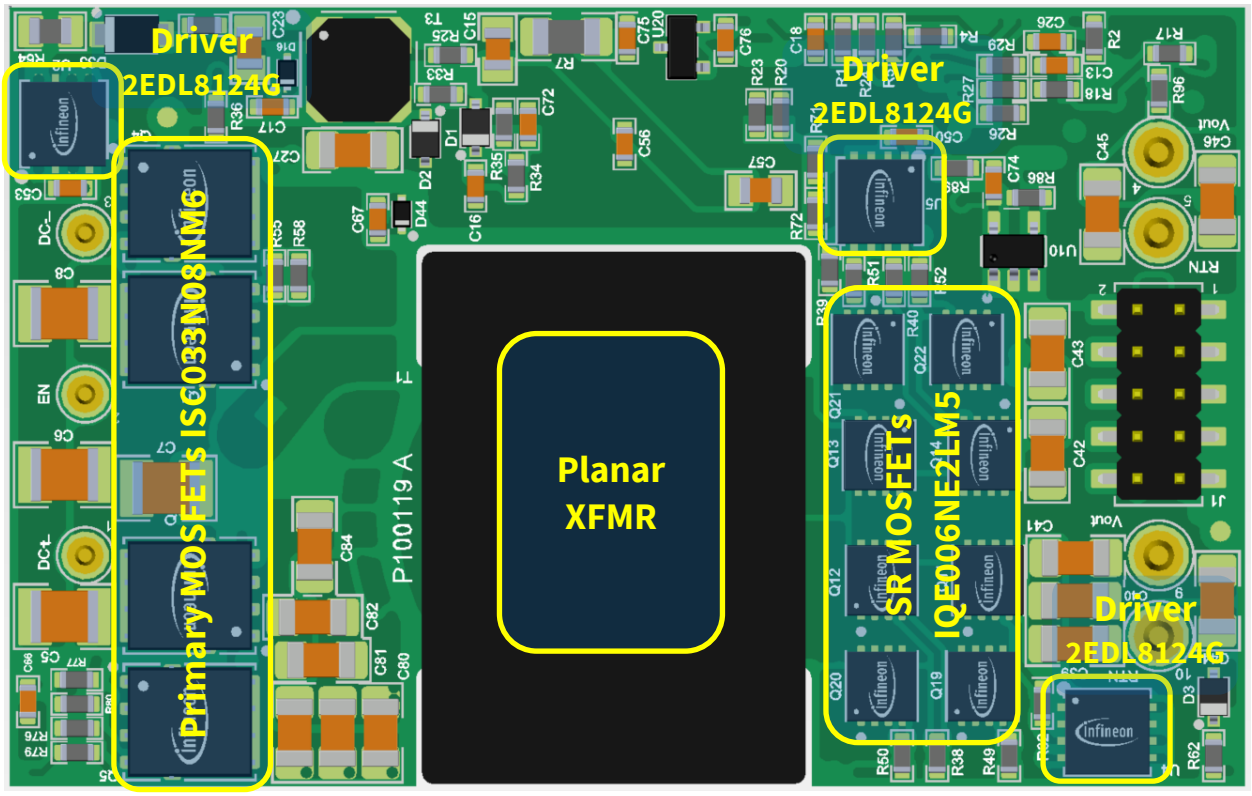
Figure 14 Planar transformer construction

2.4 Board layout

Figure 15 shows the placement of the component locations on the 1 kW fixed-frequency LLC quarter-brick converter. The outer dimensions of the board, designed without enclosure, are 2.30" x 1.45" x 0.51" (58.4 mm x 36.8 mm x 12.9 mm), which results in a power density in the range of 564 W/in^3 (34.6 W/cm^3). The PCB is fabricated from a 14-layer board. The internal layers are all 6 oz. copper, 8.23 mil (0.209 mm) thickness with the top and bottom layers at 4 oz. copper, 5.5 mil (0.140 mm) thickness. The mechanical outline and bill of materials (BOM) of the LLC quarter-brick converter can be found in the Appendix.



Top



Bottom

Figure 15 Placement of the different sections

2.5 Power loss analysis

The major sources of power losses are identified and calculated as in **Table 2**. At V_{in}=48 V and I_{out}=80 A, the estimated total power loss is 30.84 W, which is close to the measured power loss of 36.8 W. The loss breakdown chart is shown in **Figure 16**.

Table 2 Loss breakdown at V_{in}=48 V and I_{out}=80 A

Primary MOSFETs	Conduction loss	2.70 W	3.82 W
	Body diode loss	0.29 W	
	Driving loss	0.83 W	
Secondary MOSFETs	Conduction loss	4.48 W	8.21 W
	Body diode loss	0.70 W	
	Driving loss	3.03 W	
Transformer	Conduction loss	7.40 W	8.77 W
	Core loss	1.37 W	
Resonant inductor	Conduction loss	0.13 W	1.23 W
	Core loss	1.10 W	
Resonant capacitor	-	-	0.17 W
Output capacitor	-	-	0.23 W
Auxiliary bias circuit	-	-	1.06 W
High current PCB traces and vias	-	-	7.35 W
Total losses	-	-	**30.84 W**

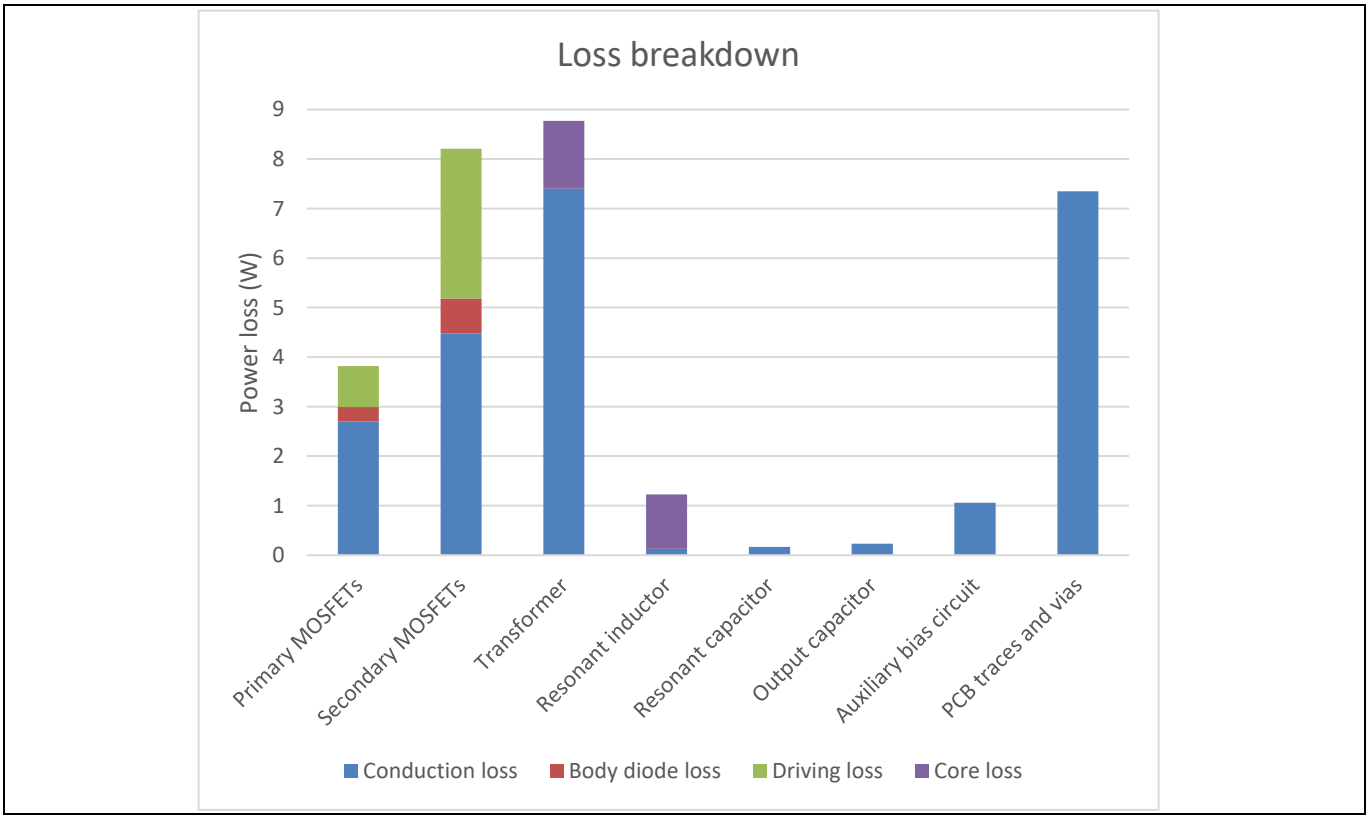


Figure 16 Power loss breakdown

2.6 Cooling solution and test setup

The quarter-brick test fixture is a test platform for the quarter-brick converter. It provides power connection terminals, communication and debugging ports, as well as a cooling fan. **Figure 17** shows the schematic of the test fixture. It has an I²C connector for I²C and PMBus communication, and a SWD debugger port for FW debugging. The fan should be biased with external DC power supply, in the 5 V to 12 V range for different air flow. This bias is necessary to enable communication with the XDPP1100 to the USB dongle.

The switch SW1 at the primary is the enable switch to turn-on the quarter-brick. Please ensure that the polarity of the enable switch can be configured by PMBus command ON_OFF_CONFIG. If EN “active low” is preferred, the user should write PMBus command ON_OFF_CONFIG and choose the polarity to be “active low”. When “active low” is selected, the on/off label on the test fixture aligns with the actual on/off status. If “active high” is selected, the on/off label shows the opposite status.

A 3.3 V LDO regulator on the test fixture provides pull-up voltage to the SDA/SCL I²C communication bus when 5 V to 12 V is applied to the external bias connector.

Test setup for the 1 kW fixed-frequency LLC quarter-brick converter using the test fixture is shown in **Figure 18**.

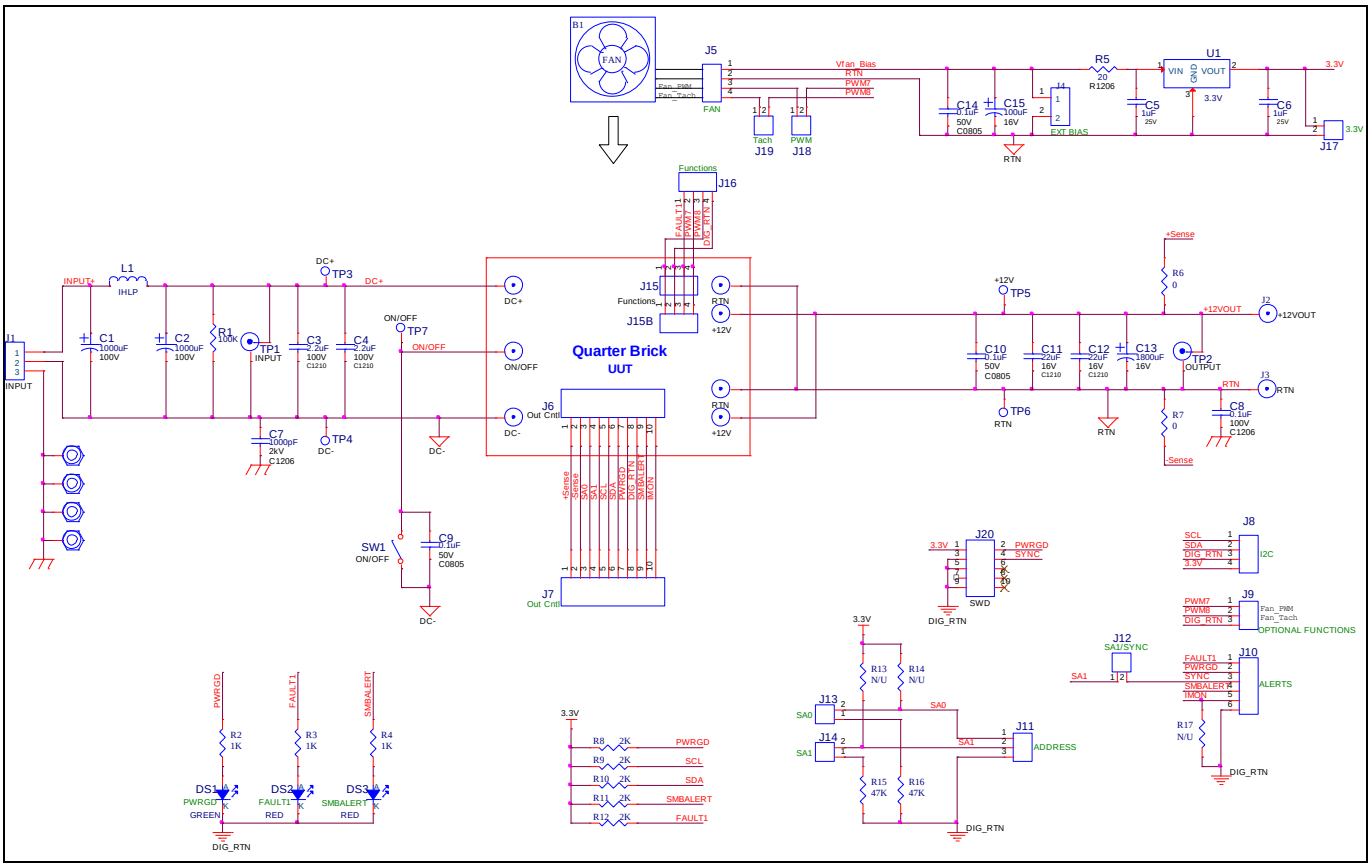


Figure 17 Test fixture schematic

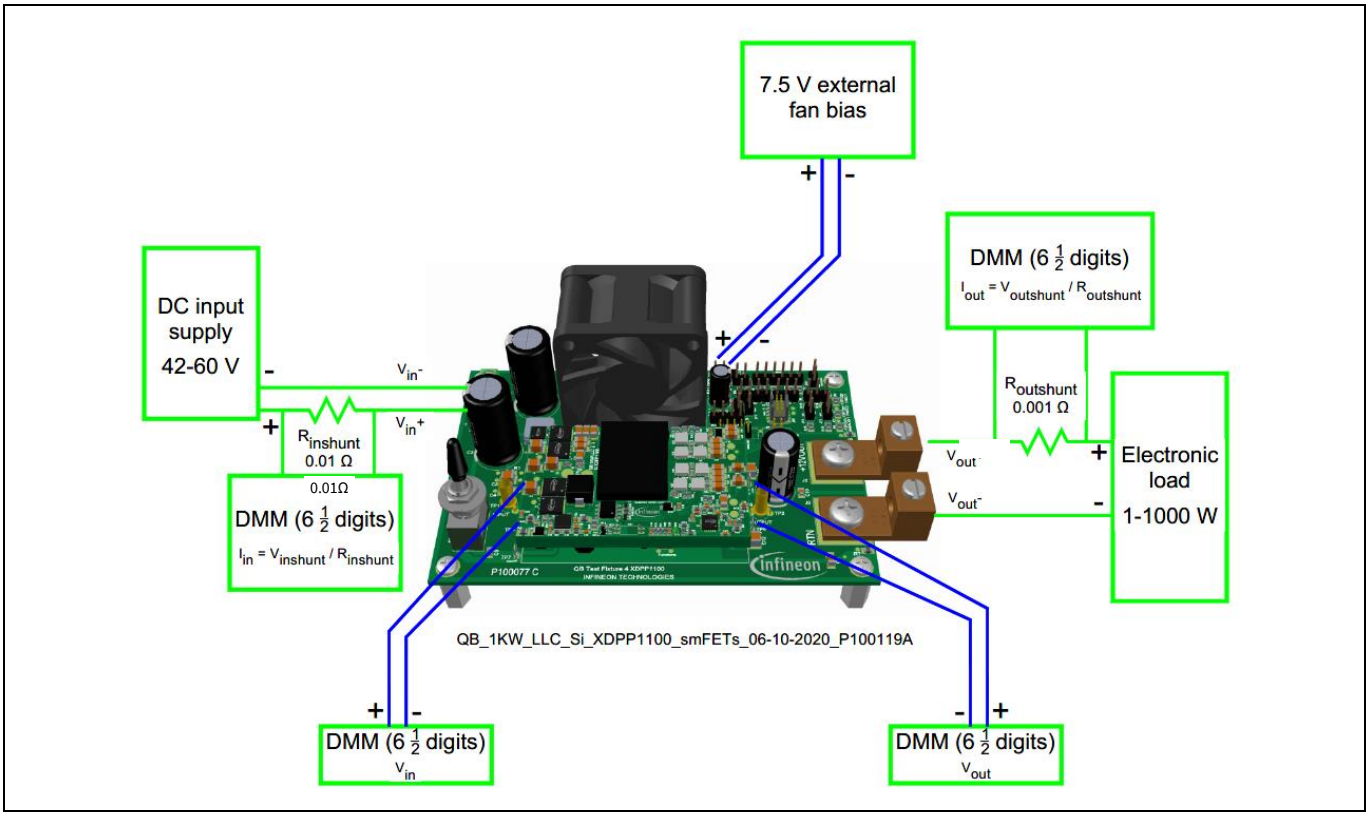


Figure 18 Test setup with test fixture

Necessary connections to operate the board:

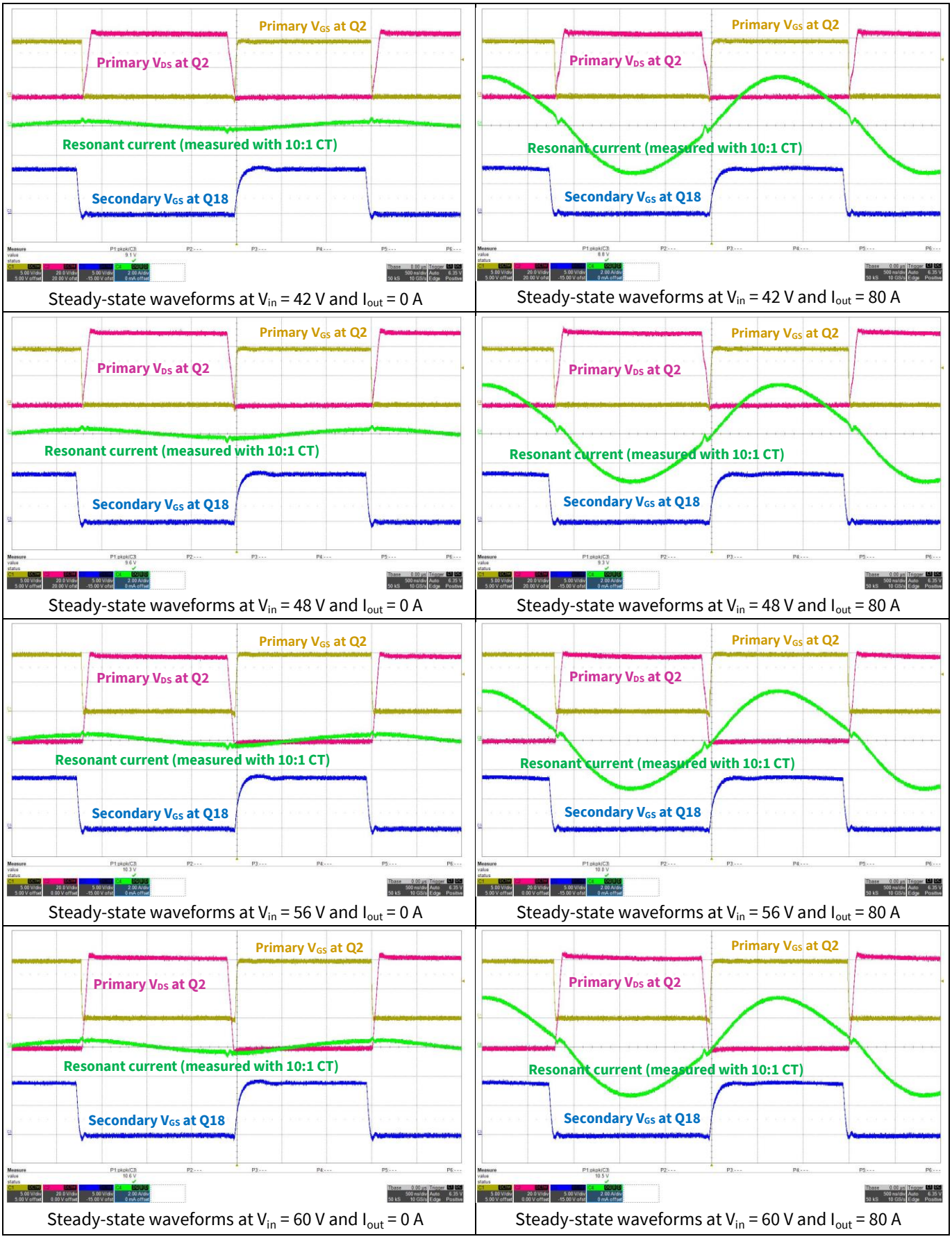
- Connect the quarter-brick to the test fixture. Make sure the DC input, 12 V output and signal connector J6 on the test fixture have good contact.
- Connect the 48 V input power supply to J1.
- Connect the load to J2 and J3.
- Bias fan with 5~12 V DC power supply at J4 (EXT BIAS).
- Connect the XDPP1100 USB dongle (USB007 revA) to J8. Find the direction by identifying the ground pin G (black wire). The blue wire of USB007 is not used and can be left floating.
- Make sure the switch SW1 is in the off position.
- Turn-on the 48 V input power supply. A minimum of 35 V is required to enable the auxiliary power supply.
- Measure the secondary 10 VS. It should have 10 V ±1 V output.
- This demo board comes with a default patch and configuration stored in OTPand can be turned on once the operation command is asserted from the XDPP1100 GUI.
- In order to assert the operation command, open XDPP1100 GUI and click on “Auto populate”. The auto populate option is in the top-left corner just below the “file” option.
- Write “ON” to PMBus command 0x01 OPERATION, and turn SW1 to the on position (sequence is not critical).

3 Experimental results

3.1 Steady-state waveforms

Figure 19 shows the key steady-state waveforms taken on the 1 kW FF LLC quarter-brick converter mounted to the Infineon test fixture. The waveforms were taken over the line and load range. As can be seen, ZVS is achieved over the whole line and load range.

Experimental results



Steady-state waveforms at V_{in} = 42 V and I_{out} = 0 A

Steady-state waveforms at V_{in} = 42 V and I_{out} = 80 A

Steady-state waveforms at V_{in} = 48 V and I_{out} = 0 A

Steady-state waveforms at V_{in} = 48 V and I_{out} = 80 A

Steady-state waveforms at V_{in} = 56 V and I_{out} = 0 A

Steady-state waveforms at V_{in} = 56 V and I_{out} = 80 A

Steady-state waveforms at V_{in} = 60 V and I_{out} = 0 A

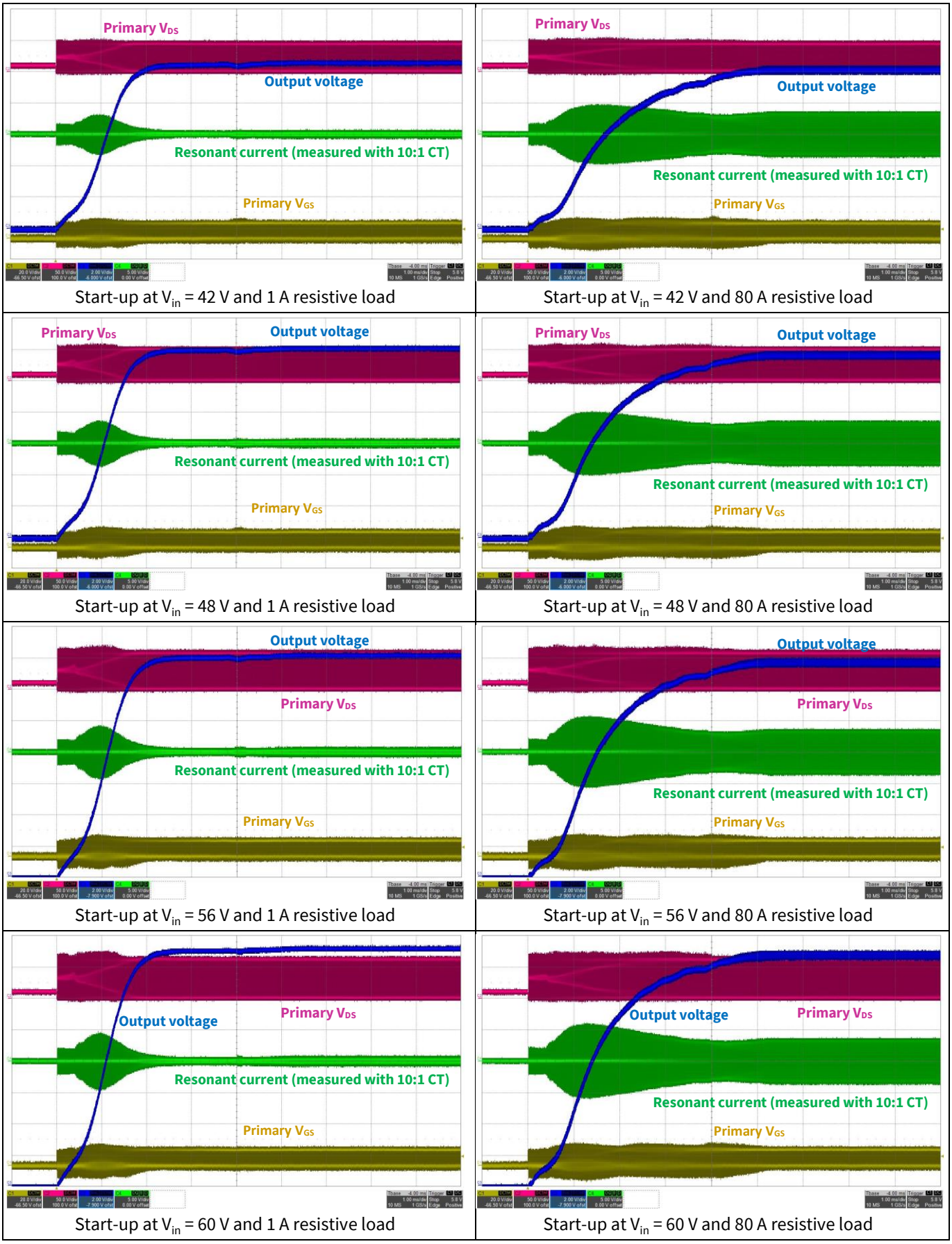
Steady-state waveforms at V_{in} = 60 V and I_{out} = 80 A

Figure 19 Steady-state waveforms

3.2 Start-up waveforms

The duty-cycle/frequency hybrid soft-start over the line and load range has been tested. **Figure 20** shows the soft-start waveforms taken under resistive load. **Figure 21** shows the soft-start waveforms taken under constant-current load.

Experimental results



Start-up at V_{in} = 42 V and 1 A resistive load

Start-up at V_{in} = 42 V and 80 A resistive load

Start-up at V_{in} = 48 V and 1 A resistive load

Start-up at V_{in} = 48 V and 80 A resistive load

Start-up at V_{in} = 56 V and 1 A resistive load

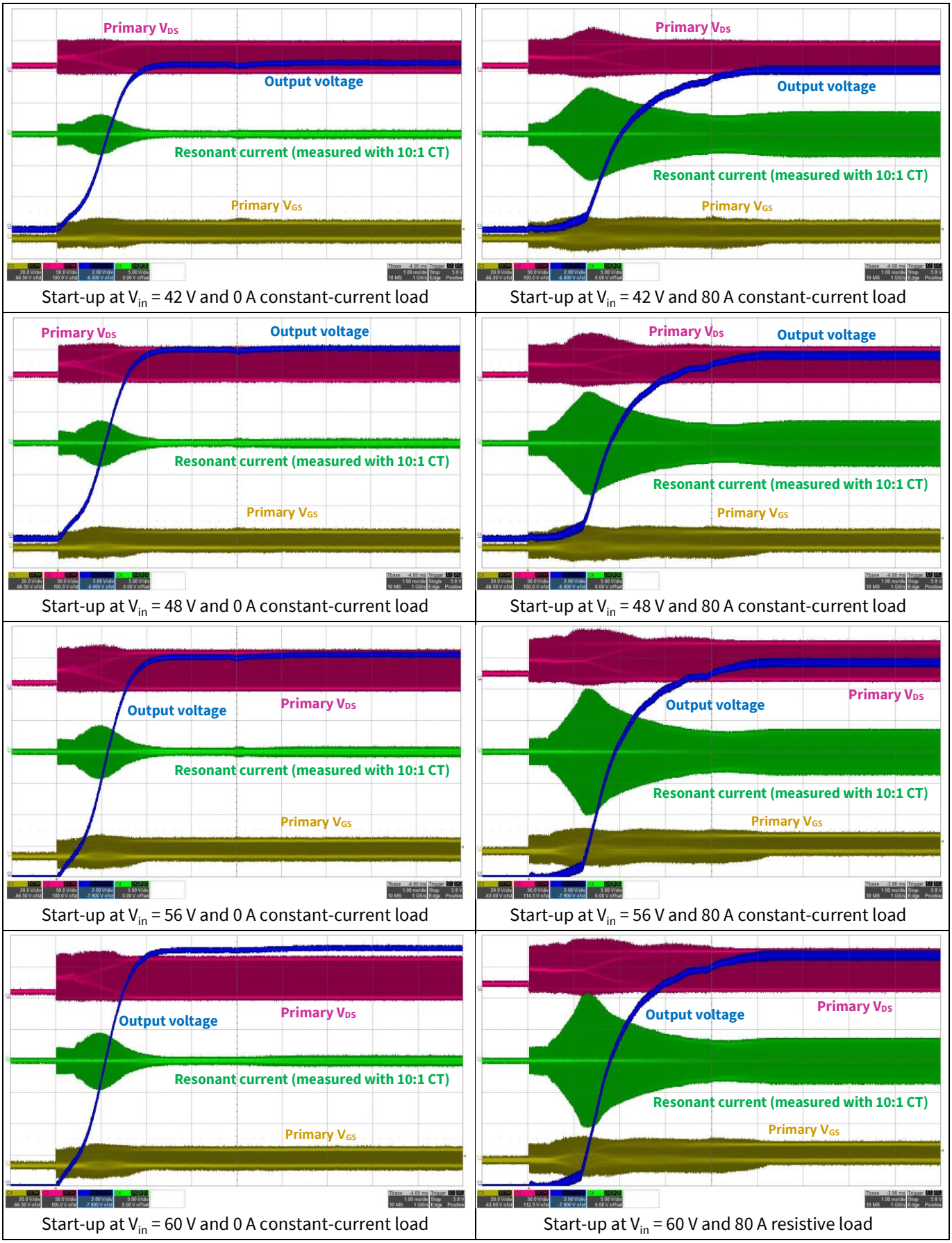
Start-up at V_{in} = 56 V and 80 A resistive load

Start-up at V_{in} = 60 V and 1 A resistive load

Start-up at V_{in} = 60 V and 80 A resistive load

Figure 20 Start-up waveforms under resistive load

Experimental results



Start-up at V_{in} = 42 V and 0 A constant-current load

Start-up at V_{in} = 42 V and 80 A constant-current load

Start-up at V_{in} = 48 V and 0 A constant-current load

Start-up at V_{in} = 48 V and 80 A constant-current load

Start-up at V_{in} = 56 V and 0 A constant-current load

Start-up at V_{in} = 56 V and 80 A constant-current load

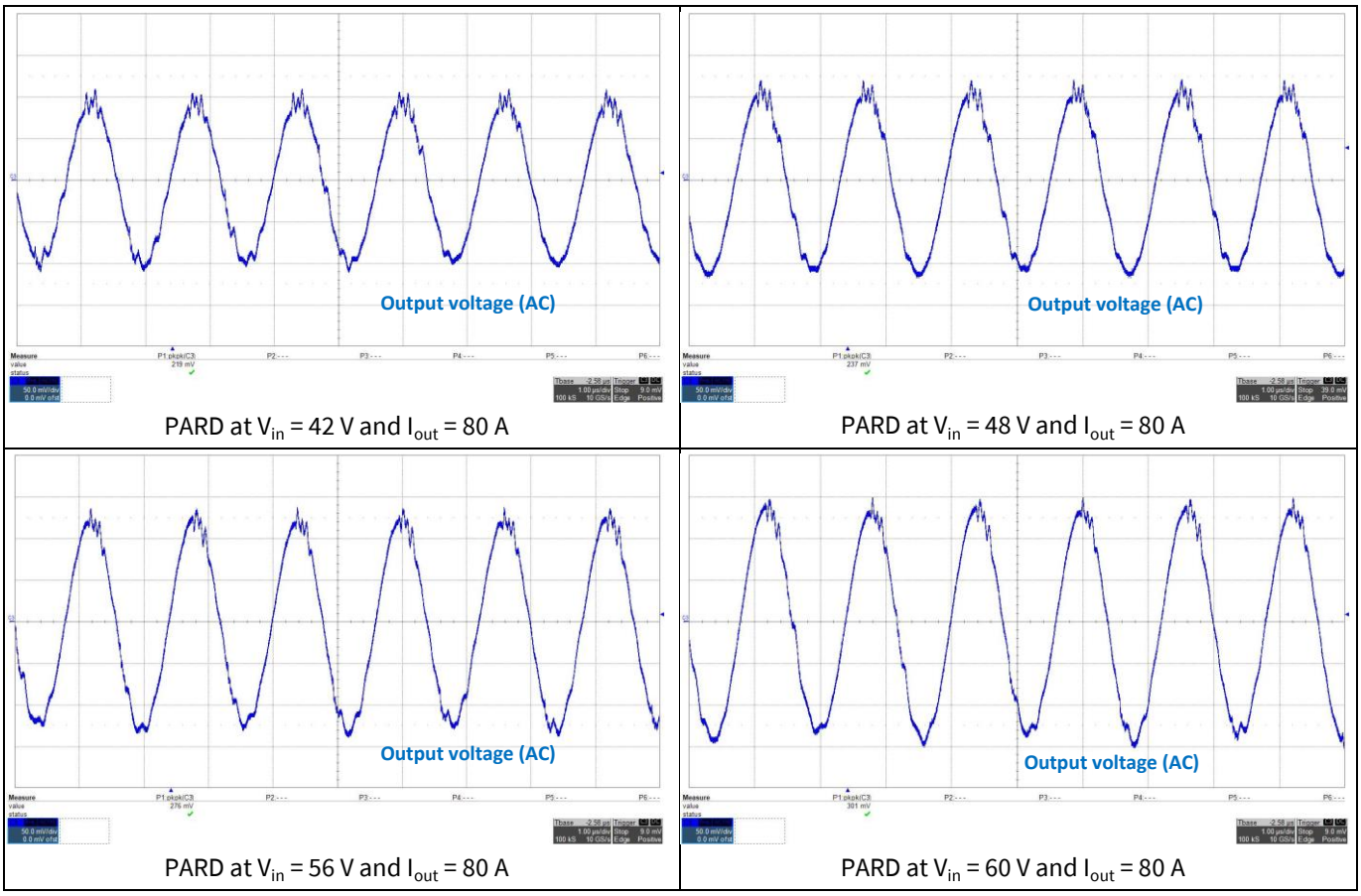
Start-up at V_{in} = 60 V and 0 A constant-current load

Start-up at V_{in} = 60 V and 80 A resistive load

Figure 21 Start-up waveforms under constant-current load

3.3 Output PARD

Figure 22 shows the output periodic and random deviation (PARD) over the line and load range. The typical output PARD (peak-to-peak) is 240 mV at V_{in} = 48 V full load.



PARD at V_{in} = 42 V and I_{out} = 80 A

PARD at V_{in} = 48 V and I_{out} = 80 A

PARD at V_{in} = 56 V and I_{out} = 80 A

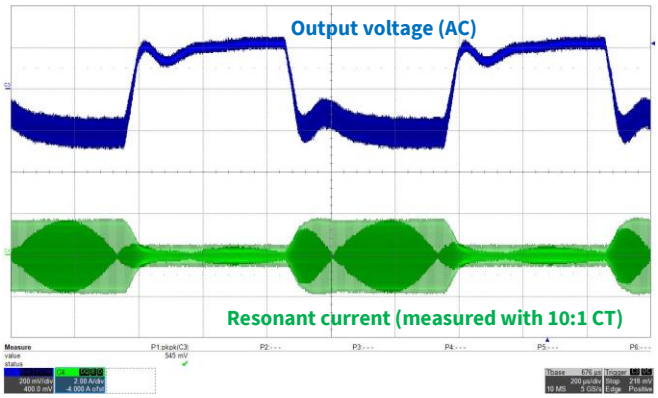
PARD at V_{in} = 60 V and I_{out} = 80 A

Figure 22 Output PARD waveforms

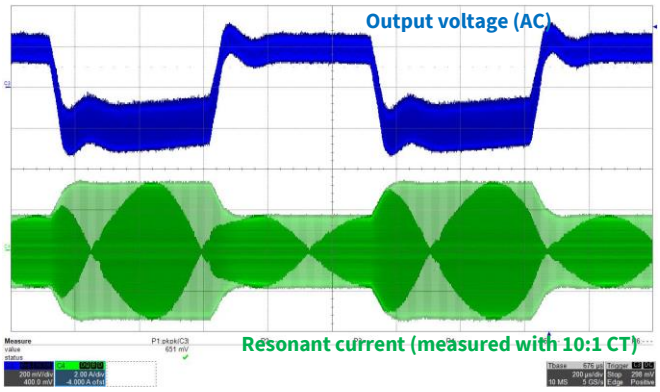
3.4 Load-transient response

Figure 23 shows the output load-transient waveforms over the line and load range. Note that the converter is unregulated. The maximum output voltage deviation is 680 mV (transition from 50 percent load to 100 percent load at 1 A/µs slew rate).

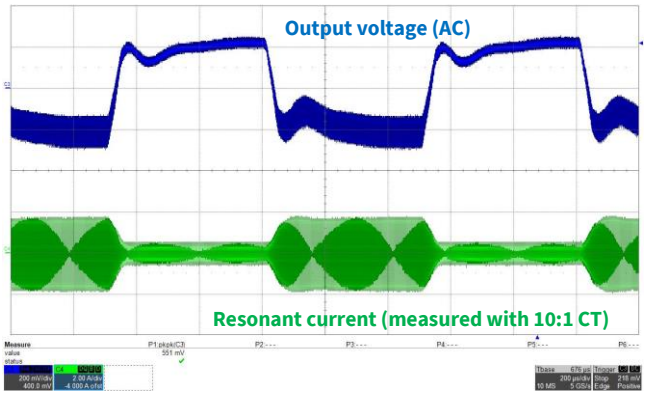
Experimental results



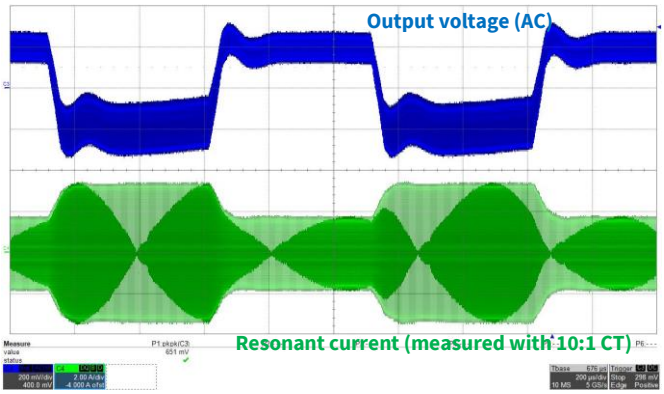
Transient at V_{in} = 42 V from no load to 50 percent load at 1 A/µs



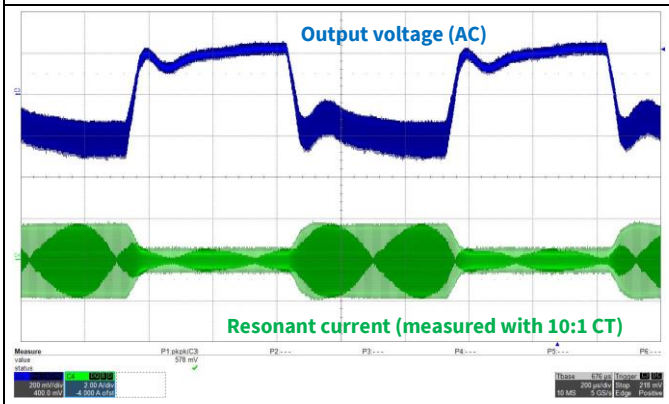
Transient at V_{in} = 42 V from 50 percent load to 100 percent load at 1 A/µs



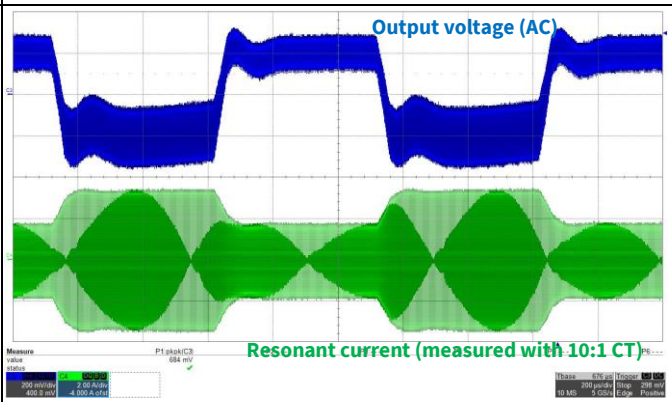
Transient at V_{in} = 48 V from no load to 50 percent load at 1 A/µs



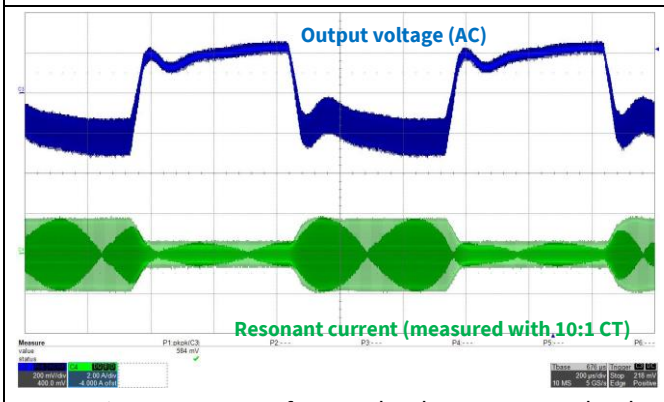
Transient at V_{in} = 48 V from 50 percent load to 100 percent load at 1 A/µs



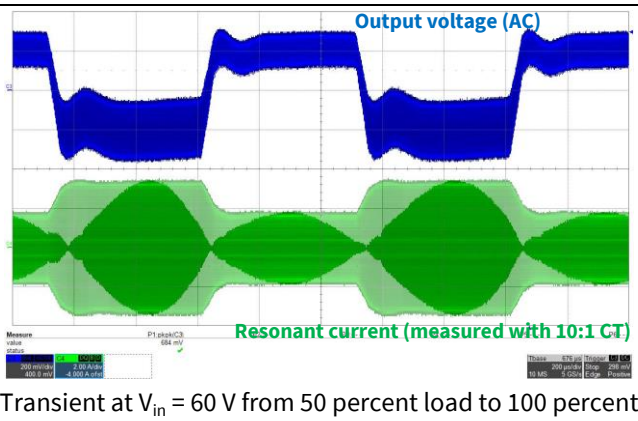
Transient at V_{in} = 56 V from no load to 50 percent load at 1 A/µs



Transient at V_{in} = 56 V from 50 percent load to 100 percent load at 1 A/µs



Transient at V_{in} = 60 V from no load to 50 percent load at 1 A/µs

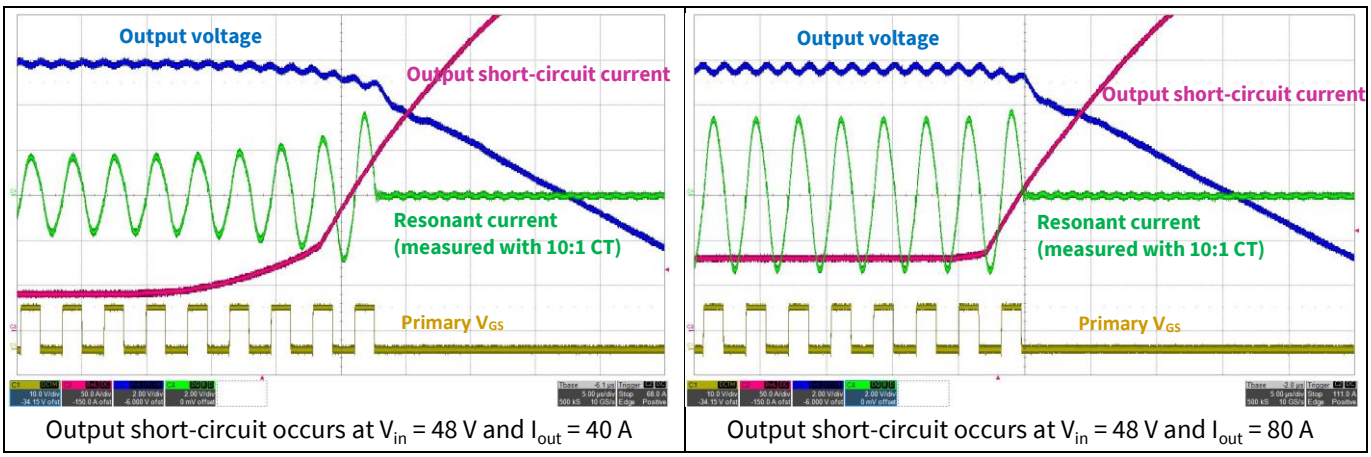


Transient at V_{in} = 60 V from 50 percent load to 100 percent load at 1 A/µs

Figure 23 Load-transient waveforms

3.5 Output SCP

The output is shorted using a DC breaker in the test. **Figure 24** shows the output SCP. The converter is protected by shutting off the PWMs when the secondary current through PCB copper shunt goes over the SCP threshold. In the test, the SCP threshold is 90 A. The corresponding peak resonant current is about 37 A at the SCP threshold. Note, the output short-circuit current (the red waveform) is mostly provided by the large output capacitor on the fixture.



Output short-circuit occurs at V_{in} = 48 V and I_{out} = 40 A

Output short-circuit occurs at V_{in} = 48 V and I_{out} = 80 A

Figure 24 Output SCP

3.6 Efficiency

Table 3 show the efficiency over the line and load range. The efficiency is measured under 600 FPM air flow. The efficiency curves are given in **Figure 25**. The output voltage range across the load and applied input voltage are provided in **Figure 26**.

Table 3 Measured efficiency (%)

Output current	V_{in} = 42 V	V_{in} = 48 V	V_{in} = 56 V	V_{in} = 60 V
10 A	95.06	95.05	94.69	94.29
20 A	96.89	96.96	96.85	96.64
30 A	97.20	97.35	97.33	97.22
40 A	97.15	97.33	97.41	97.36
50 A	96.93	97.16	97.31	97.30
60 A	96.62	96.90	97.13	97.14
70 A	96.23	96.56	96.86	96.89
80 A	95.77	96.20	96.53	96.64

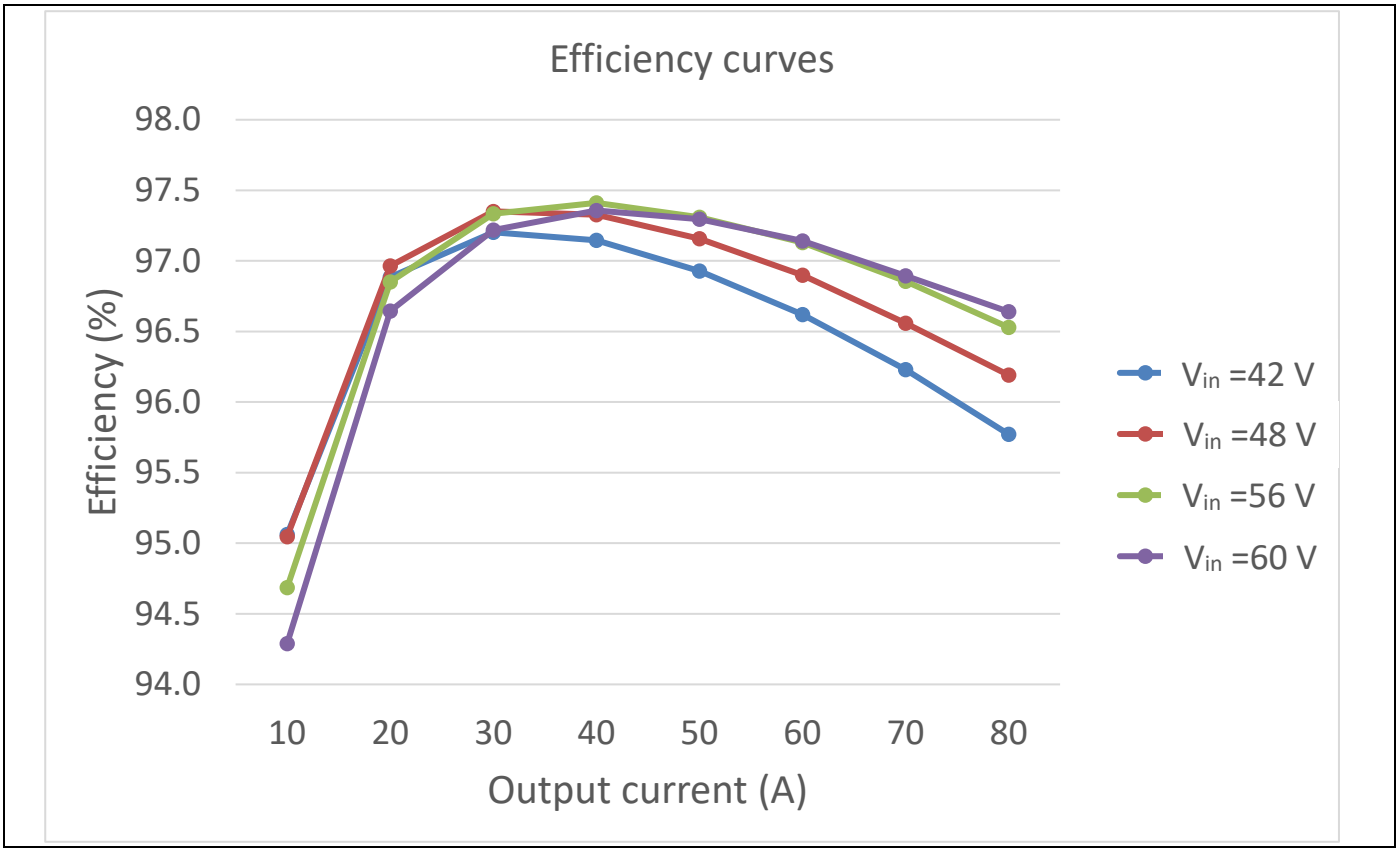


Figure 25 Efficiency graph over line and load range

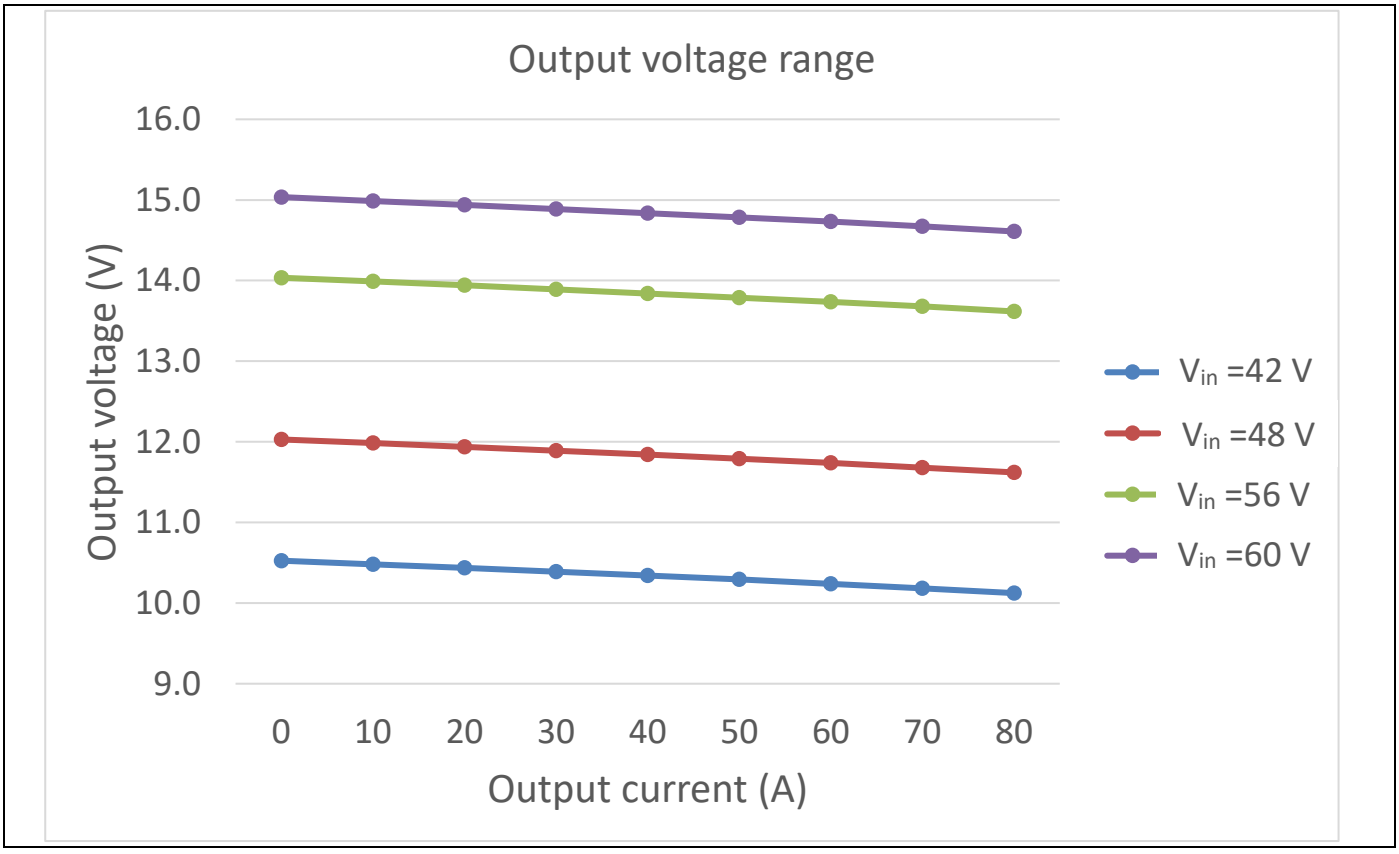


Figure 26 Output voltage across the load and input voltage

3.7 Thermal images

Figure 27 to **Figure 30** show the thermal images over the line and load range. The air flow is 600 FPM (with 7.5 V bias on the fan).

Figure 27 Thermal image taken at V_{in} = 42 V and I_{out} = 80 A

Figure 28 Thermal image taken at V_{in} = 48 V and I_{out} = 80 A

Experimental results

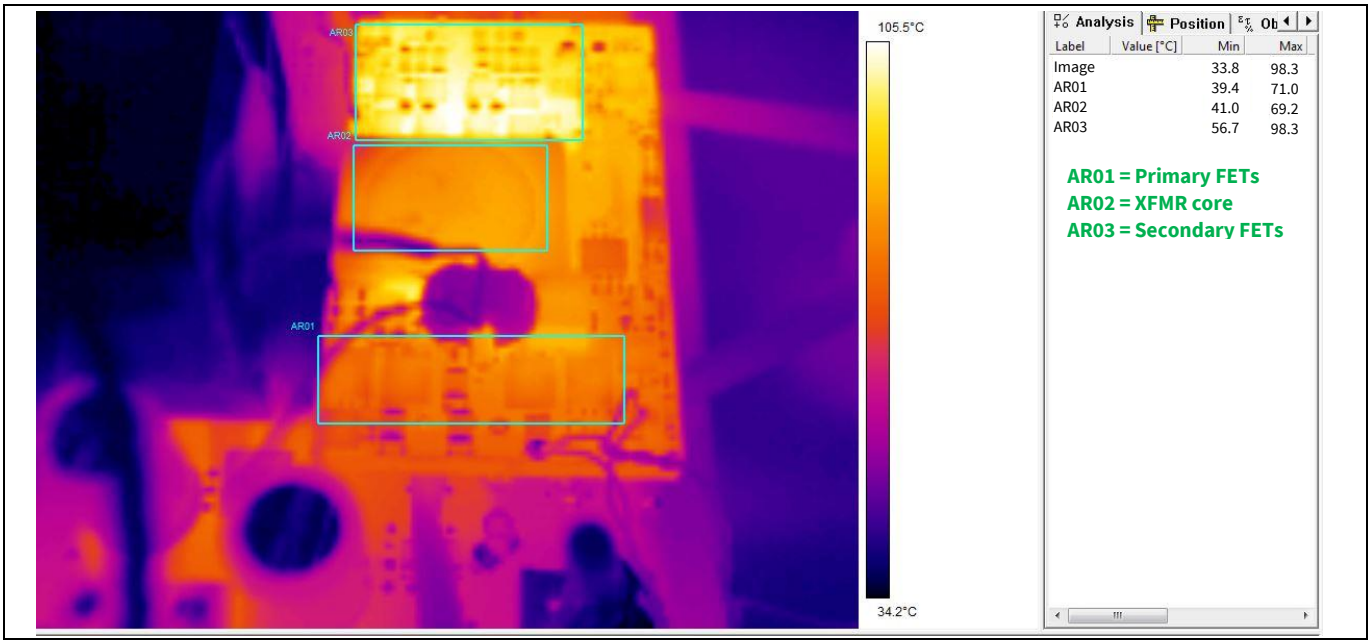


Figure 29 Thermal image taken at V_{in} = 56 V and I_{out} = 80 A

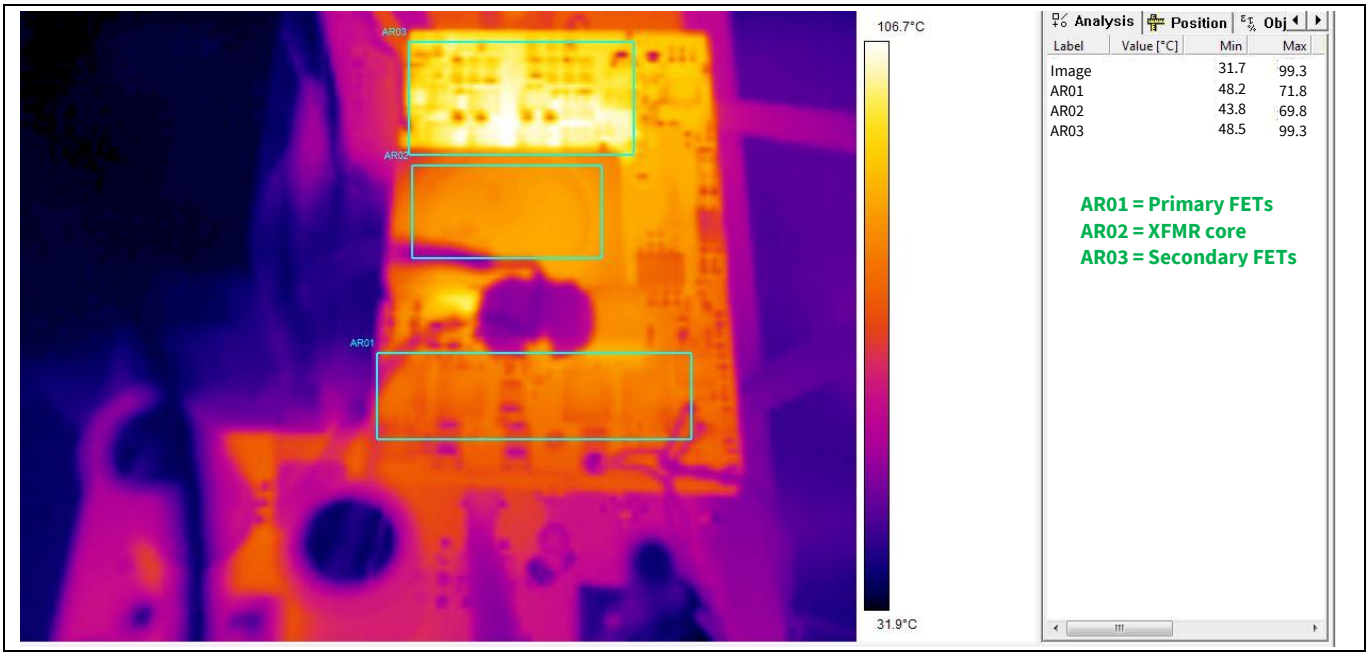


Figure 30 Thermal image taken at V_{in} = 60 V and I_{out} = 80 A

4 Summary

This document describes a complete Infineon solution for a 1 kW fixed-frequency LLC quarter-brick converter. The reference board has a standard DOSA-compliant quarter-brick footprint, and achieves 97.3 percent peak efficiency and power density of 564 W/in^3 (34.6 W/cm^3), which are enabled by the outstanding performance of Infineon's semiconductor devices.

The primary OptiMOS™ 6 80 V MOSFET (ISC033N08NM6) has an excellent FOM and superior switching performance. The low output capacitance reduces the required magnetizing current for ZVS operation in the LLC converter, minimizing circulating losses. The secondary OptiMOS™ 5 25 V MOSFET (IQE006NE2LM5) has an industry-leading $R_{DS(on)}$, significantly lowering the conduction losses of SRs in the LLC converter. The reduced form factor (PQFN 3.3x3.3 mm footprint) enables more FETs to be paralleled in the same space, which further reduces conduction losses and offers superior thermal management. Both the primary and secondary FETs are driven by Infineon's 2EDL8124G EiceDRIVER™ gate driver, a level-shift high-side low-side dual-channel driver offering differential input for superb robustness with inherent shoot-through protection.

Infineon's digital power controller XDPP1100-Q024 plays an essential role in optimal PWM timing generation, duty-cycle/frequency hybrid soft-start implementation, and enhanced protection in the fixed-frequency LLC quarter-brick converter. The industry's smallest digital power controller offers many optimized power processing blocks and pre-programmed peripherals, which enhances the performance of isolated DC-DC converters, reduces external components and minimizes firmware development effort.

5 Appendix

5.1 Mechanical outline

Figure 31 shows the mechanical outline for the 1 kW fixed-frequency LLC quarter-brick converter.

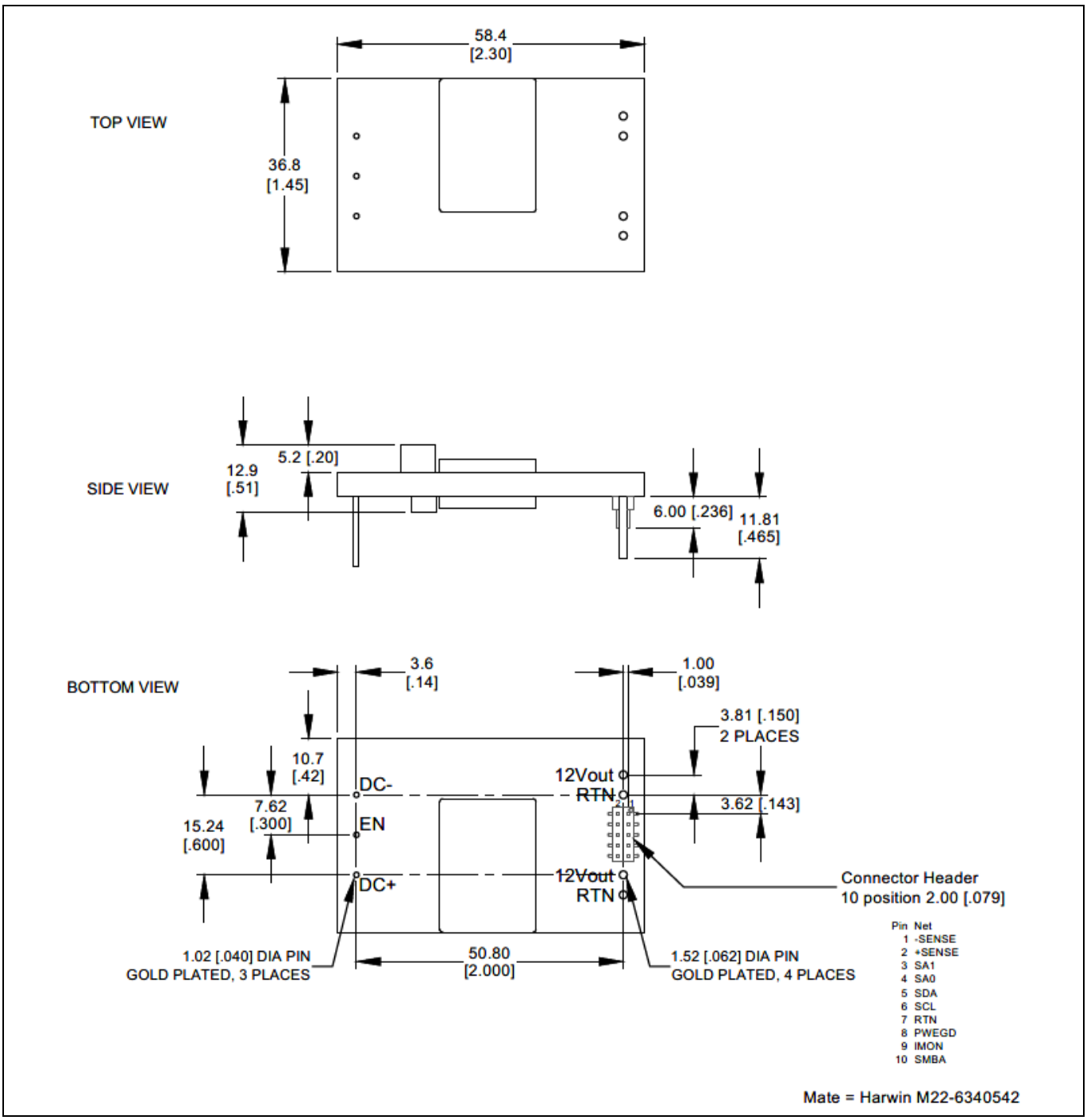


Figure 31 Mechanical outline

5.2 Bill of materials

Table 4 BOM

Item	Qty	Ref.	Manufacturer	Part number
1	1	BRD1		P100119 A
2	8	C1, C2, C3, C4, C5, C6, C7, C8	TDK	C3225X7R2A225K230
3	8	C9, C10, C17, C24, C58, C66, C69, C74	TDK	C1608X7R1H104K080
4	1	C11	TDK	C3216NP02A333J160
5	8	C12, C51, C60, C77, C78, C80, C81, C82	Murata	GRM31C5C1H224JE02L
6	5	C13, C18, C20, C21, C73	TDK	C1608C0G2A101K
7	1	C14	TDK	C1608X7R1H103K080
8	3	C15, C23, C57	Samsung	CL21B106KOQNNNE
9	1	C16	Kemet	C0603C472K2RACTU
10	1	C19	TDK	C3216C0G2A104J160AE
11	2	C22, C79	TDK	C1608X7R1H223K080
12	6	C25, C26, C56, C67, C75, C76	TDK	C1608X7R1E105K
13	1	C27	Kemet	C1206C102JGR
14	20	C28, C29, C30, C32, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C85, C86, C87	TDK	CGA5L1X8L1E106K160AC
15	1	C31	TDK	C1608C0G2A101K
16	1	C33	TDK	Not used
17	6	C47, C48, C49, C50, C53, C64	TDK	C1608X7R1H224K080
18	2	C70, C72	TDK	C1608C0G2A102J
19	2	C83, C84		Not used
20	1	DS1	Wurth	150060GS75000
21	3	D1, D2, D3	ON Semi	BAS20HT1G
22	1	D13	ON Semi	MM5Z5V1T1G
23	2	D16, D24	NXP	BAS516,135
24	4	D18, D19, D33, D43	Toshiba	CRH01 (TE85L, Q, M)
25	1	D44	ON Semi	MM5Z5V6T1G
26	1	J1	Harwin	M22-5320505
27	1	Lr	ICE	LP02-800-1S
28	8	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Infineon	ISC033N08NM6
29	16	Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24	Infineon	IQE006NE2LM5ATMA1
30	2	Q25, Q26	Toshiba	SSM3K15AMFV
31	1	RT2	Murata	NCP15WB473F03RC
32	1	R1	Panasonic	ERJ-3EKF3011V

Appendix

Item	Qty	Ref.	Manufacturer	Part number
33	3	R2, R70, R71	Panasonic	ERJ-3EKF1001V
34	9	R3, R4, R16, R20, R23, R26, R27, R28, R29	Panasonic	ERJ-3EKF1002V
35	4	R5, R6, R65, R87	Panasonic	ERJ-3EKF2001V
36	1	R7	Panasonic	ERJ-8ENF1500V
37	1	R9	Panasonic	ERA-3AEB103V
38	1	R10	Panasonic	ERA-3AEB112V
39	1	R12	Panasonic	ERJ-3EKF1202V
40	2	R13, R96	Panasonic	ERJ-3EKF20R0V
41	3	R14, R83, R84	Panasonic	ERJ-3EKF3321V
42	1	R15	Panasonic	ERJ-3EKF2002V
43	3	R17, R21, R22	Panasonic	ERJ-3EKF1000V
44	3	R18, R69, R73	Panasonic	Not used
45	1	R19	Panasonic	ERJ-3EKF2550V
46	4	R24, R25, R61, R89	Panasonic	ERJ-3GEY0R00V
47	24	R30, R31, R32, R38, R39, R40, R43, R44, R45, R46, R49, R50, R51, R52, R53, R54, R55, R56, R58, R63, R76, R77, R79, R80	Panasonic	ERJ-3RQF1R0V
48	1	R33	Panasonic	ERJ-3EKF51R1V
49	1	R34	Panasonic	ERA-3AEB104V
50	1	R35	Panasonic	ERA-3AEB132V
51	1	R36	Panasonic	ERJ-3EKF2213V
52	1	R37	Panasonic	ERJ-3EKF4871V
53	1	R47	Panasonic	ERJ-3EKF9531V
54	1	R48	Panasonic	ERJ-3EKF1741V
55	1	R57	Panasonic	ERJ-3EKF1243V
56	1	R62	Panasonic	ERJ-3EKF22R0V
57	2	R64, R81	Panasonic	ERJ-6RQF1R0V
58	2	R66, R86	Panasonic	ERJ-3EKF10R0V
59	1	R72	Panasonic	ERJ-3EKF1272V
60	1	R82	Panasonic	ERJ-6ENF5110V
61	1	R85	Panasonic	ERJ-6ENF2002V
62	10	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Harwin	S2761-46R
63	1	T1	Ferroxcube	EQ25-3F36 and PLT25/18/2-3F36
64	1	T3	Coilcraft	LPD5030V-224MR_B
65	1	U1	Infineon	XDPP1100-Q024
66	4	U2, U4, U5, U13	Infineon	2EDL8124GXUMA1
67	1	U10	Texas Instruments	OPA140AIDBVT
68	1	U11	Texas Instruments	LM5018SD/NOPB

Appendix

Item	Qty	Ref.	Manufacturer	Part number
69	1	U14	Toshiba	TLP2161 (TP, F)
70	1	U20	Analog Devices	LT1460KCS3-3.3#TRMPBF
71	1	U21	Fairchild	FODM8801A
72	1	W1		
73	3	1, 2, 3	Mil Max (input pins)	3104-3-00-15-00-00-08-0
74	4	4, 5, 9, 10	Mil Max (output pins)	4357-0-00-15-00-00-03-0

References

[1] OptiMOS™ 6 80 V MOSFET ISC033N08NM6 datasheet.

[2] OptiMOS™ 5 25 V MOSFET IQE006NE2LM5 datasheet.
https://www.infineon.com/cms/en/product/power/mosfet/12v-300v-n-channel-power-mosfet/iqe006ne2lm5/#

[3] EiceDRIVER™ gate driver 2EDL8x1x datasheet.

https://www.infineon.com/dgdl/Infineon-2EDL8012G-DataSheet-v02_01-EN.pdf?fileId=5546d4626c1f3dc3016c472fe8bf125b

[4] Digital power controller XDPP1100 datasheet.

https://www.infineon.com/dgdl/Infineon-XDPP1100-Q040-DataSheet-v01_02-EN.pdf?fileId=5546d462700c0ae6017084a8c9070d2a

[5] Application note, “The XDPP1100 digital power supply controller”, Infineon Technologies, July 2020.

https://www.infineon.com/dgdl/Infineon-Application_guide_digital_power_controler_XDPP1100-ApplicationNotes-v01_00-EN.pdf?fileId=5546d46272e49d2a01730aa45d53481b

Revision history

Document version	Date of release	Description of changes
V 1.0	30-09-2020	First release
V1.1	10-30-2020	Added power loss analysis

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Edition 2020-10-30

Published by

Infineon Technologies AG

81726 München, Germany

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Document reference

AN_2009_PL88_2010_014109

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