A COMPARISON BETWEEN TWO CURRENT-FED PUSH-PULL DC-DC CONVERTERS – ANALYSIS, DESIGN AND EXPERIMENTATION

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ABSTRACT

This paper compares two current-fed push-pull DC-DC converters: the Current-Fed Push-Pull Converter or Isolated Boost and an alternative topology named here as Dual Inductor Push-Pull Converter (DIC). Since this latter converter has just one primary winding the voltage across the main switches is reduced to the half of that in the Isolated Boost; the average current in the input inductors is also halved and the RMS current in the output capacitor results smaller. The overall efficiency is increased and the converter's volume is reduced in the DIC converter. These and other improved design characteristics make this alternative topology more attractive than the Isolated Boost for equivalent applications

Analytical equations, output characteristic curves and computer simulations of both the converters are compared. An experimental breadboard of 480W has been assembled in order to verify the performance of the DIC converter. The main results are provided.

1. INTRODUCTION

The well known Current-Fed Push-Pull DC-DC Converter is largely used by industry as battery chargers[1] or power factor correction circuits [2] due to their good operational characteristics, such as no possibility of flux unbalance [3] and good output cross regulation. Fig. 1. shows the topology of the Current-Fed Push-Pull or Isolated Boost Converter. Since it consists of just one input inductor it will be named hereafter simply as Single Inductor Converter (SIC). Although this converter features some very interesting characteristics some drawbacks are present in the topology, such as high output voltage ripple – requiring large filtering capacitors in the output –, high voltage across the main switches – twice the output voltage referred to the primary – and high volt-ampere rating for the transformer.

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In order to overcome these drawbacks, keeping the SIC good characteristics, an alternative topology is studied in comparison with the single inductor topology. This alternative converter[4] is also a current-fed converter, presenting boost characteristics, but it uses **two input inductors** instead of one and has an isolating transformer of just one primary coil. Its basic schematic is shown in Fig. 2, and is named hereafter as Dual Inductor Converter (DIC).

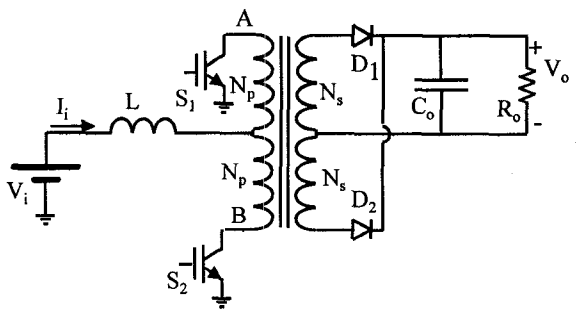

Fig. 1 Isolated boost (SIC).

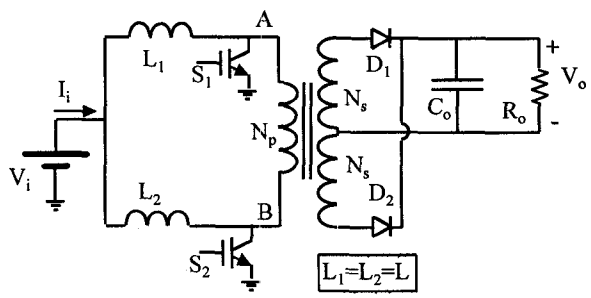

Fig. 2 Dual inductor converter (DIC).

As it will be demonstrated this alternative topology features improved design characteristics compared with the Isolated Boost (SIC). These characteristics will be verified from the analytical, simulation and experimental results presented in the following. The most important are listed below.

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i) The voltage across the main switches is reduced to the half of that in the SIC;
ii) Each input inductor results less current stressed since its average current is half that in the SIC.
iii) The rms current through the output capacitor is highly reduced since the peak secondary current is the half of that in the SIC;
iv) The current ripple in the output capacitor is also highly reduced as well as the output voltage ripple for the same equivalent series resistance of the output capacitor;
v) The volt-ampere rating of the transformer is reduced to the half of that in the single inductor converter, yielding to a smaller transformer;
vi) The input inductors are individually smaller than the unique input inductor of the SIC.

2. ANALYSIS OF THE DUAL INDUCTOR CONVERTER

2.1 - Operating Principle

The operating principle of the alternative converter is based on the same principle applied to the Single Inductor Converter: the switches are kept both in the **on** state in order the magnetization of the inductor to take place and are turned off, one after the other, so that the energy is transferred to the load via the transformer.

The discontinuous conduction mode (DCM) is not possible in these converters because of the presence of the **magnetizing inductance** of the isolating transformer. Even in the case of light loads, the inductor current reaches zero but immediately restarts its linear increasing due to the short circuit of the magnetizing inductance by means of one switch and one anti-parallel diode. Therefore the inductor current will be always in CCM, although in the case of light load the current will reach nearly zero (for a magnetizing current very small) and then we could designate this mode in a different way (to distinguish it from CCM) as Boundary Mode or Critical Mode (BM). And, in fact, in this mode the converter will operate very differently compared with the continuous one.

2.2 - Topological Stages In CCM

The topological operating stages, for a half-cycle of operation, involving the switch S_1, are described below.

- **1st Stage:** with both switches closed the primary winding is short-circuited and the current increases linearly in the input inductors according to a specified ripple. Energy is stored in the inductors while the output filter capacitor feeds the load. Fig. 3 shows the circuit for this topological stage.

- **2nd Stage:** when the switch S1 is turned-off its current is commutated to the primary winding which is submitted to the reflected output voltage and transfers energy to the load through the rectifier diodes. The voltage of this opened switch equals the reflected output voltage. Fig. 3 shows the circuit for this topological stage.

The drive signals and the main waveforms in continuous conduction mode (CCM) are presented in Fig. 4. These drive signals can be generated by inverting the outputs of a conventional PWM IC (3524).

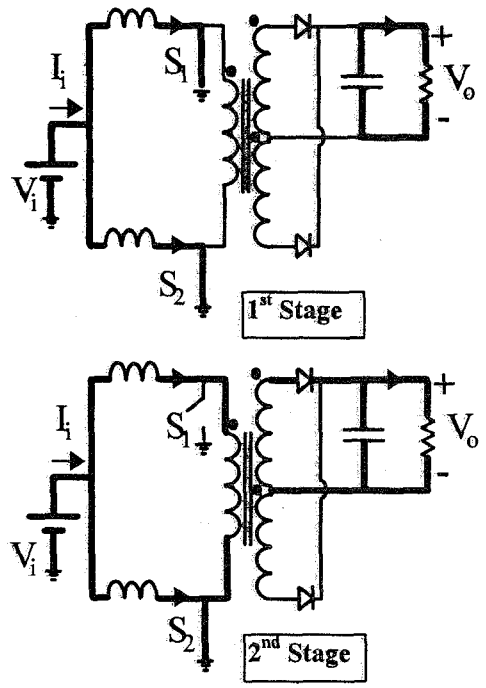

Fig. 3 DIC Topological stages in CCM.

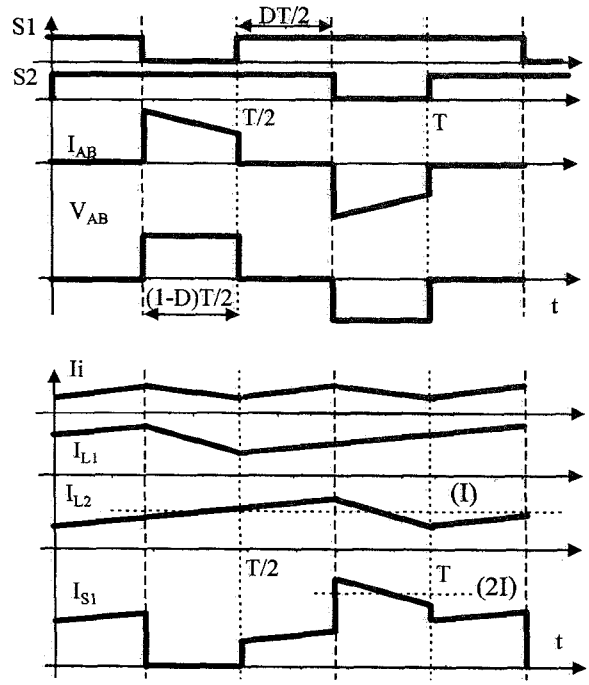

Fig. 4 DIC - drive signals and main waveforms .

2.3 - Derived Equations In CCM

- **Duty Cycle**

The duty cycle (D) is defined as the time period, beyond half a switching period, the switch is still kept on (Fig. 4). The dc current (I_i) in the input voltage source has a small and known current ripple (ΔI_i) on it and the switches share the half of this current, since through the primary flows no average current. Based on these definitions the mathematical relations of the converter can be derived.

- **Static Gain**

By the flux balance in the inductor and from the curves in Fig. 4 we have:

$$q = \frac{n \cdot V_o}{V_i} = \frac{2}{1-D} \qquad (1)$$

where $n = N_p/N_s$ is the turns ratio of the isolation transformer. With the relations obtained from Fig. 3 the following equations may be reached (for n = 1):

- **current ripple in the input source:**

$$\Delta\bar{I}_i = 4 \cdot D \qquad (2)$$

- **current ripple in one inductor:**

$$\Delta\bar{I} = 2 \cdot (1 + D) \qquad (3)$$

- **average current through the switch (I):**

$$\bar{I} = \frac{\bar{I}_o}{1-D} \qquad (4)$$

- **average current in the input source (I_i):**

$$\bar{I}_i = 2 \cdot \bar{I} \qquad (5)$$

All these equations are normalized with relation to a base current defined as ($V_i/4Lf_S$). For BM equivalent equations may also be derived, in order to plot overall output characteristics of the Dual Inductor Converter.

2.4 - Output Characteristics

The DIC output characteristics – static gain versus average output current – can be plotted from the expressions for the mode of operation, CCM, and also for the boundary mode, BM. Fig. 5 shows the resulting plot, where one can see how sharply the voltage gain increases as the converter reaches the situation in which the inductor current reaches zero periodically (BM). There is no discontinuous current mode, DCM, in this converter due to the always present magnetizing inductance of the transformer.

2.5 - Input Current Ripple

The current ripple in the input source depends just upon the duty cycle in the normalized equation, as seen in the expression (2). The plot of the variation of the input current ripple may be seen in Fig. 6 where one can also verify the increasingly ripple as the converter deepens in the BM.

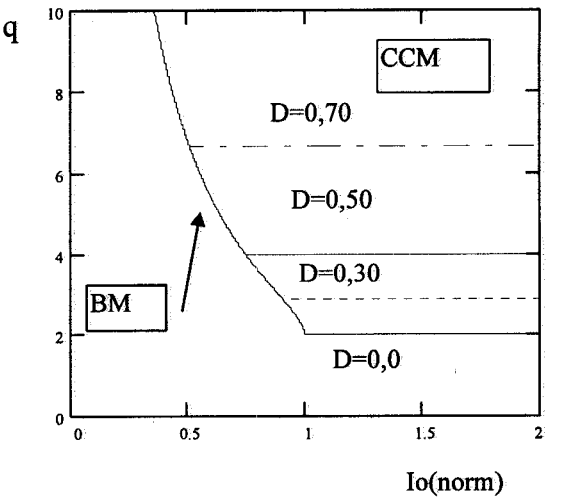

Fig. 5 Output characteristics of DIC.

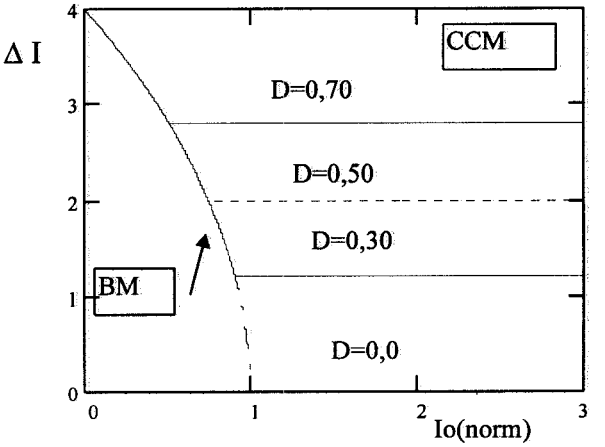

Fig. 6 Current ripple in the input source.

2.6 - RMS Current In the Output Filter Capacitor

The RMS current is an important factor of stress in the filter capacitor and should be evaluated. In the DIC converter the relation which establishes the rms current through the output filter capacitor is given by equation (6).

$$\bar{I}_c = \sqrt{\frac{q-2}{2}} \cdot \frac{n}{q} \cdot \bar{I}_i \qquad (6)$$

2.7 - Small Signal Transfer Function

By using the PWM switch model [5] the small signal transfer function for the DIC may be found:

$$\frac{\hat{v}(s)}{\hat{d}(s)} = \frac{K_d \cdot \left(1 + \frac{s}{s_{ESR}}\right)\left(1 - \frac{s}{s_{RHP}}\right)}{1 + s \cdot A + s^2 \cdot B} \qquad (7)$$

Where:

$$A=\frac{2\cdot L}{n^2\cdot(1-D)R_o} \qquad B=\frac{2\cdot L\cdot C_o}{(1-D)^2\cdot n^2} \tag{8}$$

$$K_d=\frac{4\cdot V_{in}}{n\cdot(1-D)^2} \quad s_{RHP}=\frac{2\cdot R_o\cdot n^2}{q^2\cdot L} \quad s_{ESR}=\frac{1}{R_{esr}\cdot C_o} \tag{9}$$

With these expressions, a compensation network can be designed in order to regulate the converter's output voltage.

3. SIMPLIFIED DESIGN METHODOLOGY

Based upon the specifications in Table 1, where the maximum primary voltage is also specified, taking into account the available semiconductor switch (IRF 640), the theoretical duty cycle may be calculated. From equation (1):

$$D=1-\frac{2\cdot V_i}{n\cdot V_o} \tag{10}$$

where $n\cdot V_o < V_{ds(max)}=200(V)$. By choosing an integer turns ratio equal to 3 $(n\cdot V_o=3\cdot 48=144<200)$ results:

$$D_{ideal}=0.333 \tag{11}$$

Simulation studies with the most realistic parameters indicate the need for correction in the theoretical duty cycle in order to reach the desired output voltage and power. An increase of around 10% in the duty cycle seems to be a good compensation for the idealized analysis. Therefore, the design duty cycle must be:

$$D=1.1\cdot D_{ideal} \tag{12}$$

$$D=1.1\cdot 0.333\cong 0.37 \tag{13}$$

Specifications for this design are listed in Table 1, which are the same for the SIC.

Table 1

Specifications	DIC/SIC
Rated power	480W
Input voltage	48V
Output voltage	48V
Switching frequency	100kHz
Input ripple	10%
Maximum switch voltage (V_{ds})	200V

An initial efficiency is supposed to calculate the input average current. Let's do it 90%. So the current gives

$$I_i=\frac{P_o}{0.90\cdot V_i}=11.1(A) \tag{14}$$

The remaining design steps are as follows.

- **Static gain:**

$$q=\frac{2}{1-D}=3.17 \tag{15}$$

- **Turns ratio:**

$$n=q\cdot\frac{V_i}{V_o+V_F}=3.17\cdot\frac{48}{48+1}\cong 3 \tag{16}$$

Where V_F is the forward voltage drop across the rectifier diode.

- **Input current ripple:**

$$\Delta I_i=0.1\cdot I_i=1.11A \tag{17}$$

- **Inductance**

$$L=\frac{V_i}{\Delta I_i\cdot f_s}\cdot D=160\mu H \tag{18}$$

- **Inductor current ripple:**

$$\Delta I=2\cdot(1+D)\cdot\frac{V_i}{4\cdot L\cdot f_s}=2A \tag{19}$$

- **Inrush current**: By means of a start-up resistor and a relay or any other means like the "clamping windings" in reference [6].
- **Switch voltage clamping capacitor**: Big enough to prevent a destructive switch overvoltage in case of an accidental lost of gate drive. It can be given by:

$$C_g=\frac{2\cdot L\cdot I_{L(max)}^2}{\left(V_{ds(max)}-V_g\right)^2}=230\mu F \tag{20}$$

4. COMPARISON BETWEEN THE CONVERTERS

In order to perform a comparison between the Single Inductor Converter and the Dual Inductor Converter the main equations of both the converters will be compared, specially through their representing plots, when useful. Figures 1 and 2 will be used here as the basic topologies to be compared. They will be considered equivalent converters in terms of rated power, input and output voltages and input current ripple. These equivalent design conditions require, as a consequence of the converters' describing equations, different duty cycles for the same operating point (output voltage and current). The relation of duty cycles in the converters is given by the expression below (21). The most important relations comparing the two converters are shown in Table 2.

$$D_{DIC}=2\cdot D_{SIC}-1 \tag{21}$$

4.1 Reverse Voltage Across the Switch

The well known SIC stresses the main switches with twice the output voltage referred to the transformer's primary winding. In the DIC converter the main switches are stressed by just the exact value of that voltage, since the isolation transformer, in this case, consists of just one

primary winding. The advantage of the alternative topology in this aspect is easily demonstrated and it is pointed out by the theoretical expressions in Table 2.

Table 2

Description	SIC converter	DIC converter
Input voltage source	V_i	V_i
Output voltage source	V_o	V_o
Input inductance	L (one)	L (two)
Voltage across the switch	$n \cdot 2 \cdot V_o$	$n \cdot V_o$
Isolation transformer	2 primary coils	1 primary coil
Duty cycle	D=0.66	D=0.33
Input inductor current	I_i	$0.5 \cdot I_i$
Current ripple in the output capacitor *	$\Delta i_c = I_i \cdot n$ $(n=3)$	$\Delta i_c = I_i \cdot \frac{n}{2}$
Transformer peak volt-ampere *	$S = n.V_o.I_i$	$S = n.V_o.I_i/2$
Switch rms current *	$\frac{\sqrt{2-D}}{2} \cdot \bar{I}_i = 0.65 \cdot \bar{I}_i$	$\frac{\sqrt{2-D}}{2} \cdot \bar{I}_i = 0.58 \cdot \bar{I}_i$
Inductor switching frequency	$2.f_s$	f_s
Rms current in the output capacitor *	$\sqrt{q-1} \cdot \frac{n}{q} \cdot I_i = \sqrt{2} \cdot I_i$	$\sqrt{\frac{q-2}{2}} \cdot \frac{n}{q} \cdot I_i = \frac{\sqrt{2}}{2} \cdot I_i$
* Input current source considered ripple free.		

4.2 - Utilization of The Isolation Transformer

The isolation transformers in both isolated converters are very differently utilized in terms of power handling capability. While the SIC transformer has two primary windings and carries exactly the switch current through each of them, the DIC transformer has just one primary and carries just a part of the switch current , that is, only the part needed for power transfer. It means that the DIC transformer is more efficiently used than the SIC one: the first handles half the volt-ampere handled by the second, for the same output power.

4.3 - Volume of the Input Inductors

One can easily demonstrate that the core's volume of each input inductor in the DIC converter tends to be smaller than that needed for the SIC converter. It comes from the fact that this volume depends upon the product of the rms and the peak inductor currents and being greater these currents for the SIC converter, the size of its inductor will be also bigger than the ones of the inductors in the DIC converter. Therefore the two inductor taken together won't be much greater than the unique inductor of the SIC.

4.4 - Output Filter Capacitor

The size of the output capacitor depends on its rms current stress and on the current ripple that flows through it. The lower this current ripple the greater can be the equivalent series resistance of the output capacitor for the same specified output voltage ripple and the lower its capacitance. Both these values, rms current and current ripple are smaller for the DIC converter than those for the SIC one. Fig. 7 shows the variations of these currents for both the converters, against the static gain, which is the same for the two converters. These plots are based upon the correspondent equations presented in Table 2.

4.5 - Efficiency of the Converters

The efficiencies are also different, being greatest the one of the DIC converter, since the magnetics present losses smaller than those presented by the SIC converter. And the total losses in the DIC inductors will be half that of the SIC converter, since an average current two times greater will flow through the SIC unique input inductor.

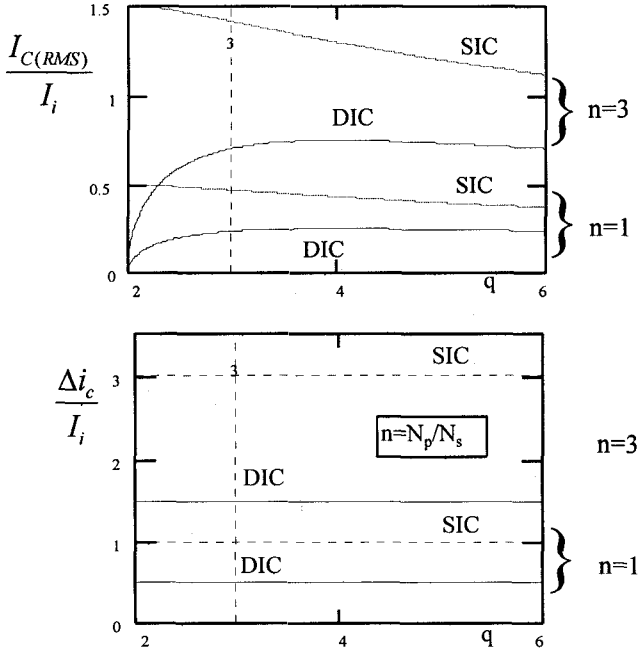

Fig. 7 Rms current and ripple in the filter capacitor.

4.6 - Global Comparison

Figure 8 plots the curves for the static gain, the input current ripple and for the voltage across the switch (V_S). The curve for the static gain of the DIC converter coincides with that for the V_S for both the converters. Each converter, however, should operate in a different duty cycle for equivalent output power.

4.7 - Simulation Results

Simulation results of the main waveforms for both converters, handling equal output power, are compared by highlighting the differences between the voltages across the switch and the rms current through the output capacitor. The specifications are those in Table 1. Figures 9-12 present the comparative simulation results.

The SIC switch voltage is clearly twice that in the DIC, according to the V_s curve, while the input current ripple in both of them is made equal by design choice (horizontal dotted line marked 1.3).

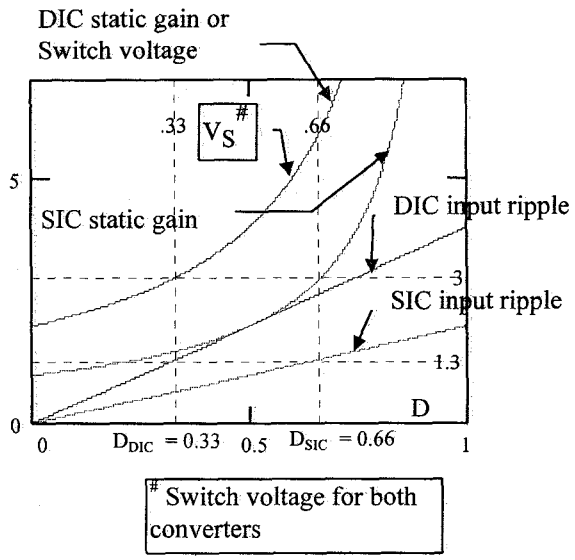

Fig. 8 Global comparison between the converters.

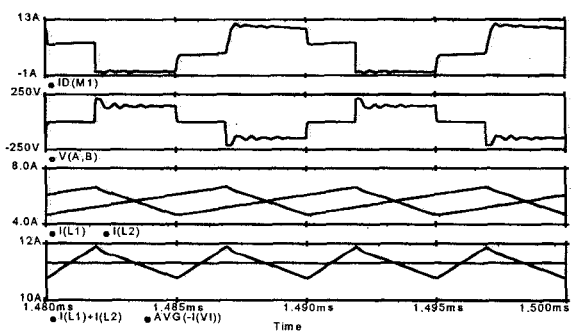

Fig. 9 Waveforms to rated output (DIC); from de top: Mosfet current, primary voltage, input inductor currents, input source current.

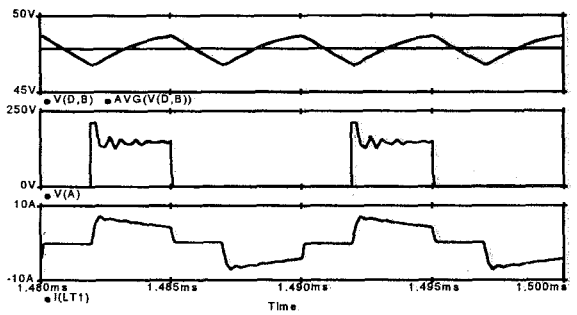

Fig. 10 Waveforms for rated output (DIC); from the top: output voltage, Mosfet voltage, primary current.

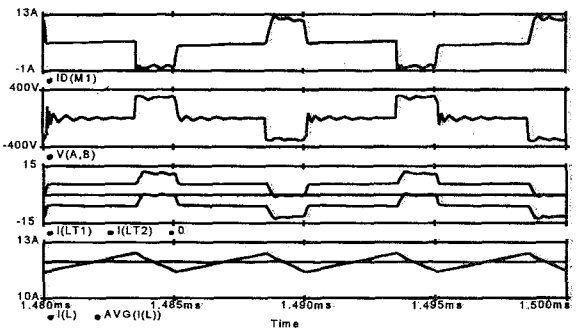

Fig. 11 Waveforms to rated output (SIC); from de top: Mosfet current, (primary-1+primary-2) voltage, primary-1 and primary-2 currents, input current source.

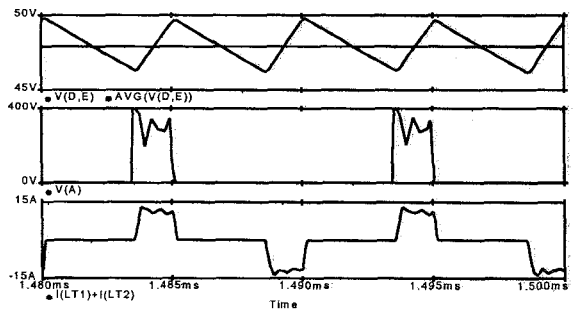

Fig. 12 Waveforms for rated output (SIC); from the top: output voltage, Mosfet voltage, primary current.

4.8 - Experimental Results

For the same specifications used in the above simulations, a 480W breadboard was assembled in order to verify the theoretical and simulation results. Fig. 16 shows the DIC main waveforms to an output situation of 42V/9A, under duty cycle of 33%. The turns ratio was designed to be equal to 3 (N_p/N_s=3).

shows the power diagram of the assembled converter. The gate drive and control circuit is shown in Fig. 14, while the auxiliary power supply is presented in Fig. 15.

The predicted waveforms of figures 9 and 10 are verified by those in the experimental results of Fig. 16.

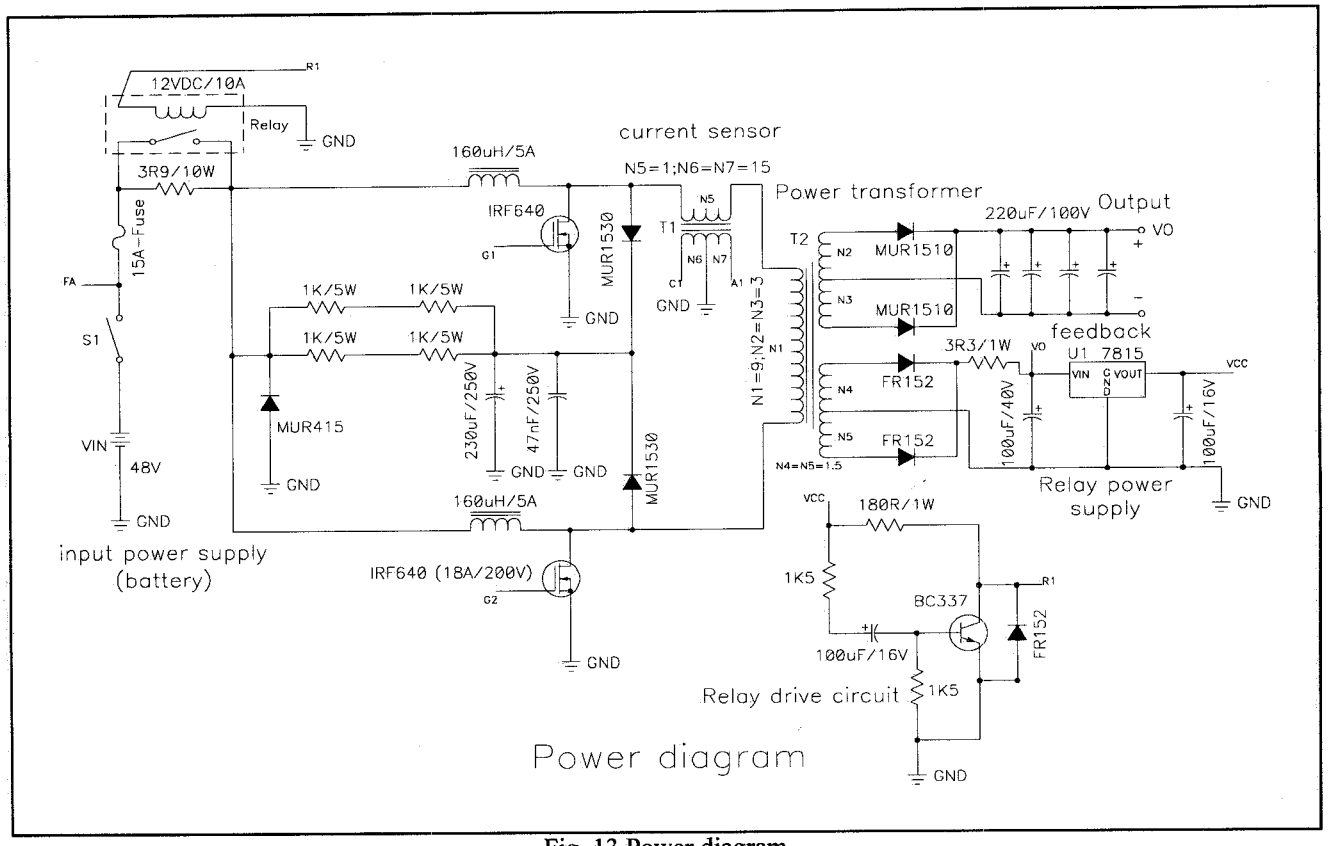

Fig. 13 Power diagram

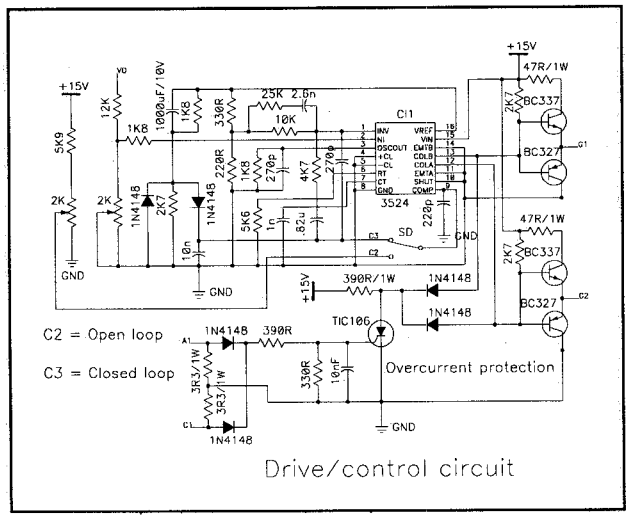

Fig. 14 Drive and control circuit

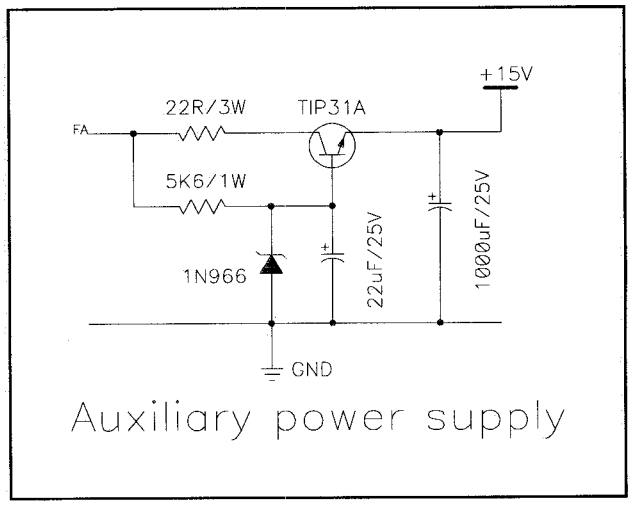

Fig. 15 Auxiliary power supply

4.8.1 - Output Characteristics

The experimental, simulated and theoretical (ideal) output characteristics are shown in Fig. 17. The difference between the ideal and simulated curves reflects the use of realistic devices and parameters in the simulated case, while the ideal one is that derived from the idealized mathematical analysis. The experimental characteristic follows the simulated one with an expected extra voltage drop.

4.8.2 - Experimental Efficiency

Since this converter breadboad is designed for low voltage and relatively high current in both output and input stages (48V/10A), and it does not make use of any soft switching circuitry the theoretical efficiency is not expected to be very high, reaching around 90%. Fig y shows the efficiency curve for the assembled DIC converter in the range of 1.5A to 10A, in open loop.

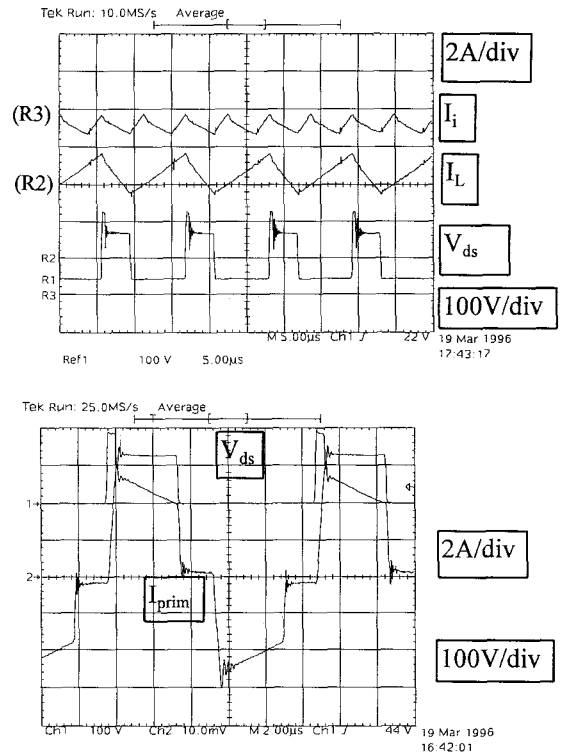

Fig. 16 Experimental results. From the top: input current; inductor current; Mosfet voltage; primary current.

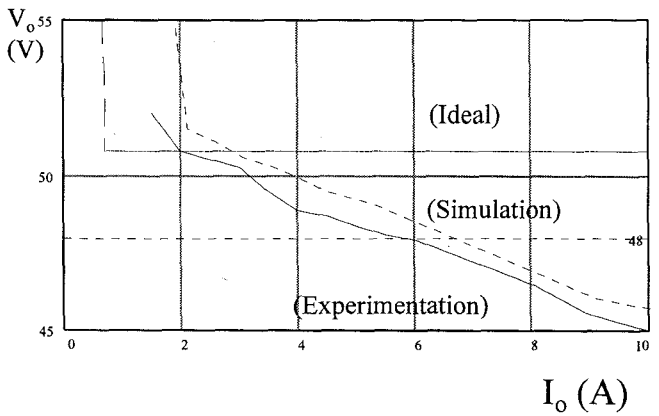

Fig. 17 Output static characteristics for DIC

The reasons for the lower experimental efficiency are related to: the use of a passive clamping circuit (around 4% of losses), the turn-on commutation and conduction losses in the power switches (around 4% of losses), and the magnetic and ohmic losses in the magnetics.

5. CONCLUSION

This paper presented a comparison between two different current-fed push-pull converters named: Single Inductor Converter (known as Isolated Boost) and Dual Inductor Converter (or Dual Inductor Push-Pull Converter).

The comparison has been made taking into consideration the descriptive equations, the output characteristics and

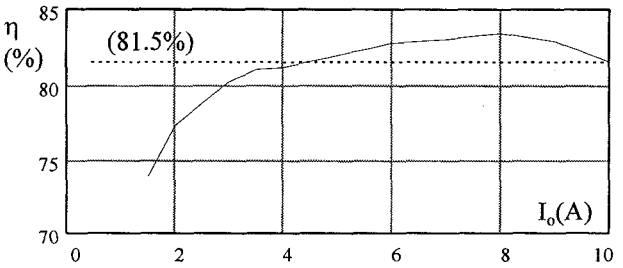

Fig. 18 Experimental efficiency

simulations, for both converters, and experimentation for the DIC converter.

The alternative Dual Inductor Current-Fed Push-Pull Converter is favorably compared concerning design characteristics. With the exception of the rms current through the switches – which is slightly greater than that in the Isolated Boost – all the other parameters and quantities are favorable to the Dual Inductor Converter which has, also, boost-like characteristics.

Other advantages may be cited: the switches are less voltage stressed; the single-primary isolation transformer is more efficiently utilized with a smaller volume; the filtering output capacitor can be smaller for the same output power.

The authors believe that this alternative converter topology can substitute the Isolated Boost with many advantages in the low voltage and high current applications range. Besides this it can be current sourced by two independent sources what enlarges its possible applications, including the use of the line side interfase transformer to reach a high power factor switching power supply.

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