INTRODUCTION

Data in data sheets is presented - whenever possible - according to a 'format', in which the following chapters are stated:

- TITLE
- FEATURES
- APPLICATIONS
- DESCRIPTION
- QUICK REFERENCE DATA
- ORDERING INFORMATION
- FUNCTIONAL DESCRIPTION
  - Product characterization
  - Limiting values
- MECHANICAL DATA
  - Mass
  - Marking
  - Outlines
- TESTS AND REQUIREMENTS

The items listed above are explained in this section *"General Introduction Chip resistors"*, with detailed information in the relevant data sheet. The chapters "Mounting" and "Packaging" are only detailed in the *"General Introduction Chip resistors"*.

DESCRIPTION

All types of chip resistors have a rectangular ceramic body. The resistive element is a metal glaze film. The chips have been trimmed to the required ohmic resistance by cutting one or more grooves in the resistive layer. This process is completely computer controlled and yields a high reliability. The terminations are attached using either a silver dipping method or by applying nickel terminations which are covered with lead/tin.

The resistive layer is coated with a coloured protective layer. This protective layer provides electrical, mechanical and/or environmental protection - also against soldering flux and cleaning solvents, in accordance with *"MIL-STD-202E"*, method 215 and *"IEC 68-2-45"*.

ORDERING INFORMATION

Resistors are ordered by their **ordering code**, a 12-digit number. In general, the packaging method and resistance code are integral parts of this number. Exceptions to this rule are customer/application specific resistors that are not included in our standard series, such as higher ohmic values and non-standard values.

FUNCTIONAL DESCRIPTION

The functional description includes: nominal resistance range and tolerance, limiting voltage, temperature coefficient, absolute maximum dissipation, climatic category and stability.

The **limiting voltage** (DC or RMS) is the maximum voltage that may be continuously applied to the resistor element, see *"IEC publications 115-8".*

The temperature rise in a resistor due to power dissipation, is determined by the laws of heat - conduction, convection and radiation. The maximum body temperature usually occurs in the middle of the resistor and is called the **hot-spot** temperature.

In the normal operating temperature range of chip resistors the temperature rise at the hot-spot, ΔT, is proportional to the power dissipated: $\Delta T = A \times P$. The proportionally constant 'A' gives the temperature rise per Watt of dissipated power and can be interpreted as a thermal resistance in K/W. This thermal resistance is dependent on the heat conductivity of the materials used (including the PCB), the way of mounting and the dimensions of the resistor. The sum of the temperature rise and the ambient temperature is:

$T_m = T_{amb} + \Delta T$

where:

T_m = hot-spot temperature

T_{amb} = ambient temperature

ΔT = temperature rise at hot-spot.

The stability of a chip resistor during endurance tests is mainly determined by the hot-spot temperature and the resistive materials used.

Summarizing

DESCRIPTION	RELATIONSHIP
Dimensions, conductance of materials and mounting determine	heat resistance
Heat resistance $\times$ dissipation gives	temperature rise
Temperature rise + ambient temperature give	hot-spot temperature

Performance

When specifying the performance of a resistor, the dissipation is given as a function of the hot-spot temperature, with the ambient temperature as a parameter.

From $\Delta T = A \times P$ and $T_m = T_{amb} + \Delta T$ it follows that:

$$P = \frac{T_m - T_{amb}}{A}$$

If P is plotted against T_m for a constant value of A, parallel straight lines are obtained for different values of the ambient temperature. The slope of these lines,

$$\frac{dP}{dT_m} = \frac{1}{A}$$

is the reciprocal of the heat resistance and is the characteristic for the resistor and its environment.

The temperature coefficient

The temperature coefficient of resistance is a ratio which indicates the rate of increase (decrease) of resistance per Kelvin (K) increase (decrease) of temperature within a specified range, and is expressed in parts per million per K ($\times 10^{-6}$/K).

Example: If the temperature coefficient of a resistor of R_{nom} = 1 kΩ between –55 °C and +155 °C is $\pm 200 \times 10^{-6}$/K, its resistance will be,

at 25 °C:

1000 Ω (nominal = rated value)

at +155 °C:

$1000\ \Omega \pm (130 \times 200 \times 10^{-6}) \times 1000\ \Omega$
= 1026 Ω or 974 Ω

at –55 °C:

$1000\ \Omega \pm (80 \times 200 \times 10^{-6}) \times 1000\ \Omega$
= 1016 Ω or 984 Ω

If the temperature coefficient is specified as $\leq 200 \times 10^{-6}$/K the resistance will be within the shaded area as shown in Fig.1.

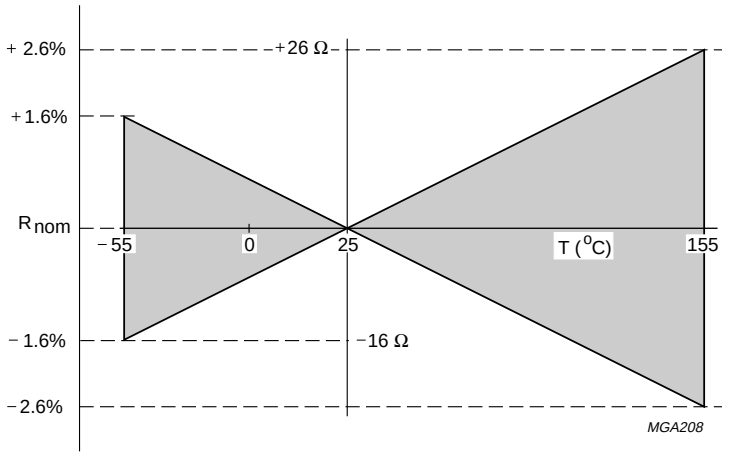

Fig.1 Temperature coefficient.

Noise

Most resistors generate noise due to the passage of current through the resistor. This noise is dependent on the amount of current, the resistive material and the physical construction of the resistor. The physical construction is partly influenced by the laser trimming process which cuts a groove in the resistive material. Typical current noise levels are shown in Fig.2.

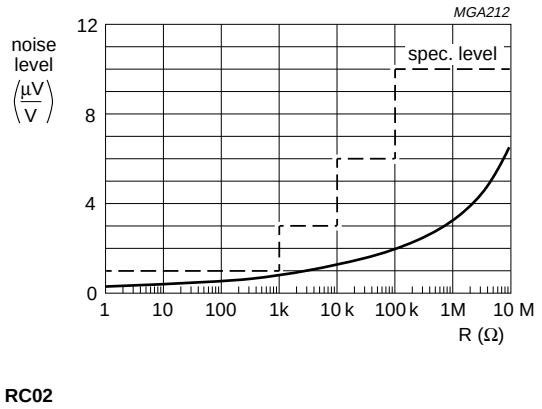

Fig.2 Typical noise levels as a function of rated resistance.

Frequency behaviour

Resistors in general are designed to function according to ohmic laws. This is basically true of rectangular chip resistors for frequencies up to 100 kHz. At higher frequencies, the capacitance of the terminations and the inductance of the resistive path length begin to have an effect.

Basically, chip resistors can be represented by an ideal resistor switched in series with a coil and both switched parallel to a capacitor. The values of the capacitance and inductance are mainly determined by the dimensions of the terminations and the conductive path length. The trimming pattern has a negligible influence on the inductance as the path length is not influenced. Also, its influence on the capacitance is negligible as the total capacitance is largely determined by the terminations.

The environment surrounding chips (e.g. landing paths, nearby tracks and the material of the printed-circuit board) has a large influence on the behaviour of the chip on the printed-circuit board.

Typical values of capacitance and inductance

QUANTITY	CHIP PROPERTIES			
	THIN FILM	THICK FILM		
	1206 R < 1 kΩ	1206	0805	0603
Capacitance	0.05 pF	0.05 pF	0.09 pF	0.05 pF
Inductance	2 nH	2 nH	1 nH	0.4 nH

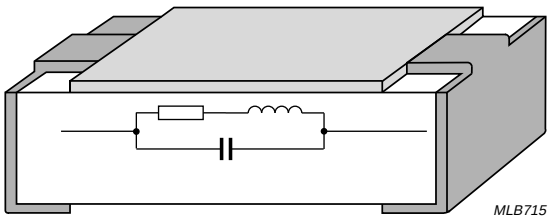

Fig.3 Equivalent circuit.

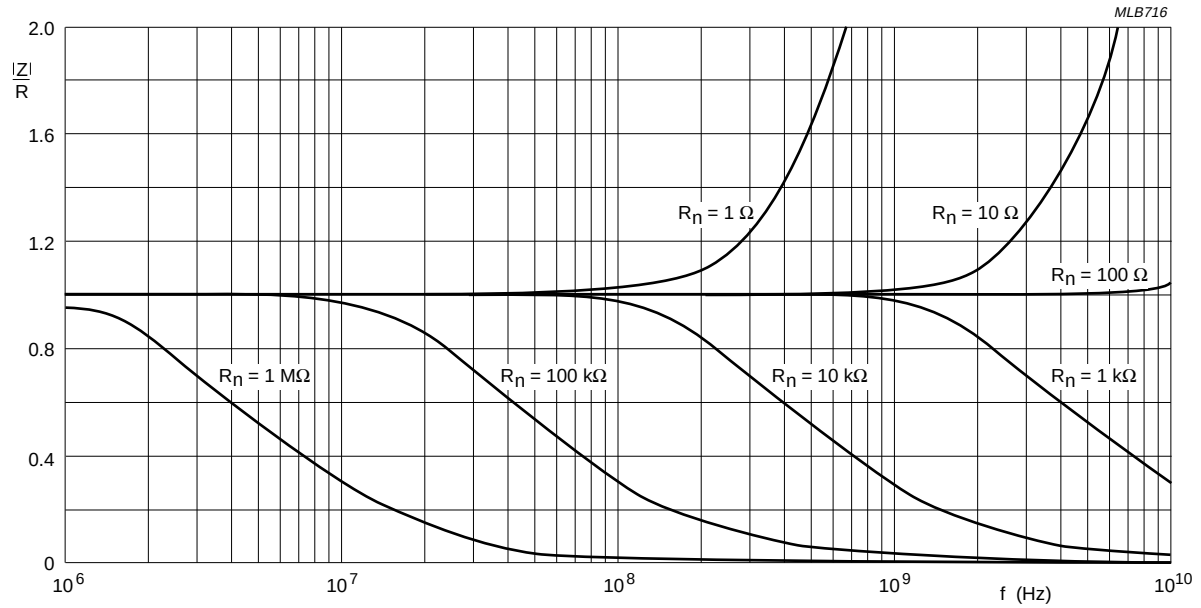

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Fig.4 Impedance as a function of frequency for a chip resistor.

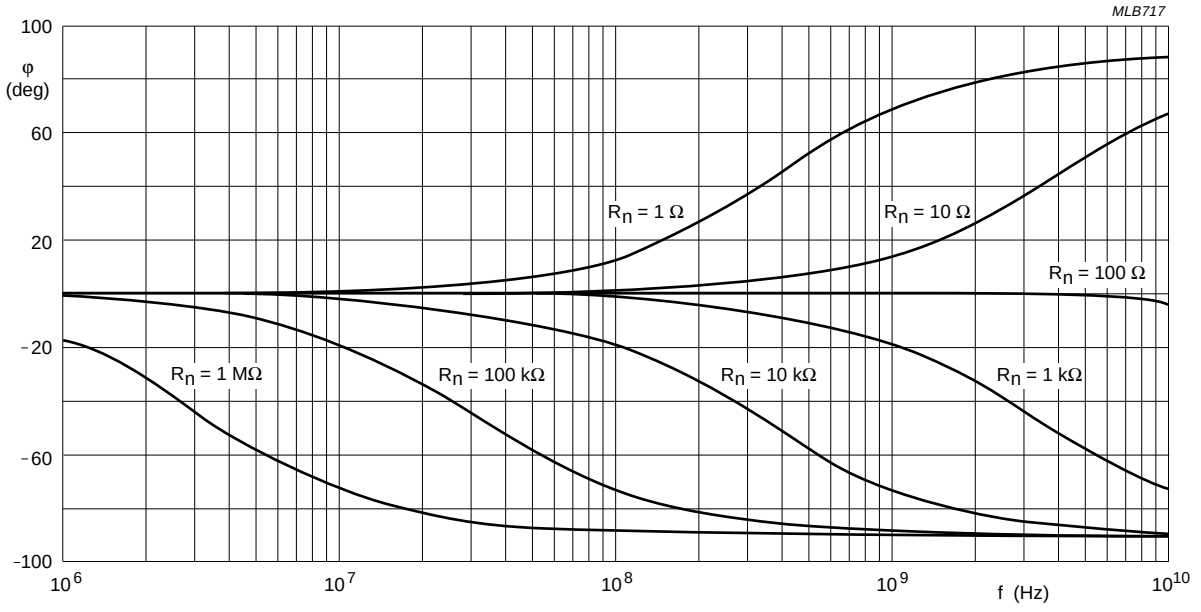

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Fig.5 Phase shift as a function of frequency for a chip resistor.

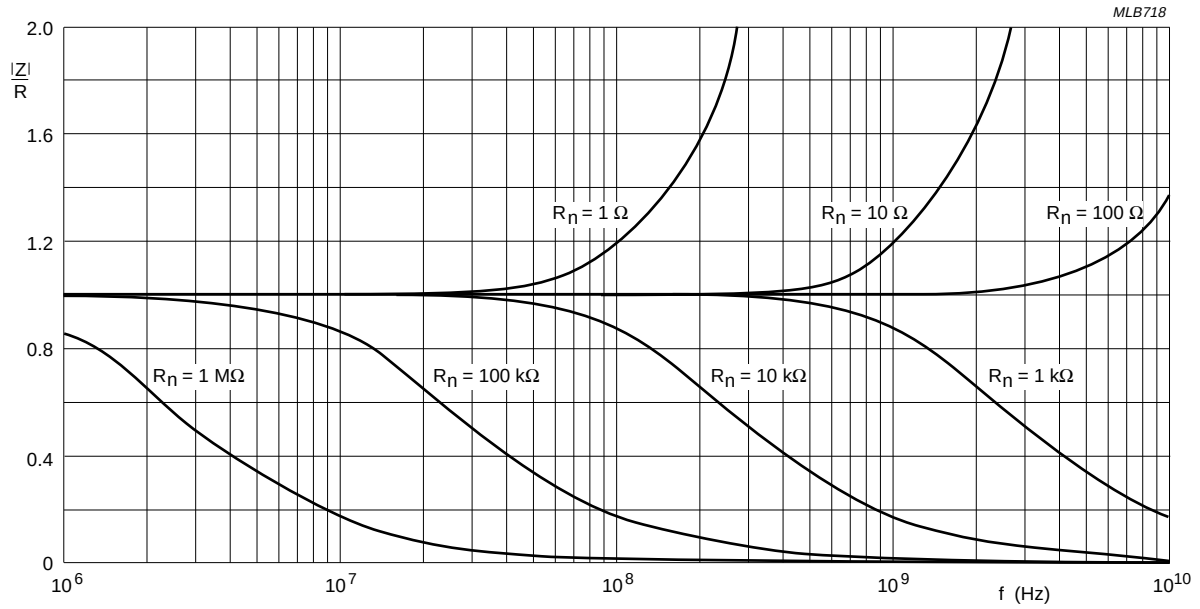

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Fig.6 Impedance as a function of frequency for a chip resistor.

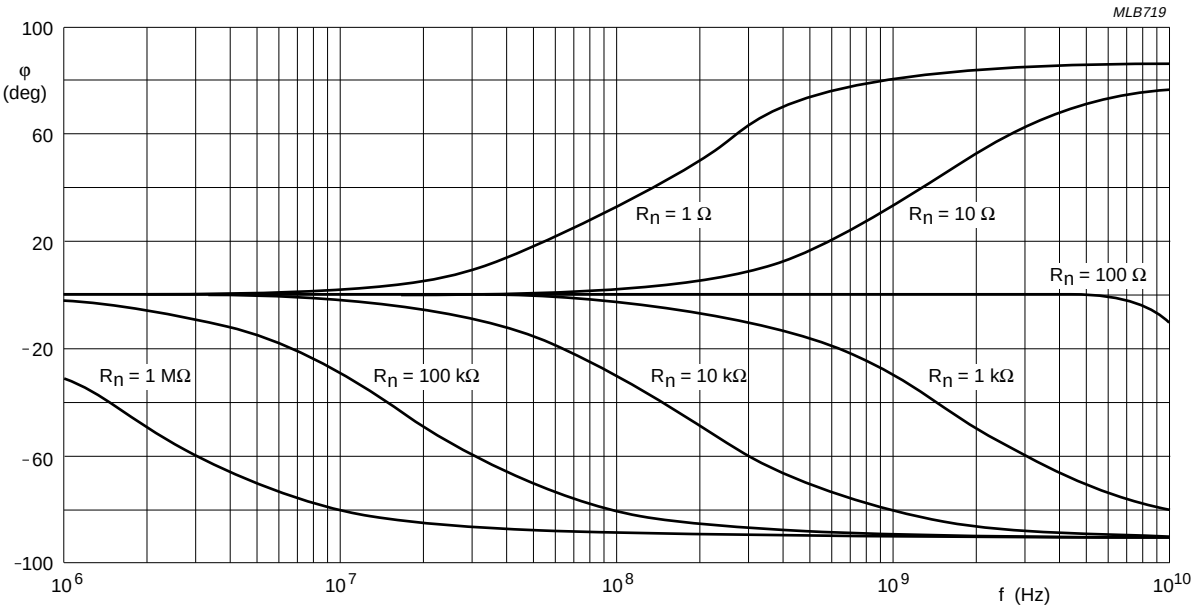

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Fig.7 Phase shift as a function of frequency for a chip resistor.

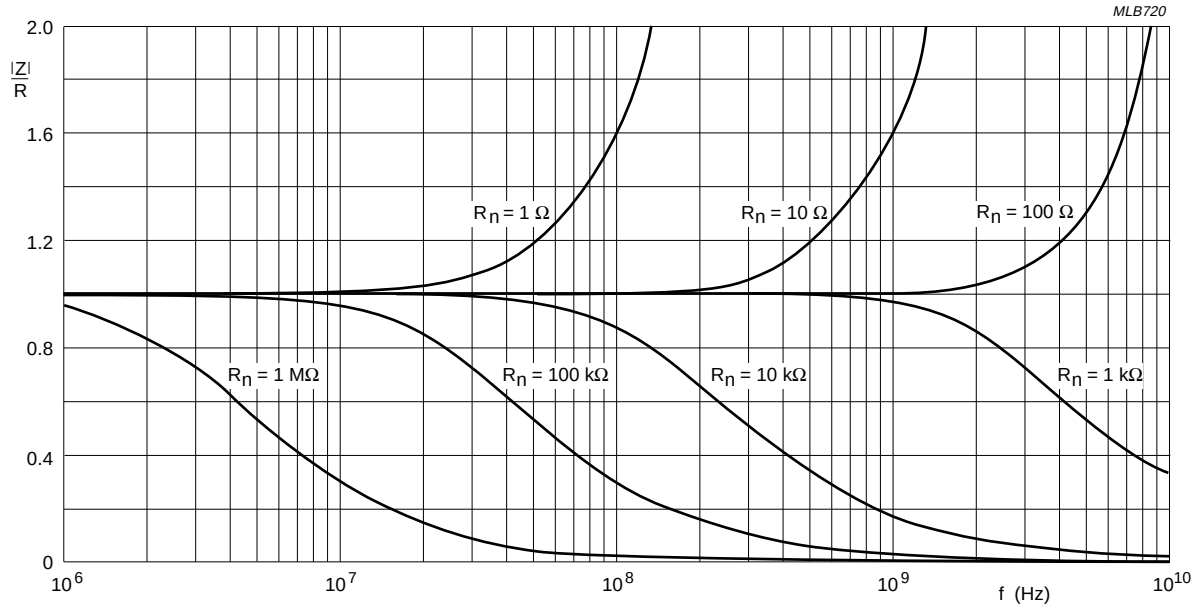

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Fig.8 Impedance as a function of frequency for a chip resistor.

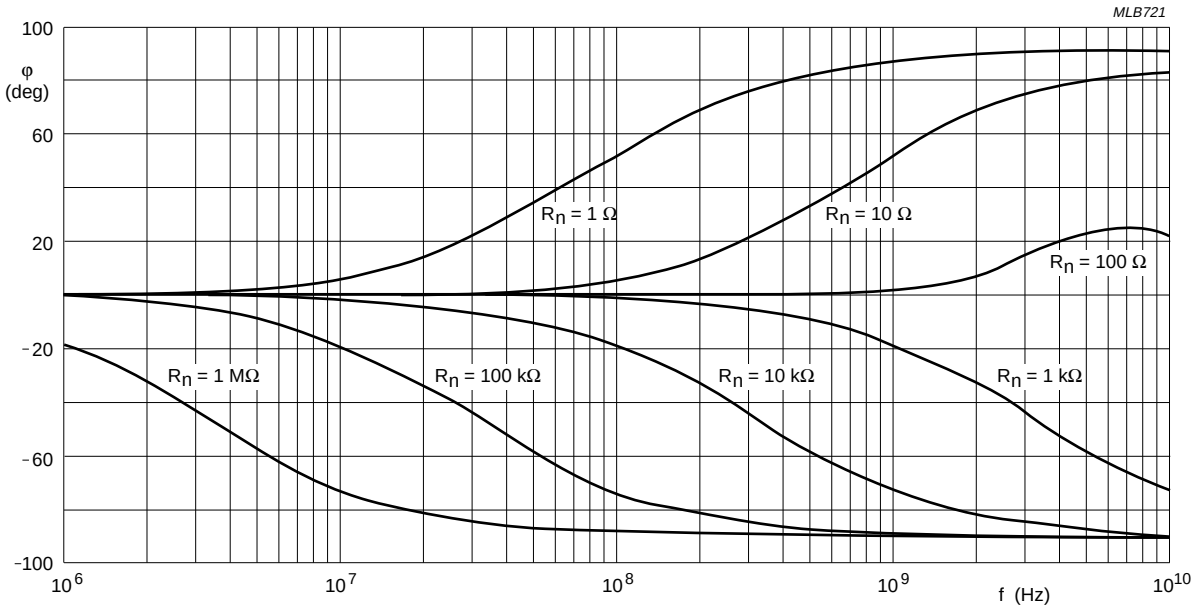

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Fig.9 Phase shift as a function of frequency for a chip resistor.

PULSE-LOAD BEHAVIOUR

The load, due to a single pulse at which chip resistors fail by going open circuit, is determined by shape and time. A standard way to establish pulse load limits is shown in Table 1.

Table 1 Pulse load limits

PARAMETER	VALUE	UNIT
Exponential time constant	50 to 700	μs
Repetition time	12 to 25	s
Amount of pulses	5 to 10	

With this test, it can be determined at which applied voltage the resistive value changes about 0.5% of its nominal value under the above mentioned pulse conditions. Figure 10 shows test results for the RC02 chip resistors. If applied regularly the load is destructive, therefore the load must not be applied regularly during the load life of the resistors. However, the magnitude of a pulse at which failure occurs is of little practical value. The maximum ‘single-pulse’ load that may be applied in a regular way can be determined in a similar manner.

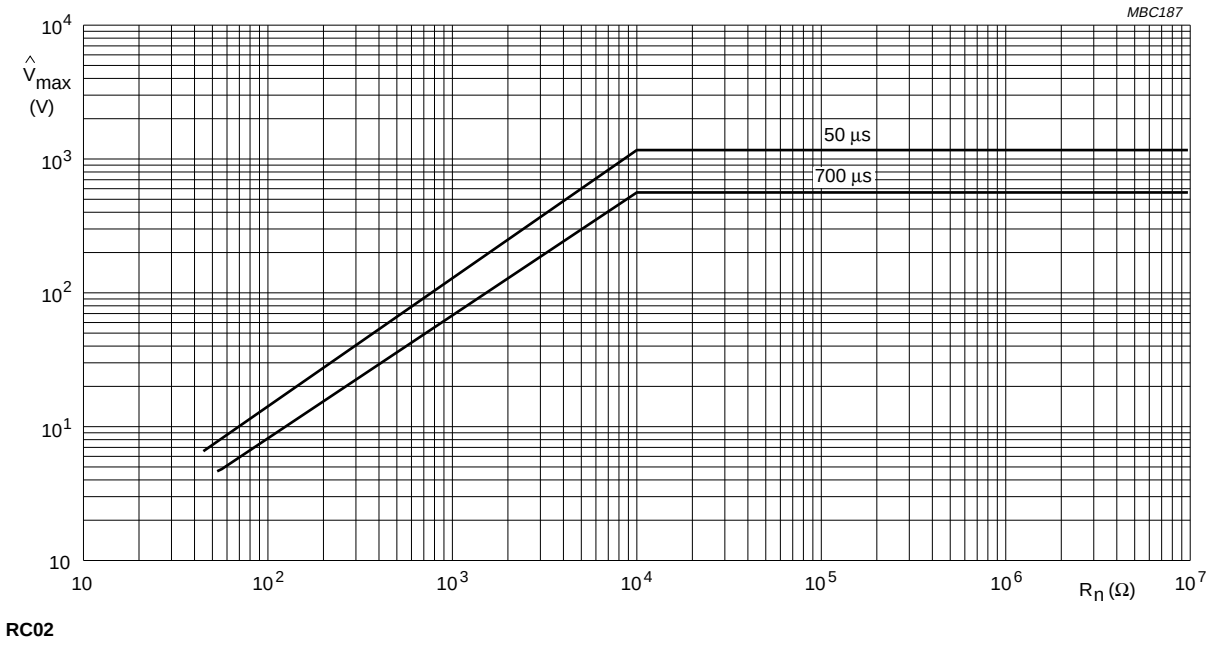


Fig.10 Maximum permissible peak pulse voltage ($\hat{V}_{max}$) without failing to ‘open circuit’ in accordance with DIN IEC 40 (CO) 533.

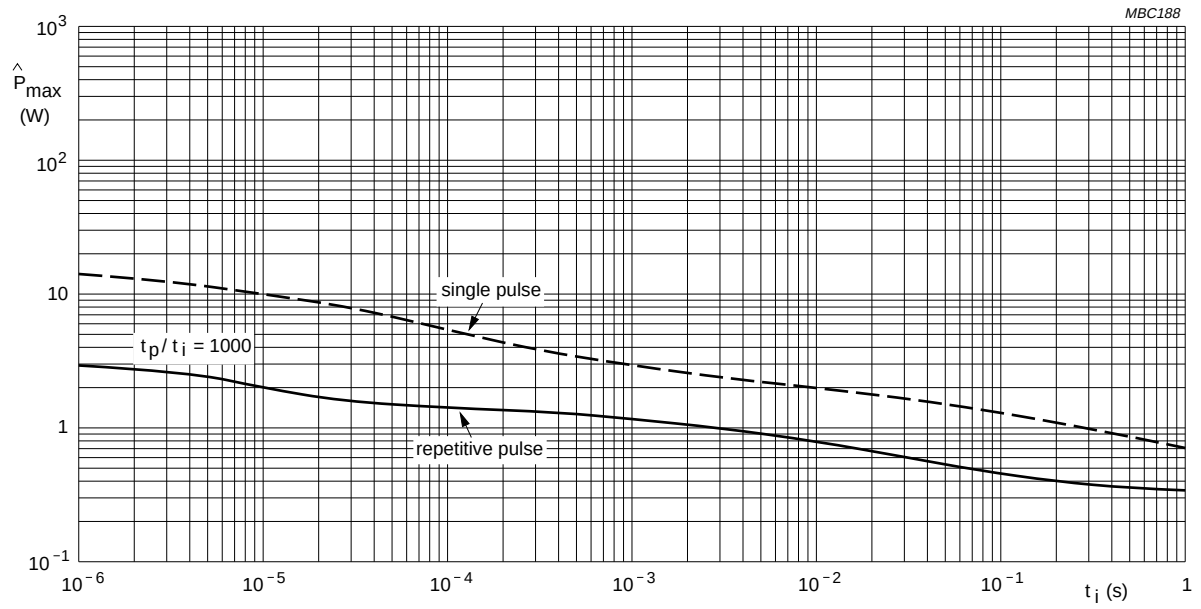


Fig.11 Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max}$) as a function of pulse duration for R ≤ 10 kΩ, single pulse and repetitive pulse t_p/t_i = 1000.

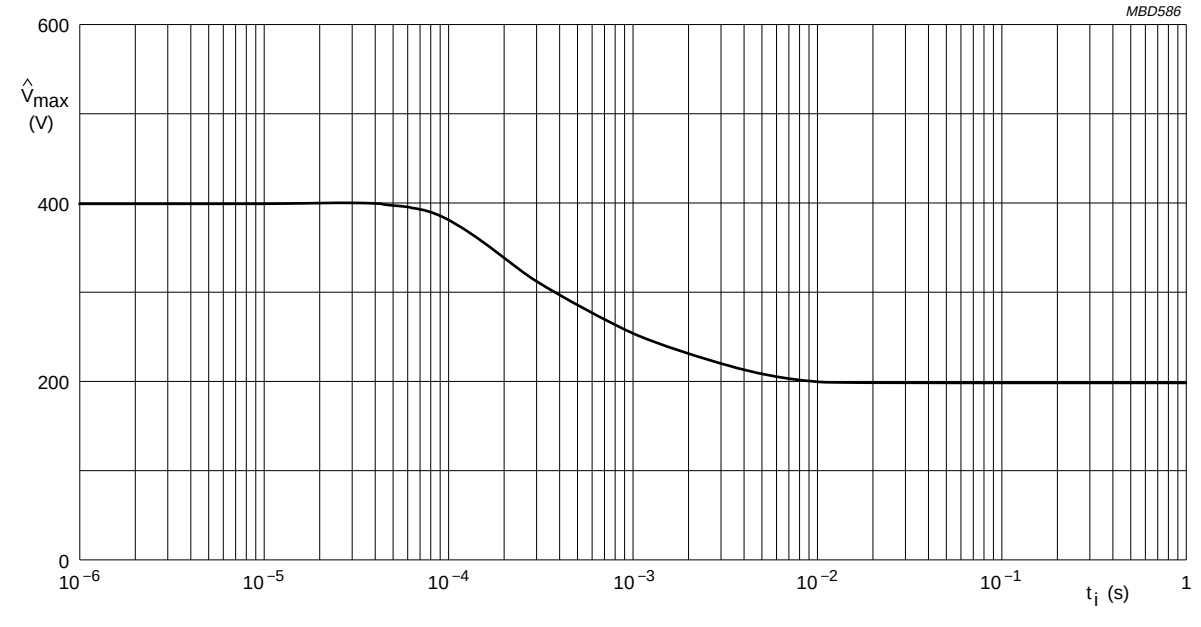


Fig.12 Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{V}_{max}$) as a function of pulse duration (t_i).

Definitions of pulses

SINGLE PULSE

The resistor is considered to be operating under single pulse conditions if, during its life, it is loaded with a limited number (approximately 1500) of pulses over long time intervals (greater than one hour).

REPETITIVE PULSE

The resistor is operating under repetitive pulse conditions if it is loaded by a continuous train of pulses of similar power.

The dashed line in Fig.11 shows the observed maximum load for the RC02G chip resistors under single-pulse loading.

More usually, the resistor must withstand a continuous train of pulses of repetition time 't_p' during which only a small resistance change is acceptable. This resistance change ($\Delta R/R$) is equal to the change permissible under continuous load conditions. The continuous pulse train and small permissible resistance change reduces the maximum handling capability.

The continuous pulse train maximum handling capacity of chip resistors has been determined experimentally. Measurements have shown that the handling capacity varies with the resistive value applied.
However, maximum peak pulse voltages as indicated in Fig.12, should not be exceeded.

Determination of pulse-load

The graphs in Figs 11 and 12 may be used to determine the maximum pulse-load for a resistor.

- For repetitive rectangular pulses:
  - $\frac{\hat{V}_i^2}{R}$ must be lower than the value of $\hat{P}_{max}$ given by the solid lines of Fig.11 for the applicable value of t_i and duty cycle t_p/t_i.
  - $\hat{V}_i$ must be lower than the value of $\hat{V}_{max}$ given in Fig.12 for the applicable value of t_i.
- For repetitive exponential pulses:
  - As for rectangular pulses, except that $t_i = 0.5\ \tau$.
- For single rectangular pulses:
  - $\frac{\hat{V}_i^2}{R}$ must be lower than the $\hat{P}_{max}$ given by the dashed line of Fig.11 for the applicable value of t_i.
  - $\hat{V}_i$ must be lower than the value of $\hat{V}_{max}$ given in Fig.12 for the applicable value of t_i.

Definition of symbols used in Figs 11**,** 12**,** 13 and 14

SYMBOL	DESCRIPTION
$\hat{P}$	applied peak pulse power
$\hat{P}_{max}$	maximum permissible peak pulse power (Fig.11)
$\hat{V}_i$	applied peak pulse voltage (Figs 13 and 14)
$\hat{V}_{max}$	maximum permissible peak pulse voltage (Fig.12)
R_{nom}	nominal resistance value
t_i	pulse duration (rectangular pulses)
t_p	pulse repetition time
τ	time constant (exponential pulses)
T_{amb}	ambient temperature
$T_{m(max)}$	maximum hot-spot temperature of the resistor

Examples

Determine the stability of a typical resistor for operation under the following pulse-load conditions.

CONTINUOUS PULSE TRAIN

A 100 Ω resistor is required to operate under the following conditions: V_i = 10 V; $t_i = 10^{-5}$ s; $t_p = 10^{-2}$ s.

Therefore:

$$\hat{P} = \frac{10^2}{100} = 1 \text{ W and } \frac{t_p}{t_i} = \frac{10^{-2}}{10^{-5}} = 1000$$

For $t_i = 10^{-5}$ s and $\frac{t_p}{t_i} = 1000$, Fig.11 gives $\hat{P}_{max}$ = 2 W and Fig.12 gives $\hat{V}_{max}$ = 400 V. As the operating conditions $\hat{P}$ = 1 W and $\hat{V}_i$ = 10 V are lower than these limiting values, this resistor may be safely used.

SINGLE PULSE

A 10 kΩ resistor is required to operate under the following conditions: $\hat{V}_i$ = 250 V; $t_i = 10^{-5}$ s.

Therefore:

$$\hat{P}_{max} = \frac{250^2}{10000} = 6.25 \text{ W}$$

The dashed curve of Fig.11 shows that at $t_i = 10^{-5}$ s, the permissible $\hat{P}_{max}$ = 10 W and Fig.12 shows a permissible $\hat{V}_{max}$ of 400 V, so this resistor may be used.

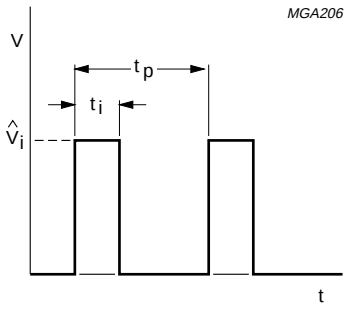


Fig.13 Rectangular pulses.

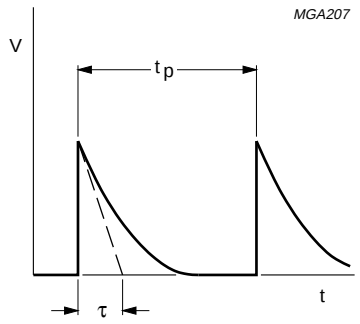
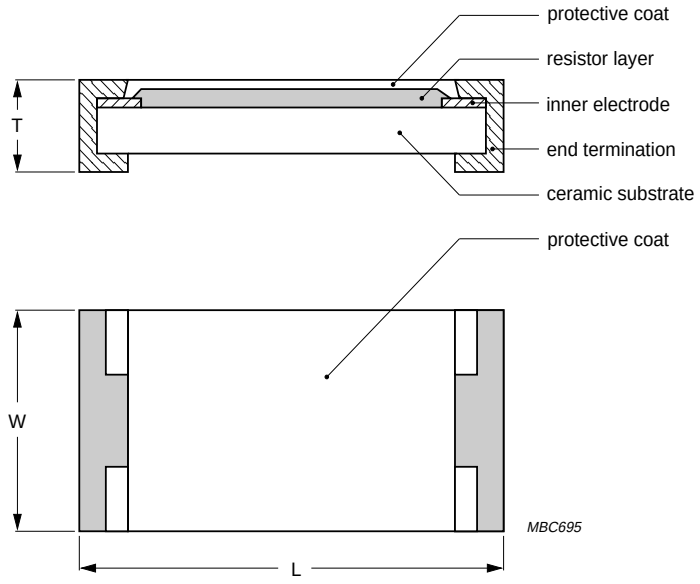


Fig.14 Exponential pulses.

MECHANICAL DATA

Outlines



For dimensions see Table 2.

Fig.15 Component outline.

Table 2 Chip resistor type; USA case size code; mass per 100 units and relevant physical dimensions; see Fig.15

TYPE	USA SIZE CODE	L (mm)	W (mm)	T (mm)	MASS (g)
RC0...	1206	3.2	1.6	0.6	1.0
RC1..	0805	2.0	1.25	0.6	0.55
RC2..	0603	1.6	0.8	0.45	0.4

Marking

Wherever possible chip resistors are provided with a **resistance code**; see Table 3. The resistance code includes the first two or three significant digits of the resistance value (in ohms) followed by the number of zeros to follow. Whether two or three significant values are represented depends on the tolerance: ±5% requires two digits; ±2% tolerance may be marked with two or three digits; ±2% tolerance may be marked with two or three digits; ±1% and lower requires three digits.

Table 3 Resistance value indication

INDICATOR	TOL. ≥ ±2%	TOL. ≤ ±1%
0	0.0 Ω; jumper	–
R[1]	1 to 91 Ω	1 to 976 Ω
1	100 to 910 Ω	1 to 9.76 kΩ
2	1 to 9.1 kΩ	10 to 97.6 kΩ
3	10 to 91 kΩ	100 to 976 kΩ
4	100 to 910 kΩ	1 MΩ
5	1 to 9.1 MΩ	–
6	10 MΩ	–

Note

1. R denotes the decimal point.

TESTS AND PROCEDURES

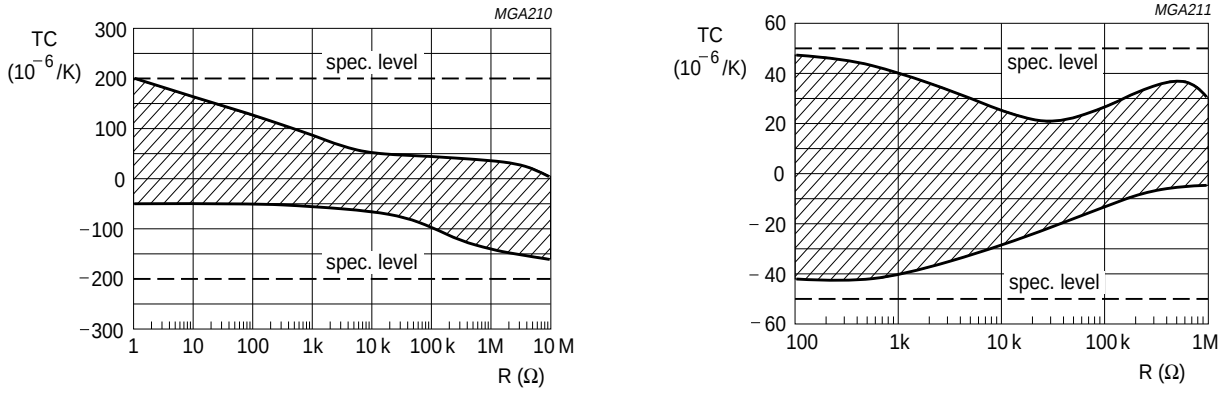
To guarantee zero defect production standards, Statistical Process Control is an essential part of our production processes. Furthermore, our production process is operating in accordance with *"ISO 9000"*.

Essentially all tests on resistors are carried out in accordance with the schedule of *"IEC publication 115-1"* in the specified climatic category and in accordance with IEC publication 68, *"Recommended basic climatic and mechanical robustness testing procedure for electronic components"*. In some instances deviations from the IEC recommendations are made.

Table 4 Test procedures

IEC 115-8 CLAUSE	IEC 68-2 TEST METHOD	TEST	PROCEDURE
4.17	20 (Ta)	soldering	unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C; flux 600
		solderability	16 hours steam or 16 hours at 155 °C; unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C; flux 600
4.18	20 (Tb)	resistance to soldering heat	10 s; 260 ±5 °C; flux 600
4.19	14 (Na)	rapid change of temperature	30 minutes at –55 °C and 30 minutes at upper category temperature; 5 cycles
4.22	6 (Fc)	vibration	frequency: 10 to 500 Hz; displacement 1.5 mm or acceleration 10 g; 3 directions; total 6 hours
4.20	29 (Eb)	bump	3 × 1500 bumps in 3 directions; 40 g
4.33		bending	resistors mounted on a 90 mm glass epoxy resin PCB, bending: 5 mm
4.24		humidity load (JIS)	1000 hours; +40 °C; 90 to 95% RH; loaded with P_n or 150 V; maximum 1.5 hours on and 0.5 hours off
4.23		climatic sequence:	
4.23.2	2 (Ba)	dry heat	16 hours; 125 °C
4.23.3	30 (D)	damp heat (accelerated) 1st cycle	24 hours; 55 °C; 95 to 100% RH
4.23.4	1 (Aa)	cold	2 hours; –55 °C
4.23.5	13 (M)	low air pressure	1 hour; 8.5 kPa; 15 to 35 °C
4.23.6	30 (D)	damp heat (accelerated) remaining cycles	5 days; 55 °C; 95 to 100% RH

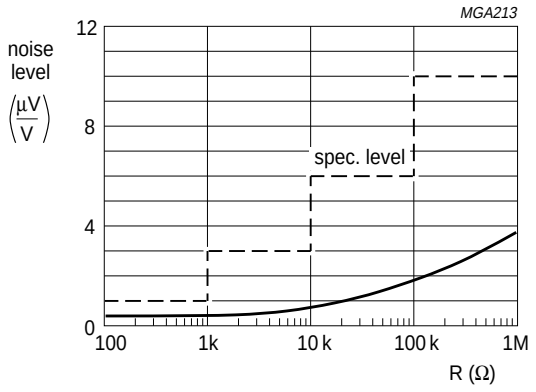
IEC 115-8 CLAUSE	IEC 68-2 TEST METHOD	TEST	PROCEDURE
4.24.2	3 (Ca)	damp heat (steady state) (IEC)	56 days; 40 °C; 90 to 95% RH; loaded with $0.01P_n$ (IEC steps: 0 to 100 V); dissipation ≤1 mW
4.25.1		endurance	1000 hours; 70 °C; nominal dissipation
4.6.1.1		insulation resistance	100 V (DC) after 1 minute
4.13		short time overload	room temperature; dissipation $6.25 \times P_n$; 5 s (voltage not more than $2 \times V_{max}$)
4.8.4.2		temperature coefficient	between –55 °C and +125 °C
4.12		noise	IEC publication 195 (measured with Quantech - equipment)
4.23.2	27 (Ba)	endurance at upper category temperature	1000 hours; 125 °C; no load
4.7		voltage proof on insulation	V_{max} (RMS) during 1 minute



a. RC-01.

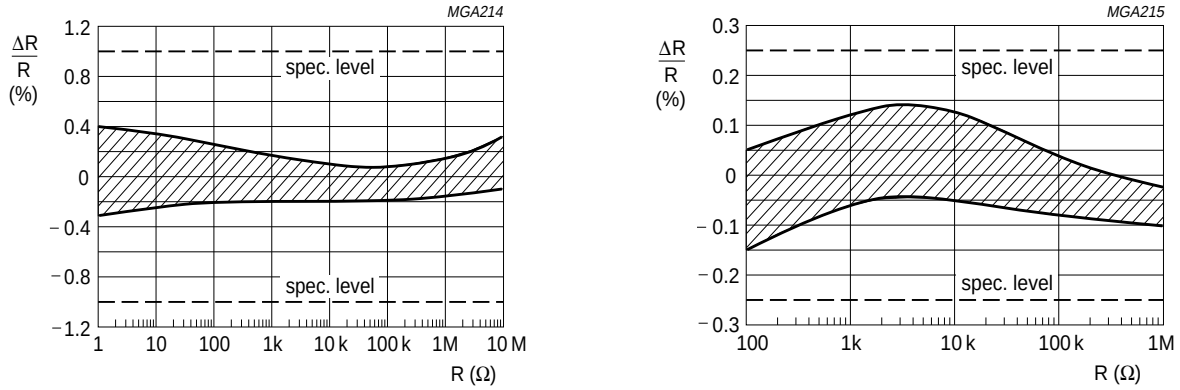
b. RC-02G.

Fig.16 Typical temperature coefficients between the lower and upper category temperatures.



RC-02G.

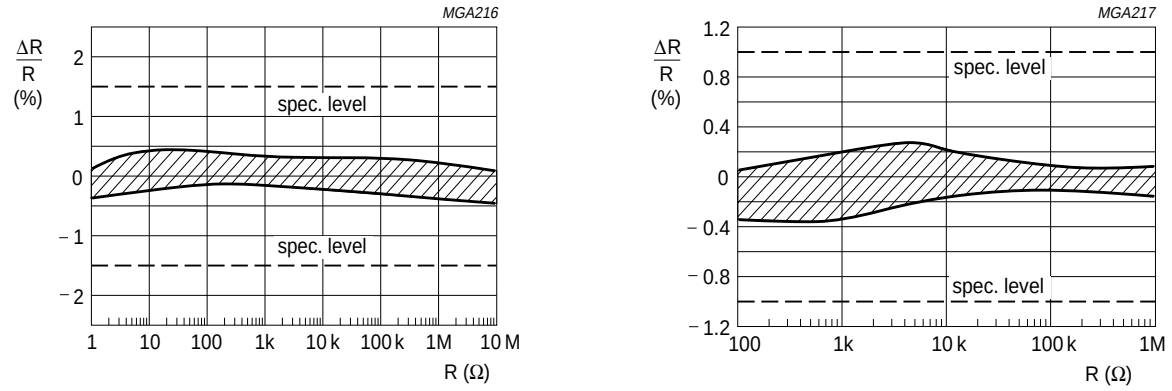
Fig.17 Typical noise level as a function of rated resistance measured using Quantech - equipment.



a. RC-01.

b. RC-02G.

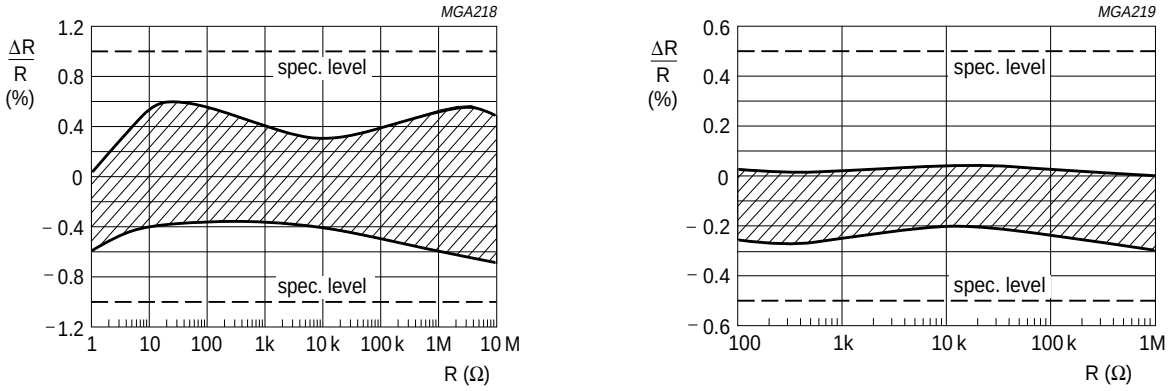
Fig.18 Typical percentage change in resistance after soldering for 10 seconds at 260 °C, completely immersed.



a. RC-01.

b. RC-02G.

Fig.19 Typical percentage change in resistance after 56 days at 40 °C and 90 to 95% relative humidity loaded with P_{nom}.



a. RC-01.

b. RC-02G.

Fig.20 Typical percentage change in resistance after 1000 hours loaded with P_{nom} at 70 °C ambient temperature.

MOUNTING

Mounting

Chip resistors are designed for handling by automatic chip placement systems.

The temperature rise in a resistor due to power dissipation, is determined by the laws of heat - conduction, convection and radiation. The maximum body temperature usually occurs in the middle of the resistor and is called the **hot-spot** temperature.

The hot-spot temperature depends on the ambient temperature and the dissipated power. This is described in the data sheets under the chapter heading “Functional description”.

The hot-spot temperature is important for mounting because the connections to the chip resistors will reach a temperature close to the hot-spot temperature. Heat conducted by the connections must not reach the melting point of the solder at the joints. Therefore a maximum solder joint temperature of 110 °C is advised.

The ambient temperature on large or very dense printed-circuit boards (PCBs) is influenced by the dissipated power. The ambient temperature will again influence the hot-spot temperature. Therefore, the packing density that is allowed on the PCB is influenced by the dissipated power.

Example of mounting effects

Assume that the maximum temperature of a PCB is 95 °C and the ambient temperature is 50 °C. In this case the maximum temperature rise that may be allowed is 45 °C. In the graph (see Fig.21), this point is found by drawing the line from point A (PCB = 95 °C) to point B (T_{amb} = 50 °C) and from here to the left axis.

To find the maximum packing density, this horizontal line is extended until it intersects with the curve, 0.125 W (point C). The maximum packing density, 19 units/50 × 50 mm^2 (point D), is found on the horizontal axis.

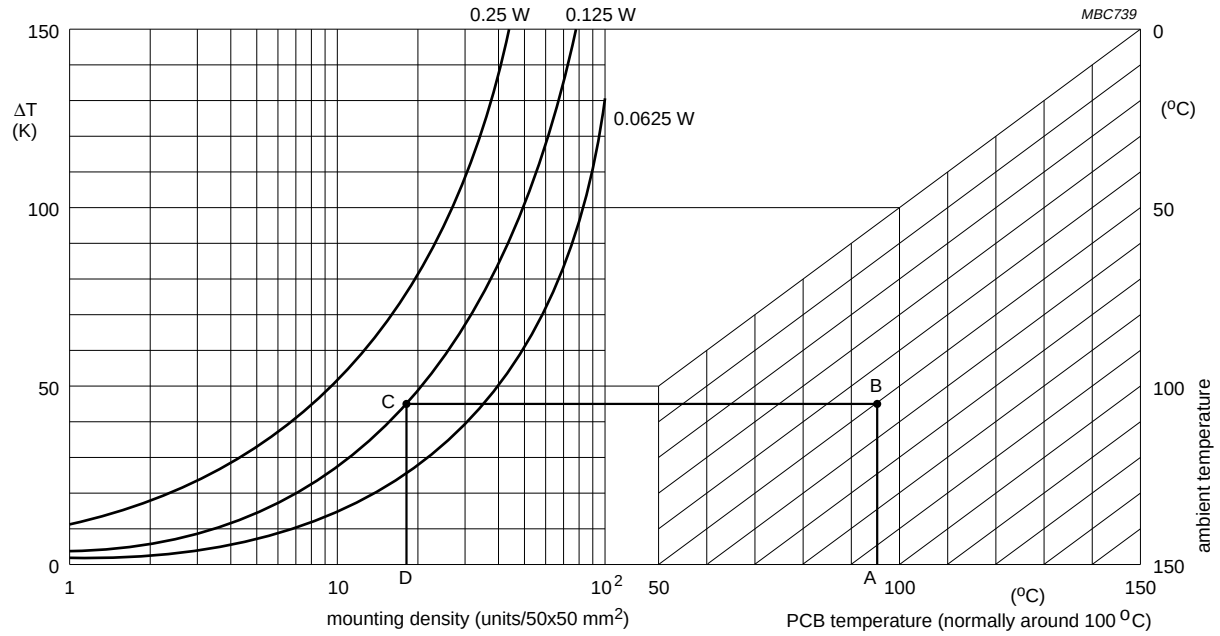


Fig.21 PCB temperature as a function of applied power, mounting density and ambient temperature.

Heat resistance (R_{th})

Heat resistance is the thermal resistance that prohibits the release of heat generated within the resistor to the surrounding environment. It is expressed in K/W and defines the surface temperature (T_{HS}) of the resistor in relation to the ambient temperature (T_{amb}) and the load (P) of the resistor, as follows:

$T_{HS} = T_{amb} + P \times R_{th}$

Due to their direct contact with the solder spot, chip resistors dissipate over 85% of their heat via conduction to the solder spot and hence to the PCB. Thus the PCB on which the chip resistor is mounted functions as a heat sink. Different PCBs have different heat conductance. Figure 22 shows the different values of heat resistance per material type. Substrates with a higher heat conductance give lower thermal resistance figures; substrates with a lower heat conductance give higher thermal resistance figures.

It should be noted that the temperature of the terminations of the chip resistor is virtually the same as the hot-spot temperature. Therefore the power that may be dissipated by the resistor is dependent on:

T_{amb} (which is also dependent on the packing density)

R_{th} of the PCB

maximum solder spot temperature (generally 110 °C).

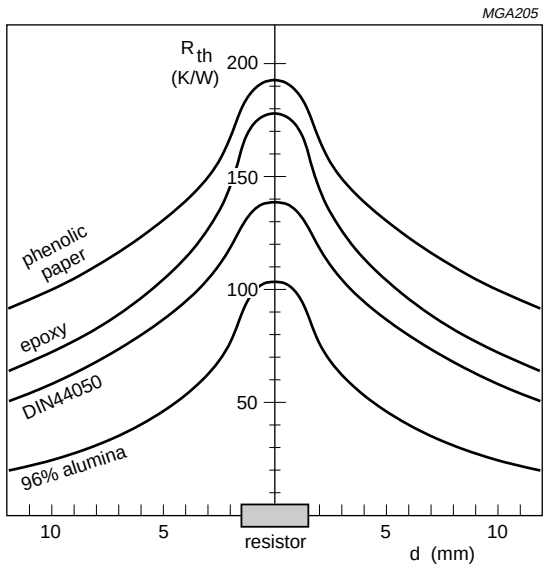
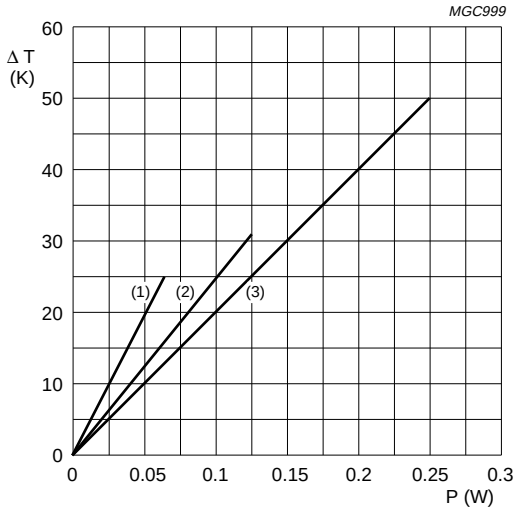


Fig.22 Heat resistance for 1206 sized resistors as a function of distance and material.



(1) For size 0603: R_{th} = 400.
(2) For size 0805: R_{th} = 250.
(3) For size 1206: R_{th} = 200.

Fig.23 Hot-spot temperature rise (ΔT) as a function of dissipated power.

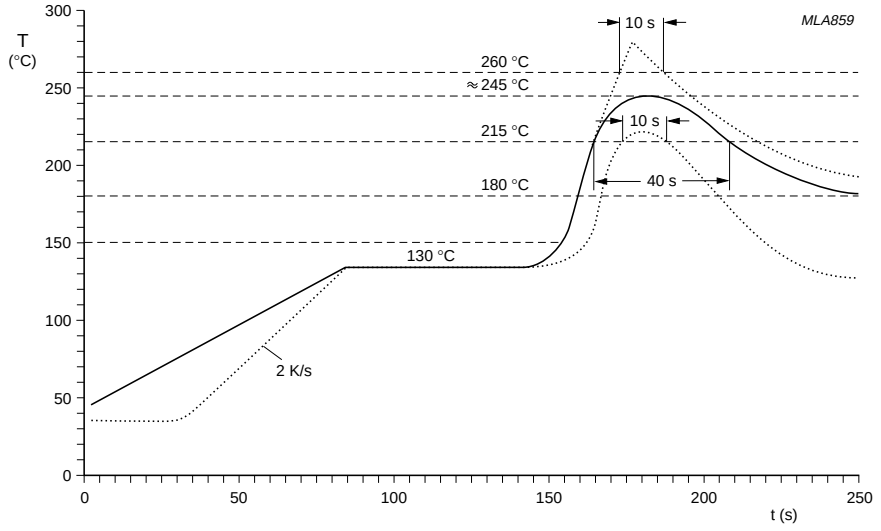
MOUNTING

Due to their rectangular shape and small tolerances on the dimensions, Surface Mounted Resistors are suitable for handling by automatic placement systems. Chip placement can be done on ceramic substrates and printed-circuit boards (PCBs). Electrical connection to the circuit is by wave, vapour phase or infrared soldering. The end terminations guarantee a reliable contact and the protective coating enables 'face down' mounting.

The robust construction of the device allows it to be completely immersed in a solder bath of 260 °C for one minute. Therefore, it is possible to mount Surface Mounted Resistors on one side of a PCB and other discrete components on the reverse (mixed PCBs).

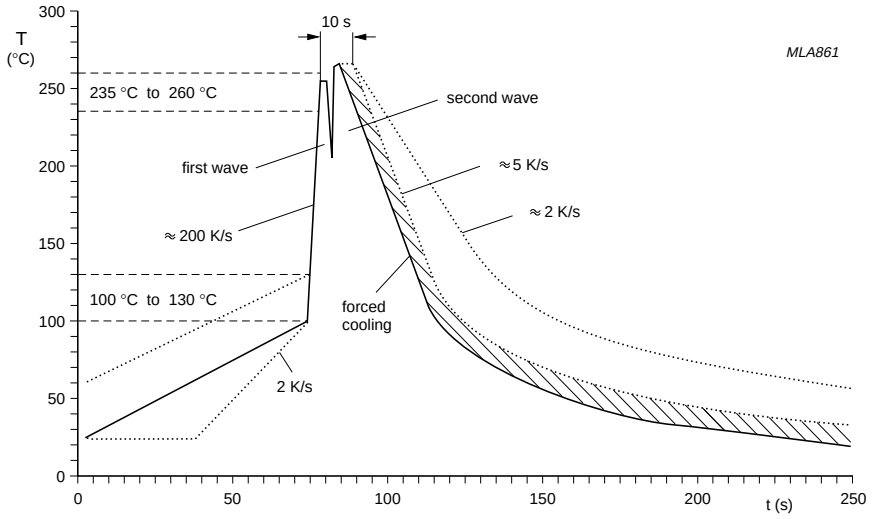
SOLDERING CONDITIONS

Surface Mounted Resistors are tested for solderability at 235 °C during 2 seconds. The test condition for no leaching is 260 °C for 60 seconds. Typical examples of soldering processes that provide reliable joints without any damage, are given in Figs 24, 25 and 26.



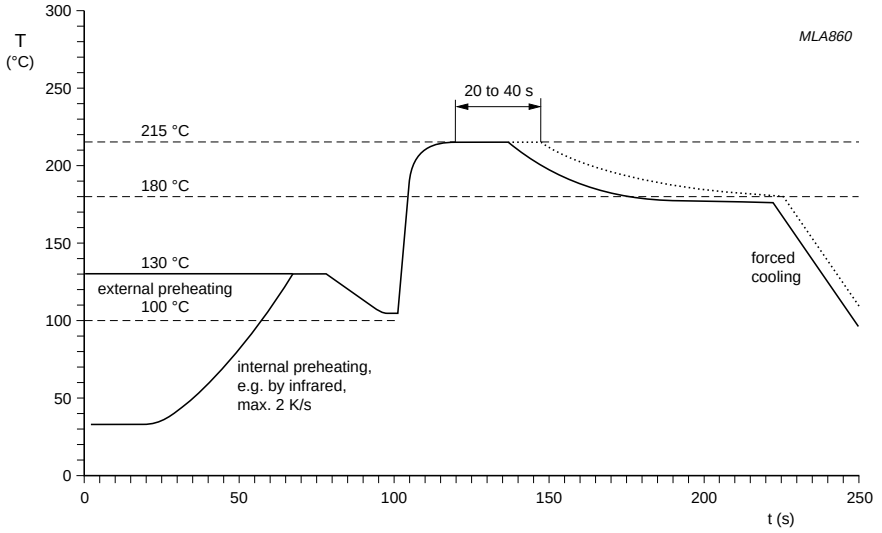
Typical values (solid line).
Process limits (dotted lines).

Fig.24 Infrared soldering.



Typical values (solid line).
Process limits (dotted lines).
The capacitors may be soldered twice in accordance with this method if desired.

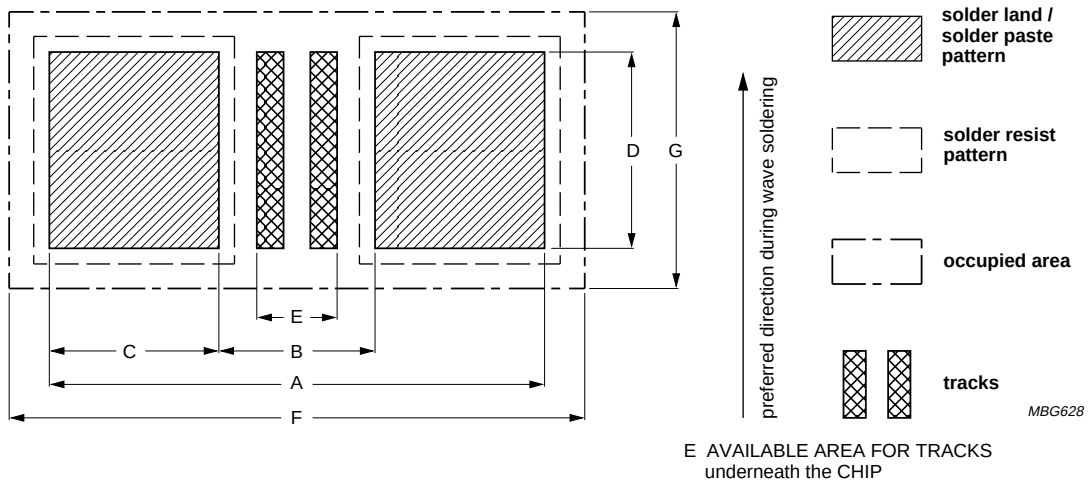
Fig.25 Double wave soldering.



Typical values (solid line).
Process limits (dotted line).

Fig.26 Vapour phase soldering.

FOOTPRINT DIMENSIONS



For dimensions see Tables 5 and 6.

Fig.27 Recommended dimensions of footprints.

Table 5 Reflow soldering; for dimensions see also Fig.27

SIZE CODE	FOOTPRINT DIMENSIONS (mm)							PROCESSING REMARKS	PLACEMENT ACCURACY (mm)
	A	B	C	D	E	F	G		
0603	2.1	0.7	0.7	0.9	0.26	2.5	1.5	IR or hot plate soldering	±0.15
0603	2.1	0.5	0.8	0.9	0.0	2.5	1.7		±0.25
0805	2.6	0.9	0.85	1.4	0.5	3.0	2.1		±0.25
1206	3.8	2.0	0.9	1.8	1.4	4.2	2.5		±0.25

Table 6 Wave soldering (no dummy tracks allowed for the high voltage series); for dimensions see also Fig.27

SIZE CODE	FOOTPRINT DIMENSIONS (mm)							PROPOSED NUMBER AND DIMENSIONS OF DUMMY TRACKS (mm)	PLACEMENT ACCURACY (mm)
	A	B	C	D	E	F	G		
0603	2.5	1.1	0.7	0.8	0.3	3.0	1.7	$1 \times (0.3 \times 0.8)$	±0.15
0603	2.7	0.9	0.9	0.8	0.15	3.2	1.9	$1 \times (0.15 \times 0.8)$	±0.25
0805	3.3	1.3	1.0	1.3	0.7	3.9	2.4	$1 \times (0.3 \times 1.3)$	±0.25
1206	4.5	2.5	1.0	1.7	1.25	5.0	2.8	$3 \times (0.25 \times 1.7)$	±0.25
1218	4.4	1.9	1.25	4.8	1.3	4.6	5.6	–	±0.25

PACKAGING

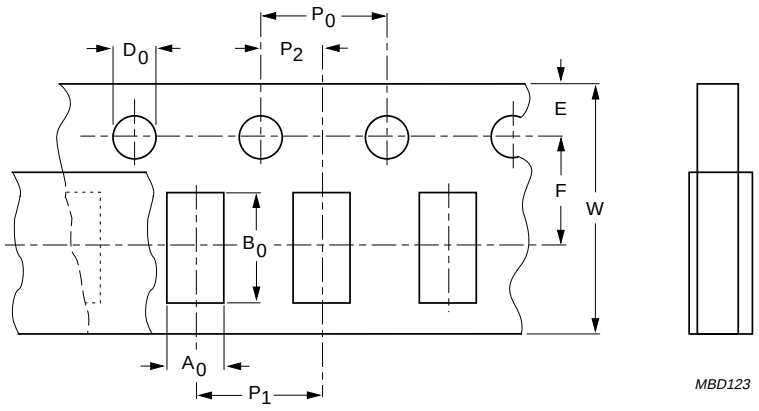
Tape and reel specifications

All tape and reel specifications are in accordance with the first edition of *"IEC 286-3"*, and amendments as proposed in *"IEC 40 (Secretariat) 570"*. Basic dimensions are given in Figs 28, 29, 31 and Tables 7, 8 and 10.

Peel-off force

Peel-off forces of both cardboard and blister tapes are in accordance with *"IEC 286-3"*; that is, 0.1 N to 0.7 N at a peel-off speed of 120 mm/minute and 0.2 N to 1.0 N at a peel-off speed of 300 mm/minute. For both methods, the peel-off angle should be between 165° and 180°.

Cardboard tape



Cumulative tolerance over 10 holes: ±0.2 mm.
Bottom fixing tape thickness: 50 ±10 µm.
Top fixing tape thickness: 50 ±10 µm.
For dimensions see Table 7.
Carrier tape thickness:
0.6 ±0.05 mm (0603)
0.75 ±0.05 mm (1206; 0805).

Fig.28 Cardboard tape.

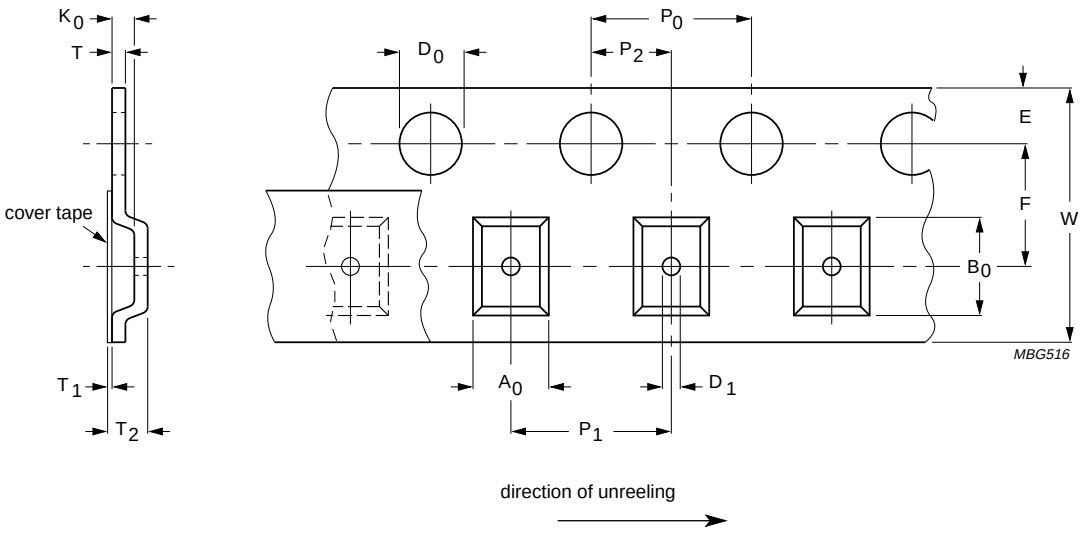
Table 7 Physical dimensions of cardboard tape for relevant chip size; see Fig.28

SYMBOL	PRODUCT SIZE CODE			TOLERANCE	UNIT
	06036	0805	1206		
A_0	1.0	1.5	1.85	+0.2/–0	mm
B_0	1.8	2.25	3.45	+0.2/–0	mm
W	8	8	8	±0.3	mm
E	1.75	1.75	1.75	±0.1	mm
F	3.5	3.5	3.5	±0.05	mm
D_0	1.5	1.5	1.5	+0.1/–0	mm
P_0	4	4	4	±0.1	mm
P_1	4	4	4	±0.1	mm
P_2	2	2	2	±0.05	mm

Embossed carrier tape

ENVIRONMENTAL CONSIDERATIONS

- Cover tape, carrier tape and reel do not contain the environmentally harmful PVC materials.
- Because the carrier tape is made of a homogeneous material (so called mono-plastic), it is ideally suited for recycling.
- Compared to other PVC-free materials Polycarbonate shows excellent stiffness and very little deformation as a function of temperature.



Cumulative pitch error: 0.2 mm over 10 pitches.
Cumulative tolerance over 10 holes: ±0.2 mm.
K_0: so chosen that the orientation of the component cannot change.
For W = 8 mm: T_2 = 2.5 mm max.
For W = 12 mm: T_2 = 4.5 mm max.
For dimensions see Table 8.

Fig.29 Embossed carrier tape.

Table 8 Physical dimensions of embossed carrier tape for relevant chip size; see Fig.29

SYMBOL	PRODUCT SIZE CODE			TOLERANCE	UNIT
	0805	1206	1218		
A_0 nominal clearance; note 1	0.30			–	mm
B_0 nominal clearance; note 1	0.20			–	mm
K_0 minimum clearance; note 1	0.10			–	mm
W	8.1	8.1	12	±0.2	mm
E	1.75	1.75	1.75	±0.1	mm
F	3.5	3.5	3.5	±0.05	mm
D_0	1.5	1.5	1.5	+0.1/–0.0	mm
D_1	≥1	≥1	≥1.5	+0.1/–0.0	mm
P_0; note 2	4	4	4	±0.1	mm
P_1	4	4	8	±0.1	mm
P_2	2	2	2	±0.05	mm

Notes

1. Possible product displacement in pocket.
2. P_0 pitch tolerance over any 10 pitches is ±0.2 mm.

Leader/trailer tape specification

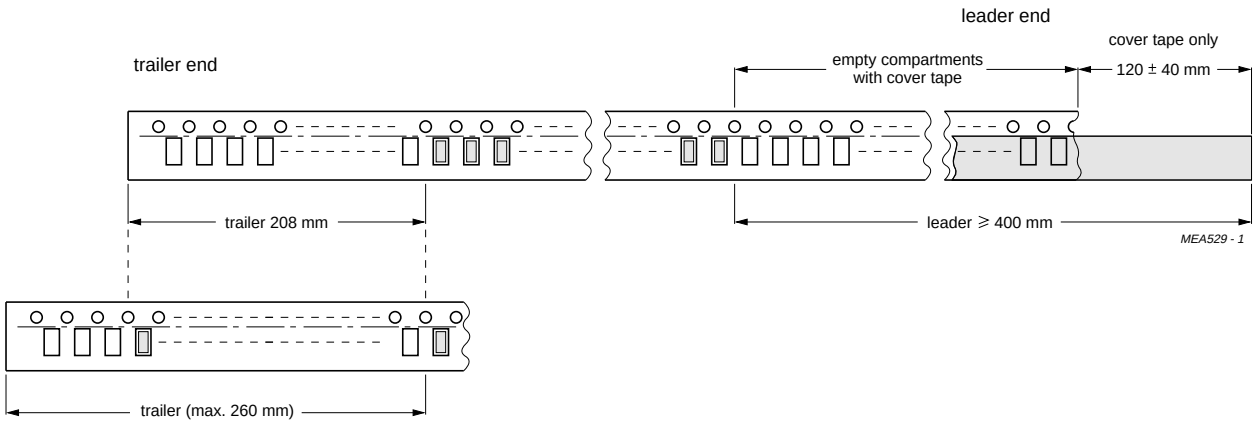
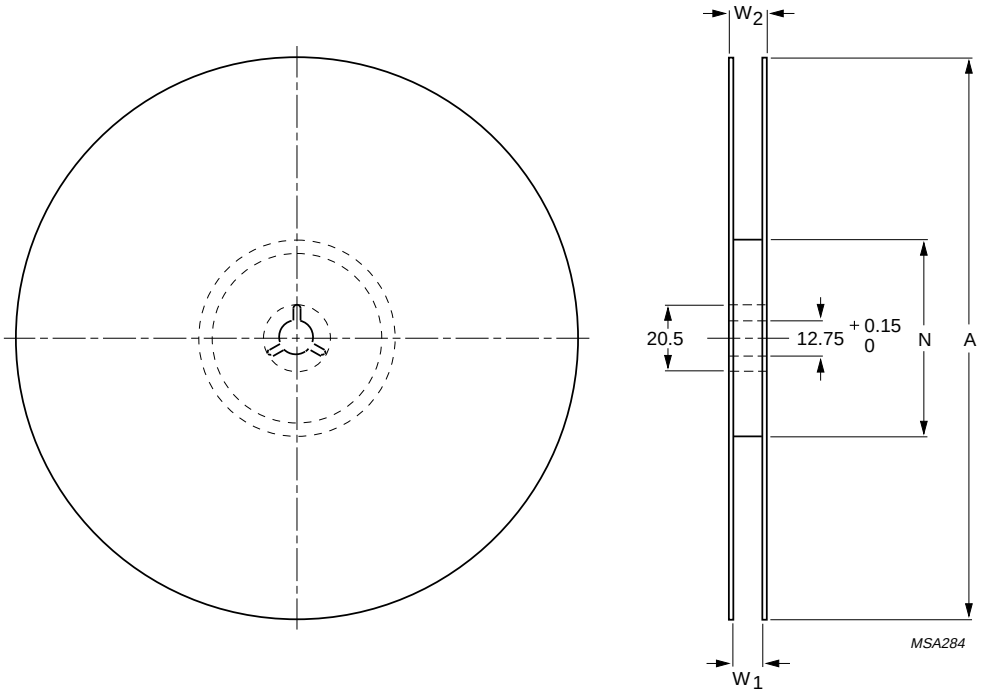


Fig.30 Leader/trailer tape.

Table 9 Leader/trailer tape data

DESCRIPTION	VALUE
Minimum length of empty compartments at leader end	≥400 mm of which a minimum 240 mm of empty compartments are covered with cover tape and 120 ±40 mm cover tape only.
Minimum length of empty compartments at trailer end	208 mm or 260 mm If the length is 260 mm an extra product is placed at 208 mm to mark this position.

REEL SPECIFICATIONS



Dimensions in mm.
For dimensions see Table 10.

Fig.31 Reel.

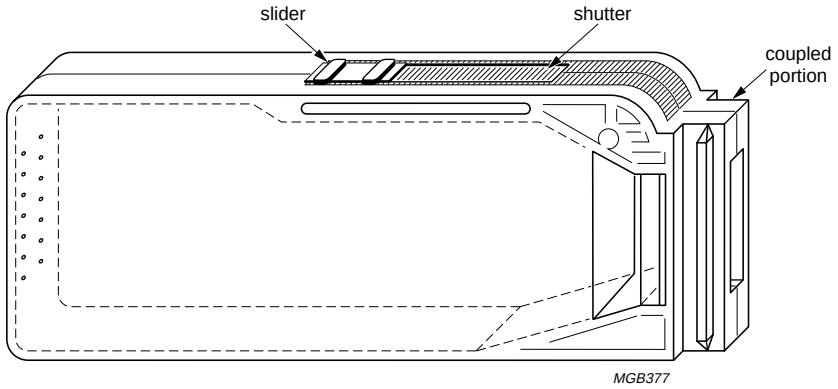
Table 10 Reel dimensions; see Fig.31

PRODUCT SIZE CODE	UNITS PER REEL	TAPE WIDTH (mm)	A (mm)	N (mm)	W_1 (mm)	W_2 MAX. (mm)
0603	10000	8	250	62 ±1.5	8.4 +1.5/–0.0	14.4
1206; 0805	5000		180			
1218	1000	12	180		12.4 +2/–0.0	18.4
	5000		260			

BULK CASE SPECIFICATION

Features and benefits:

- Reduced costs
  - Storage
  - Transport
  - Machine handling
  - Packaging.



For dimensions see Table 11.

Fig.32 Bulk case outlines.

Table 11 Bulk case dimensions; see Fig.32

LENGTH (mm)	WIDTH (mm)	THICKNESS (mm)
110	35	12

Table 12 Product size versus packaged quantity

PRODUCT SIZE CODE	UNITS PER CASE
0603	25000
0805	10000