SERVICE MANUAL
PV400S

PORTABLE AUDIO/VIDEO PLAYER PV400S

www.bbk.ru

CONTENTS

PV400S Project Structure Diagram

Briefness introduce main part of system ：

Pickup：KSM-1000BBC CD-deck compatible with CD, CD-R, Can be playing 12 cm & 8cm Discs.

RF AMP：The CXA2550N is 3-Beam Head Amp IC of SONY, Compatible with CD, CD-R.

Driver：The FAN8038 is 4CH H bridge driver and DC-DC converter control circuit, battery charge control circuit on a chip.
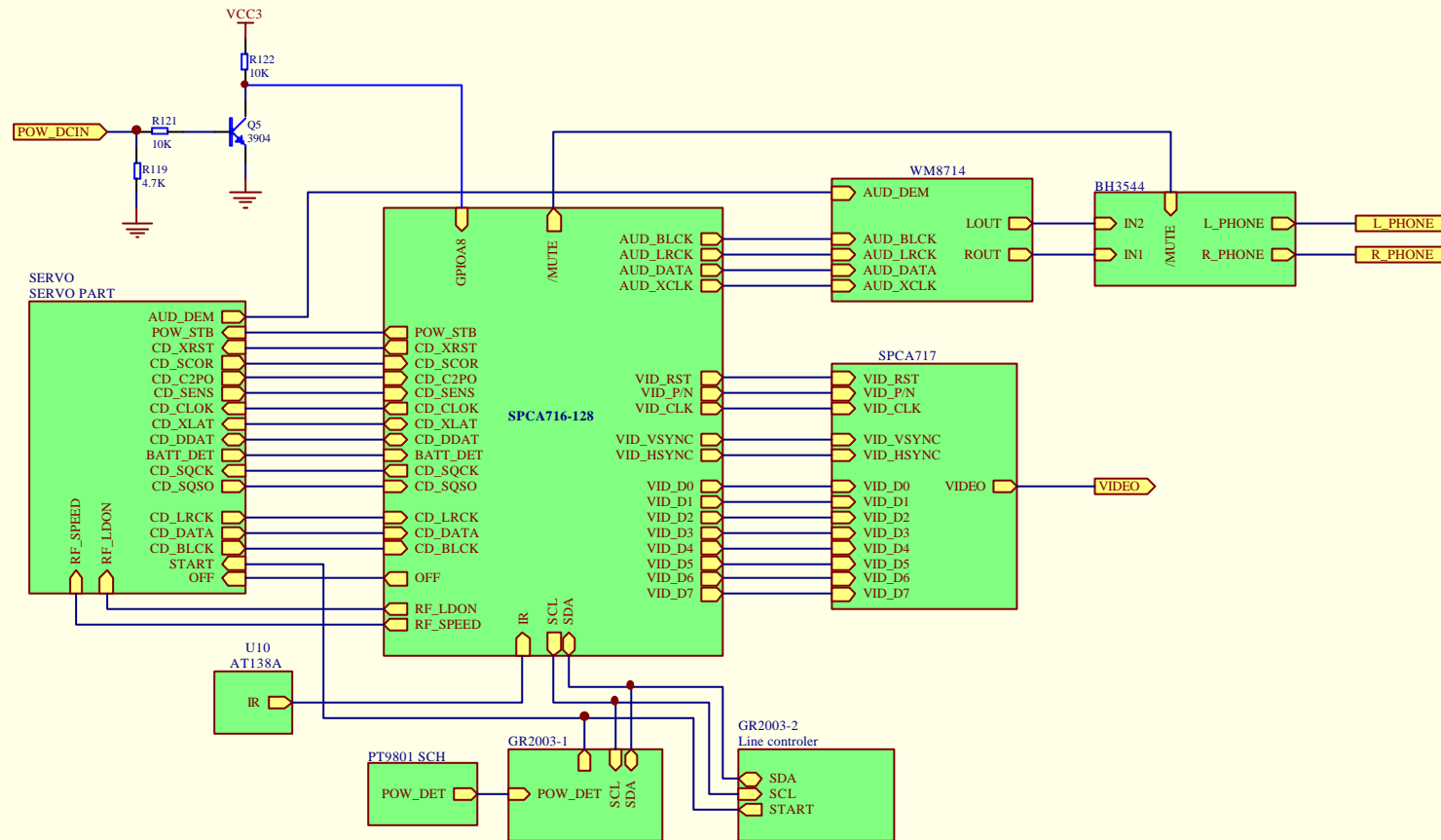
DSP：The CXD3068Q is a digital signal processor LSI for CD player, this LSI incorporates a digital servo.

MPEG：The SPCA716A A /V decoder is a single-chip VCD decoder, this LSI incorporates a MCU.

TV ENCODER：The SPCA717A is a single-chip VCD encoder.

D/A：The WM8714 is a digital to analog converter.

Power AMP：The BH3544 is audio power AMP, so that to driver headphone.

1

VCC3

R122
10K

POW_DCIN

R121
10K

Q5
3904

R119
4.7K

WM8714

AUD_DEM

AUD_BLCK
AUD_LRCK
AUD_DATA
AUD_XCLK

LOUT

ROUT

BH3544

IN2

IN1

/MUTE

L_PHONE

R_PHONE

L_PHONE

R_PHONE

GPIOA8

/MUTE

SPCA716-128

SERVO
SERVO PART

AUD_DEM
POW_STB
CD_XRST
CD_SCOR
CD_C2PO
CD_SENS
CD_CLOK
CD_XLAT
CD_DDAT
BATT_DET
CD_SQCK
CD_SQSO

CD_LRCK
CD_DATA
CD_BLCK
START
OFF

RF_SPEED
RF_LDON

POW_STB
CD_XRST
CD_SCOR
CD_C2PO
CD_SENS
CD_CLOK
CD_XLAT
CD_DDAT
BATT_DET
CD_SQCK
CD_SQSO

CD_LRCK
CD_DATA
CD_BLCK

OFF

RF_LDON
RF_SPEED

AUD_BLCK
AUD_LRCK
AUD_DATA
AUD_XCLK

VID_RST
VID_P/N
VID_CLK

VID_VSYNC
VID_HSYNC

VID_D0
VID_D1
VID_D2
VID_D3
VID_D4
VID_D5
VID_D6
VID_D7

SPCA717

VID_RST
VID_P/N
VID_CLK

VID_VSYNC
VID_HSYNC

VID_D0
VID_D1
VID_D2
VID_D3
VID_D4
VID_D5
VID_D6
VID_D7

VIDEO

VIDEO

IR

SCL
SDA

U10
AT138A

IR

PT9801 SCH

POW_DET

GR2003-1

POW_DET

SCL
SDA

GR2003-2
Line controler

SDA
SCL
START

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TECHNICAL DATA

MODEL : **KSM1000BBC**

Sony reserves the right to change specification of products and discontinue products without notice.

SONY CORPORATION
OPTICAL DEVICE DIVISION

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Scope of Document

This document describes the specification of drive unit KSM1000BBC, for use in compact disc player. This model is not for professional use.

The provisions of this document may be altered upon agreement between both parties.

If any disagreement should arise, these two parties shall meet in good faith to resolve the problem.

Within the range of these specifications, parts are subject to change without notice for technical improvement.

Please be sure to observe the following each time you deliver your finished and /or semi-finished products containing the device(s). Otherwise, SONY may not be able to assume the responsibility for things to happen.

Always use the device(s) within conditions given in the specifications.

Never given additional process to the device(s).

Make sure that a finished product containing SONY device(s) is in compliance with the rules and regulations for spurious radiation.

Measure leak laser output from a finished product containing the device(s) and make sure that the finished product is in compliance with applicable requirements.

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General Specifications

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2-1. Optical Specifications

Objective lens

Effective focal length (f)	3.85 mm
Numerical aperture (NA)	0.45
Working distance (WD)	1.8 mm

Semiconductor laser

Laser wavelength( )　　775　815 mm

Servo error detection methods

Focus error	SSD method
Tracking error	3-SPOT method

2-2. Mechanical Specifications

Dimensions　　　Figure 2

Mass　　　　35g　　　Standard value

Direction of objective lens movement

Figure 1.　　　see Figure 1

( )

Focus Direction

A positive voltage applied to pin (FCS) of the flex moves
the objective lens toward the disc.

( )

Tracking Direction

A positive voltage applied to pin (TRK) of the flex moves
the objective lens toward the center of the disc.

Range of objective lens movement

± 0.5 mm

Focus Direction The disc equal to surfacewave ± 0.5 mm should be able to play back.

± 0.5 mm

Tracking Direction　　or more

Specified at the datum of center position and the amount of
beam movement on the disc.

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Slide direction

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A positive voltage applied to pin   of sled motor moves the objective lens toward
the outer of the disc.

Pick-up movable distance

Mechanical center position	24 mm
Mechanical the most periphery position	58 mm

Length between the center of turntable and objective lens

Direction of turntable movement

A positive voltage applied to pin   of spindle motor rotates the turntable clockwise.

2-3.   Electrical Specifications of Pick-up

Item	Specifications
Power supply for LD	Single power supply
PD signal out put method	Voltage out put

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Evaluation Conditions

3-1.   Position

The negative Z axis is defined as the direction of gravity as shown in Figure 1.

3-2.   Environment

Temperature	22 ± 2
Relative Humidity	50 ± 5 %RH

If no errors occur in evaluation, the following range of conditions is acceptable.

Temperature	15	35
Relative Humidity	45	85 %RH

3-3.   Equipment

		Standard cabinet for measurement
(Figure 4)		APC circuit
	(Figure 5)	Standard measurement circuit
		Jitter meter
(	KJM-6235SA)	(KJM-6235SA, KIKUSUI ELE.CO.)
		Digital multimeter
		Servo analyzer
		Oscilloscope

3-4.   Disc

GLD-CR11
Glass disc manufactured by SONY : GLD-CR11

3-5.   Voltage

PDIC	$V_{CC} = 3 \pm 0.1$ V	
Pick-up PDIC	$V_C = 1/2 \, V_{CC} \pm 0.1$ V	

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Characteristics Specifications

4-1.　　　　　　　　Absolute Maximum Rating

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Actuator

Item		Standard value	Remarks
Coil current	Focus	150 mA RMS	150mA Focus　Tracking total current must be less than 150mA RMS
	Tracking		

Laser diode

Item	Standard value	Remarks
Laser diode inverse voltage	2 V	
Monitor pin photo diode inverse voltage	15 V	

Item	Standard value	Remarks
Supply Voltage	6 V	

／　　　　Spindle/Sled motor

Item		Standard value	Remarks
Allowable voltage	Spindle	3 V	
	Sled	3 V	

4-2.　　　　　　　　Operating Voltage Range

Item	Standard value	Remarks
(Vcc) Operating supply voltage(Vcc)	2.7　5.5 V	
(Vc) Neutral point voltage(Vc)	1.3　(Vcc　1.3) V	

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4-3. Performance Specifications

4-3-1. Optical Pick-up

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Actuator

*

Temperature deviation from room temperature and humidity measurement.
(* : Deviation percentage)

Item		Standard value — Room temperature and humidity	Temperature Deviation −5	Temperature Deviation +55	Remarks
ocus	DC resistance	6 ± 1	———		
	Sensitivity	1.5 $^{0.65}_{0.45}$ mm/V	* within ± 35%	* within ± 35%	Specified at 5Hz
	(fo) Resonant frequency	46 ± 7 Hz	within $^{+7}_{-2}$ Hz	within $^{2}_{-6}$ Hz	Specified at maximum Q-value
	Q-value	12.5 ± 6 dB	within ± 8dB	within ± 7dB	Q-value=Gain(fo)-Gain(5Hz)
Tracking	DC resistance	6.3 ± 1	———		
	Sensitivity 1)	0.48 $^{0.22}_{0.15}$ mm/V	* within ± 35%	* within ± 35%	Specified at 5Hz
	(fo) Resonant frequency	46 ± 8 Hz	within $^{+8}_{-2}$ Hz	within $^{+2}_{-6}$ Hz	Specified at maximum Q-value
	Q-value	14.5 ± 6 dB	within ± 8dB	within ± 7dB	Q-value=Gain(fo)-Gain(5Hz)

1)
Specified at beam spot on the disc.
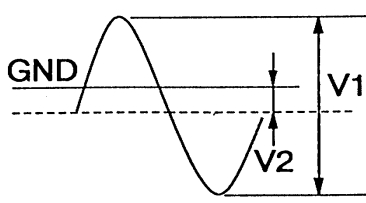
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Optics

Temperature deviation from room temperature and humidity measurement.
(* : Deviation percentage ** : Actually measured value)

RF signal
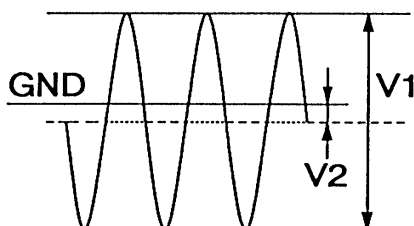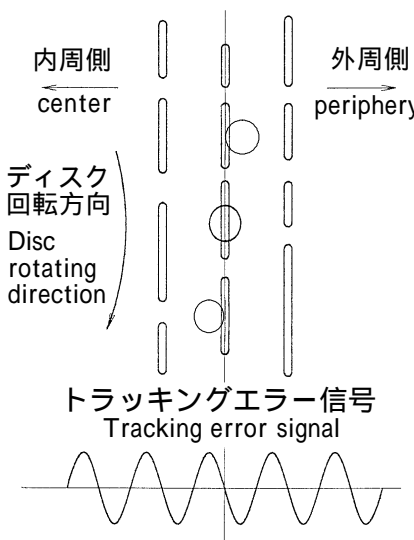
Item	Standard value	Temperature Deviation		Remarks
	Room temperature and humidity	- 5	+ 55	
RF RF signal amplitude	1.0 ± 0.2 Vp-p	* within ± 20%	* within ± 20%	APC temperature characteristics excluded
Jitter	26ns RMS or less	** 34ns RMS or less	** 32.5ns RMS or less	
RF RF signal offset voltage	within 0± 0.25V	————	————	At LD on.

Focus error signal

Item	Standard value	Temperature Deviation		Remarks
	Room temperature and humidity	- 5	+ 55	
Focus error signal amplitude	12± 5 Vp-p	* within ± 20%	* within ± 20%	P P 7μm Focus error
Defocus	within 0± 1.2μm	within ± 1μm	within ± 1μm	Defocus $\dfrac{V_2 - F.E._{offset}}{V_1} \times 7\mu m$ V_1 : Focus error signal amplitude V_2 : Focus bias at minimum jitter F.E.$_{offset}$: ON, DC Focus error DC offset at laser on and no reflection from the disc. Center of Focus error signal amplitude Defocus polarity When objective lens moves toward the disc and able to get minimum jitter,it is defined as plus, otherwise, it is defined as minus.
Focus error signal offset voltage	within 0± 2.3V	————	————	At LD on.
Polarity	F.E. The focus error signal changes from minus to plus the objective lens approaches the disc.			

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Tracking error signal

| Item | Standard value | Temperature Deviation | | Remarks |
	Room temperature and humidity	- 5	+ 55	
Tracking error signal amplitude	14.5± 7.5Vp-p	* within ± 30%	* within ± 30%	
EF EF balance	within 0± 30%	** within 0± 35%	** within 0± 35%	$\frac{V_2}{V_1} \times 100\%$ TPP balance GND ... V1 ... V2 The center of tracking error signal
E-F E-F phase difference	within ± 60°	** within ± 90°	** within ± 90°	
Polarity	When the spot is off track, the direction toward the center of the disc is defined as plus and the periphery of the disc is defined as minus.			center ... periphery Disc rotating direction Tracking error signal

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4-3-2.   Turntable unit

Item	Standard value	Remarks
Height of turntable	6.1± 0.2 mm	From insulator fixing surface
Surface vibrations of turntable	0.07 mm or less	
Maximum load of turntable	98 N or more	

4-3-3.   Sled mechanism

Item	Standard value Room temperature and humidity	Temperature Deviation - 5	+ 55	Remarks
Minimum starting voltage	1.0 V or less	1.2 V or less	1.2 V or less	
Full stroke time	2.3 s or less	3.0 s or less	3.0 s or less	1.5V( ) Applied voltage 1.5V (one way)
Current consumption	160mA or less	210mA or less	210mA or less	1.5V Applied voltage 1.5V
Make position of limit switch	Make should be completed before pick-up operation reaches mechanically innermost position.			

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Reliability Standard

5-1.   Reliability Standard

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Operating Temperature

Temperature   - 5   55

The operating characteristics at - 5   and 55   are expressed as deviations from standard values as shown in the performance specifications.
Leave the pick- up in the idle state within the above temperature range for four hours.   Do not let condensation to form on the mechanism

Storage Temperature

Temperature   - 30   60

Leave the pick- up at temperatures in the above range for 24 hours and then at room temperature for over 16 hours. After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications.   Do not let condensation to form on the mechanism

Storage in hot and humid conditions

Temperature   60
Humidity   90

Leave the pick- up at temperatures in the above range for 48 hours and then at room temperature for over 16 hours. After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications.   Do not let condensation to form on the mechanism

Vibration

$23.6 m/s^2$ 2.4G , 7   30Hz
Conditions   linear sweep, three directions

Subject the drive unit to above vibrations under the above conditions for 15 minutes in each direction(time for return sweep:5 minutes).   After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications.

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Impact

2,940m/s² 300G 1.6mSec, ± ± ± directions

Conditions

Subject the drive unit to above impact in each direction.   After the test, the deviation
of characteristics from the standard values must be within the tolerance specified in
the reliability specifications.

Service life of laser diode

,   .

Percent defective : 0.1% max after 3,000 hours operation at 25
(excluding damage due to electrostatic discharge)

Service life of spindle motor

,

The current consumption of spindle motor must be less than initial value plus 30%
after 1,000 hours of playback.

Service life of Sled motor

,

The current consumption of sled motor must be less than initial value plus 30%
after 10,000 cycles.
(1cycle : innermost track   outermost track   innermost track)

Service life of limit switch

,
The contact resistance must be less than 500m   after 10,000 cycles.
(1cycle : innermost track   outermost track   innermost track)

Pick-up slide operation

,

The pick-up should operate perfectly after 10,000 cycles.
(1cycle : innermost track   outermost track   innermost track)

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5-2.　　　　　　　　　Reliability Specifications

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Deviations after evaluation tests under the conditions specified on reliability
test except operating temperature test.(　：Actually measured value)

| Actuator |

Item		Standard value	
Focus	Sensitivity	± 25 %	within ± 25 %
	(fo) Resonant frequency	± 6 Hz	within ± 6 Hz
	Q-value	± 6 dB	within ± 6 dB
Tracking	Sensitivity	± 25 %	within ± 25 %
	(fo) Resonant frequency	± 7 Hz	within ± 7 Hz
	Q-value	± 6 dB	within ± 6 dB

| Optics |

Item			Standard value	
RF signal		RF signal Amplitude	± 20 %	within ± 20 %
		Jitter	34 ns RMS	34 ns RMS or less
Focus signal		Focus error signal amplitude	± 20 %	within ± 20 %
		Defocus	± 1 μm	within ± 1 μm
Traverse signal		Tracing error signal amplitude	± 30 %	within ± 30 %
	EF	EF balance	0± 35 %	within 0± 35 %
	EF	EF phase difference	0± 90	within 0± 90

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| Sled mechanism | | |

Item	Standard value	Remarks
Minimum starting voltage	1.2 V or less	
Sled time	3 sec or less	1.5 V Applied voltage 1.5V
Current consumption	210 mA or less	

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Markings

6-1.   Stamp

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| | | | | | No. | Alphabet |
| BBC | Day | Month | Last digit of year | Quality control No. | or Number |

Lot No.

10, 11, 12   X, Y, Z
X,Y and Z signify October, November and December
respectively.

The last alphabet is for management
purposes in the factory.   Use up to three characters.

6-2   Position of label

Fig. 1
Refer to Fig. 1. Description of components.

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Package Specifications

Set into protection sheet.

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MD cover

MD case

Protection sheet
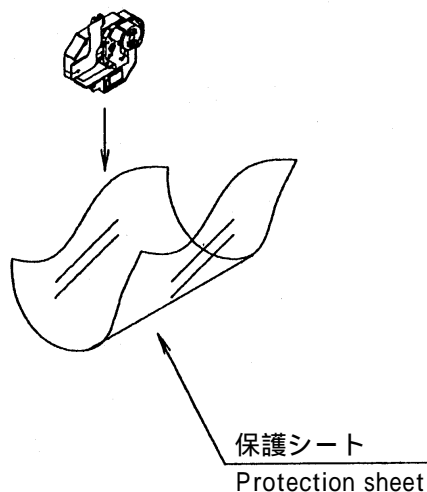
(50× 2)
Set into MD case.   50 pcs× 2 lines (Total 100 pcs)

Master carton

MD cover

MD case

PP tape

0 mm 以上
50 mm or more

Shipping label

19
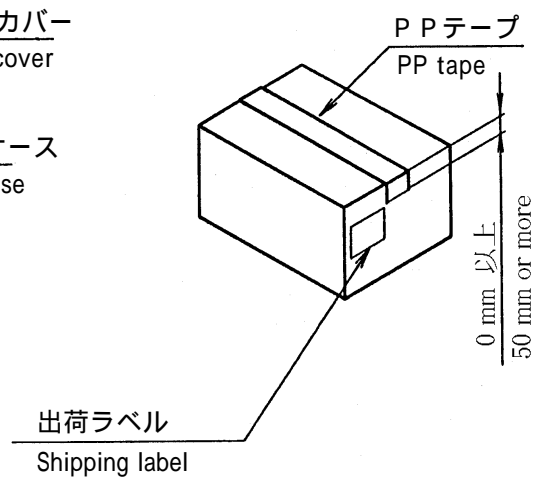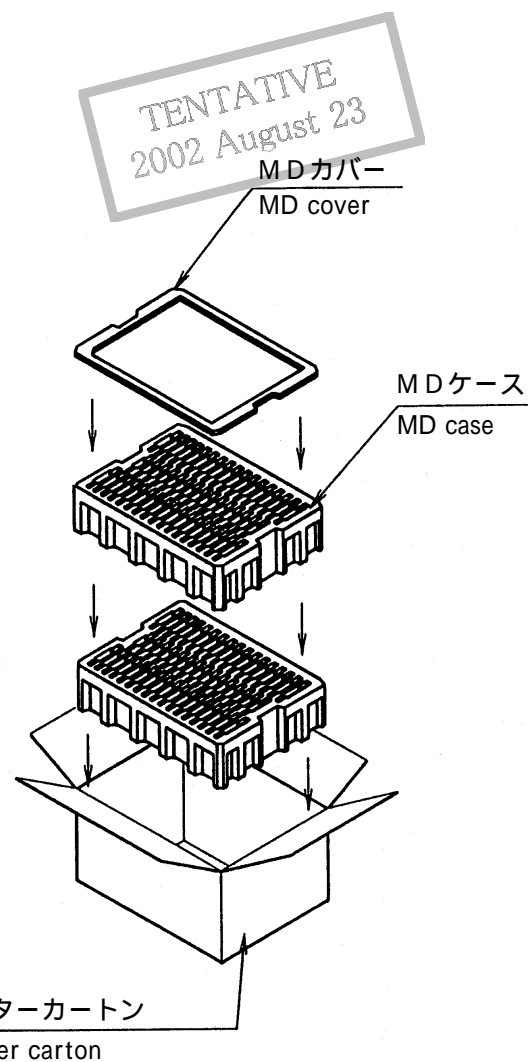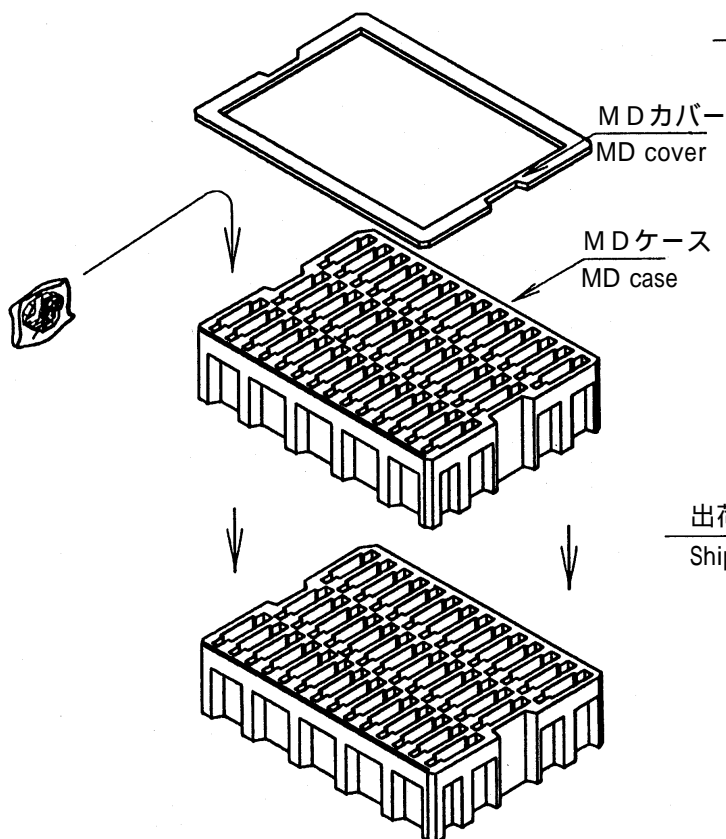
Attachment

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Figure 1.   Description of components
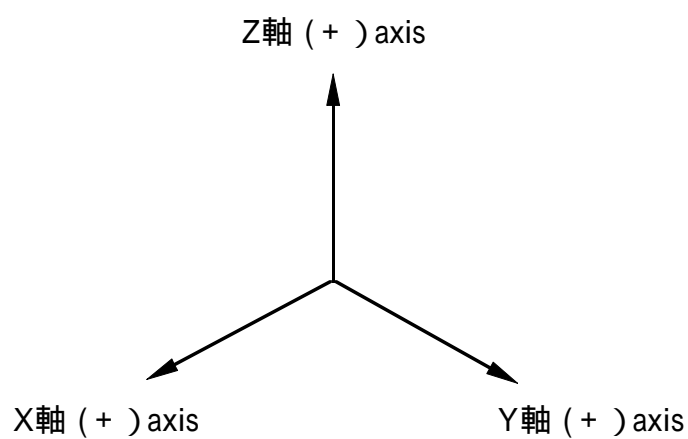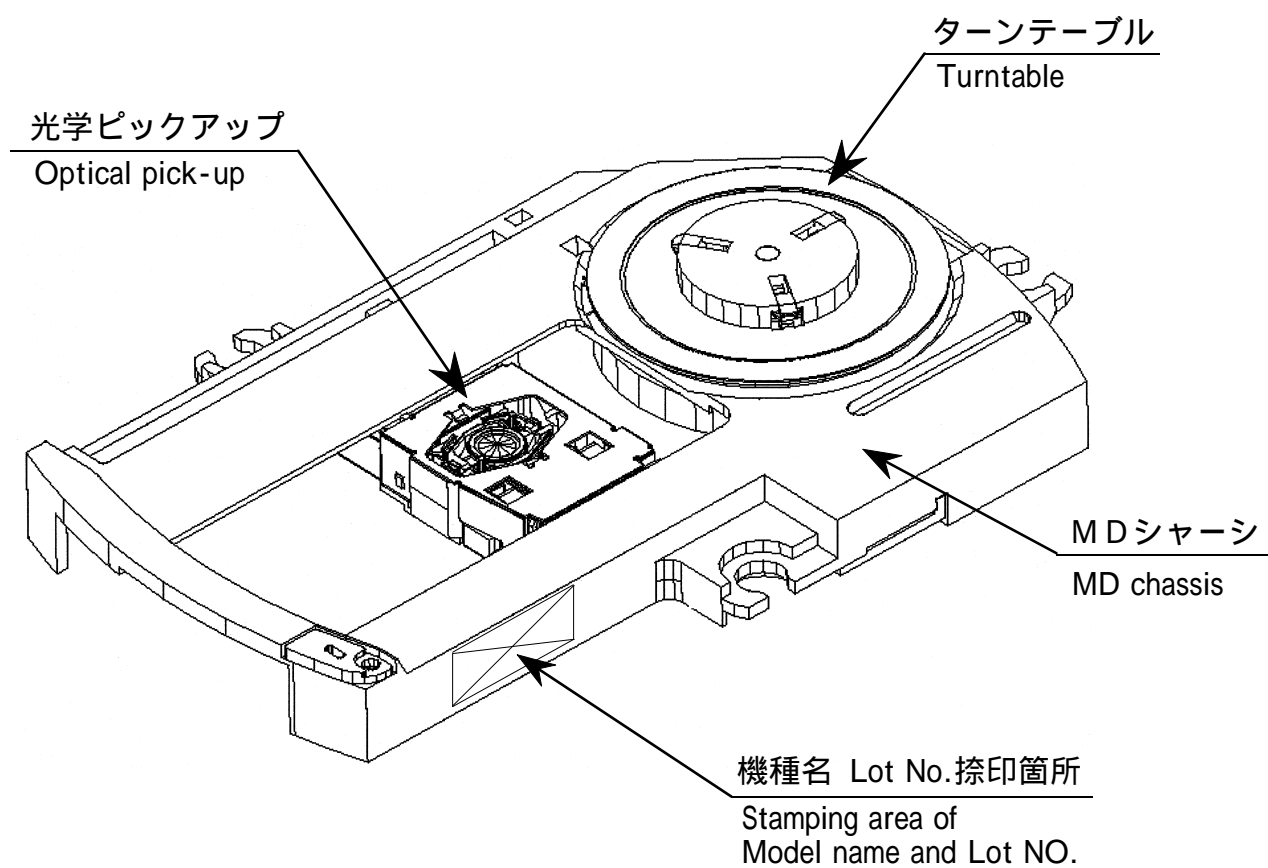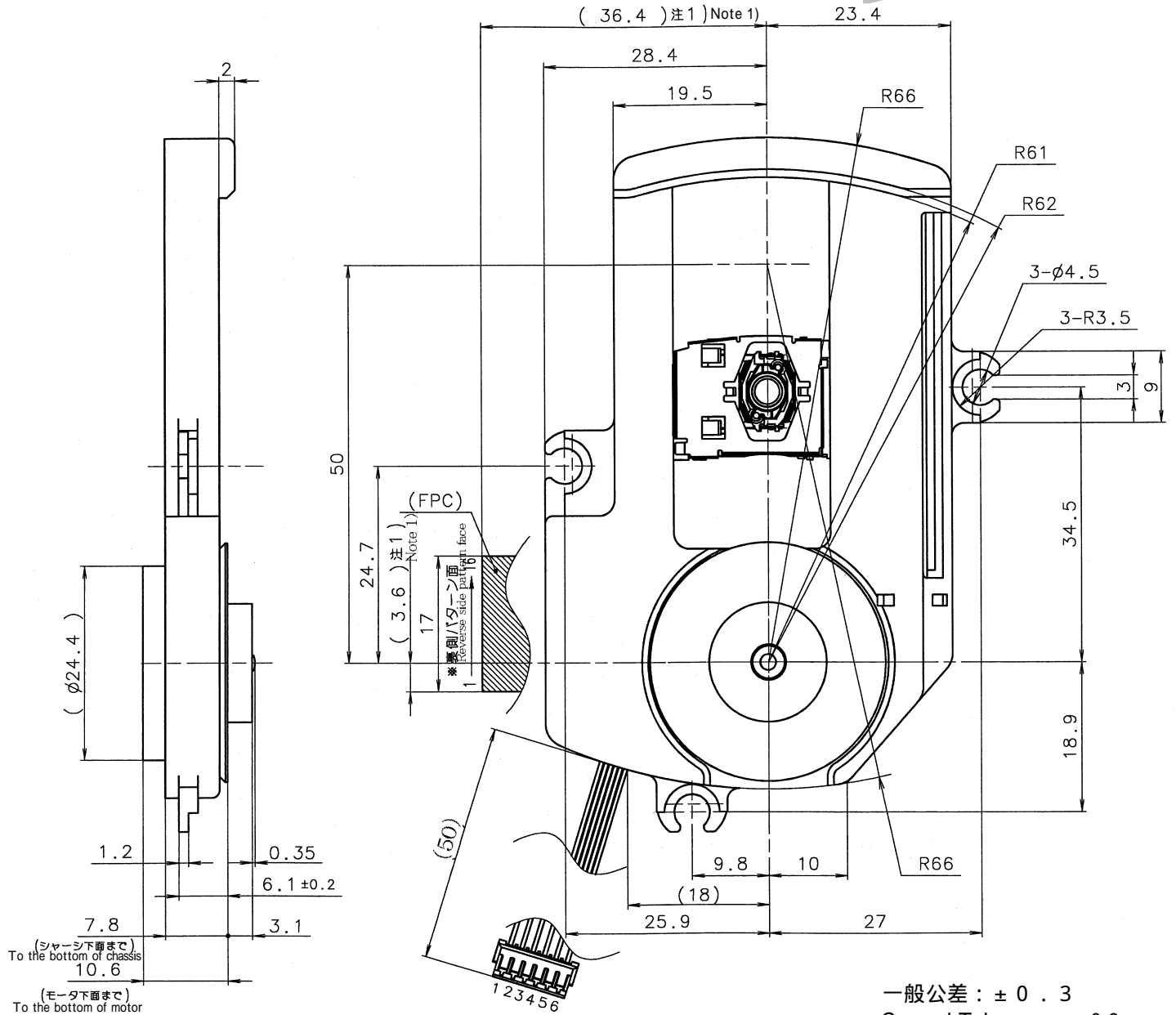
Turntable

Optical pick-up

MD chassis

Lot No.

Stamping area of
Model name and Lot NO.

Z   (axis

X   (axis   Y   (axis

20

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Figure 2. Appearance Drawing

(36.4) 注1) Note 1)   23.4

28.4

19.5

R66

R61

R62

3-ø4.5

3-R3.5

3

9

50

34.5

24.7

(3.6) 注1) Note 1)

17

(FPC)

※裏側パターン面 Reverse side pattern face

18.9

2

(ø24.4)

1.2   0.35

6.1 ±0.2

7.8   3.1

(シャーシ下面まで) To the bottom of chassis
10.6

(モータ下面まで) To the bottom of motor

(50)

(18)

25.9

9.8   10   R66

27

1 2 3 4 5 6

±
General Tolerance : ± 0.3

)
Note 1) Recommended FPC position

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Figure 3.   Pin connection diagram

.   FPC Terminal

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Hologram Unit

16   1

17 ±0.1
15 ±0.05
1 ±0.15
0.7 +0.07 -0.05 (導体幅) Width of conductor
1 ±0.02 (ピッチ) Pitch
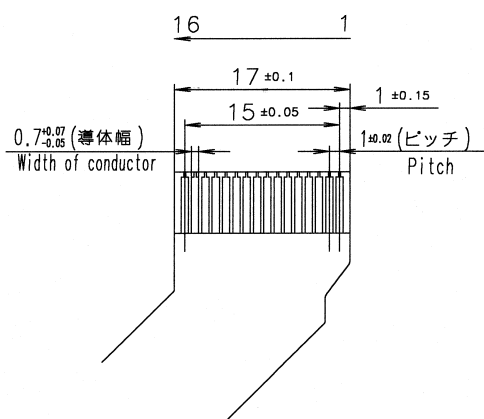
No. Pin No.	Terminal
1	E
2	Vcc
3	GND (Vcc)
4	PD2
5	LD+
6	GND (LD)
7	VR
8	Mon out
9	PD1
10	VC
11	F
12	GND (PDIC)
13	FCS+
14	TRK-
15	TRK+
16	FCS-
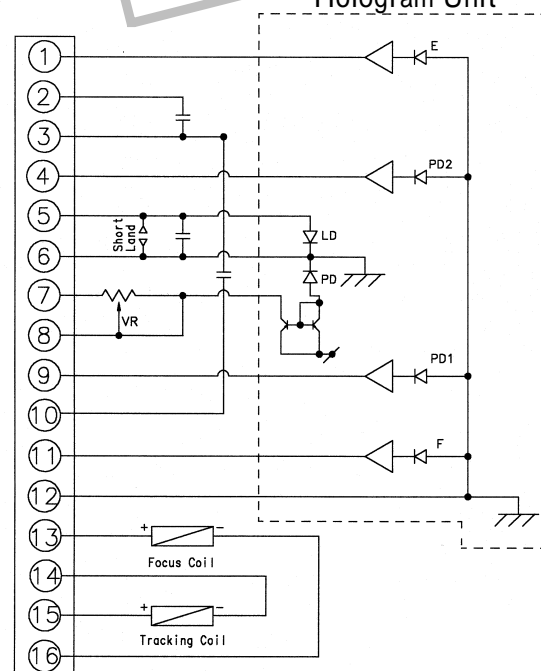
6224

Recommended connector : Product of ELCO INTERNATIONAL CO., LTD.
Series 6224

PD1 - PD2
E - F
RF   PD1 + PD2

.   Housing Terminal

No. Pin No.	Terminal
	SLED +
	SLED -
	LIMIT SW
	LIMIT SW
	SPINDLE (+)
	SPINDLE (-)

SLD Mo.   LIMIT SW   SP Mo.
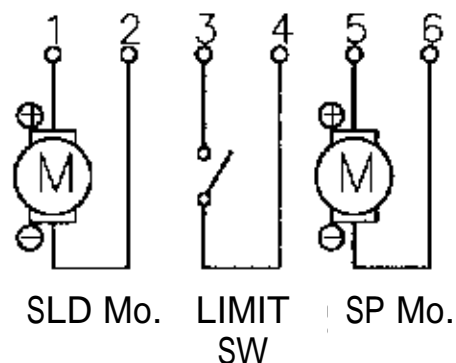
Recommended connector : Product of JAPAN SOLDERLESS TERMINAL CO., LTD.
Series ZR.

Figure 4.   APC Circuit diagram (Reference)

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Figure 5.   Standard test circuit diagram

IC 1~2	⟶	LM6361	TP 2	⟶	PD1 + PD2
IC 5	⟶	LF357N	TP 3	⟶	R.F Level
IC 6,7	⟶	TL084CN	TP 4	⟶	E-F Signal
IC 8	⟶	μPC4558	TP 5	⟶	E Signal
Tr	⟶	2SA706	TP 6	⟶	F Signal

TP 1 ⟶ F.E(Focus.Error)= PD1 - PD2

Vc ○—▢ 1/2Vcc
Vcc : Pick-up supply voltage

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Figure 6.

Major characteristics of Spindle motor (Made by SANYO SEIMITSU)

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Standard operating conditions and electrical characteristics (for reference)

Standard operating conditions	Rated voltage (DC)		2.0 V
	Used voltage range (between motor terminals : DC)		1.0 ～ 3.0 V
	Rated load		0.49 mN·m
Electrical characteristics	Speed	At rated voltage and load	2300 ± 345 r/min
	Current	At rated voltage and load	145 mA or less
	Initial torque	At rated voltage and by winding-up method	1.37 mN·m or more
	Initial current	At rated voltage	400 mA or less

Motor characteristics diagram

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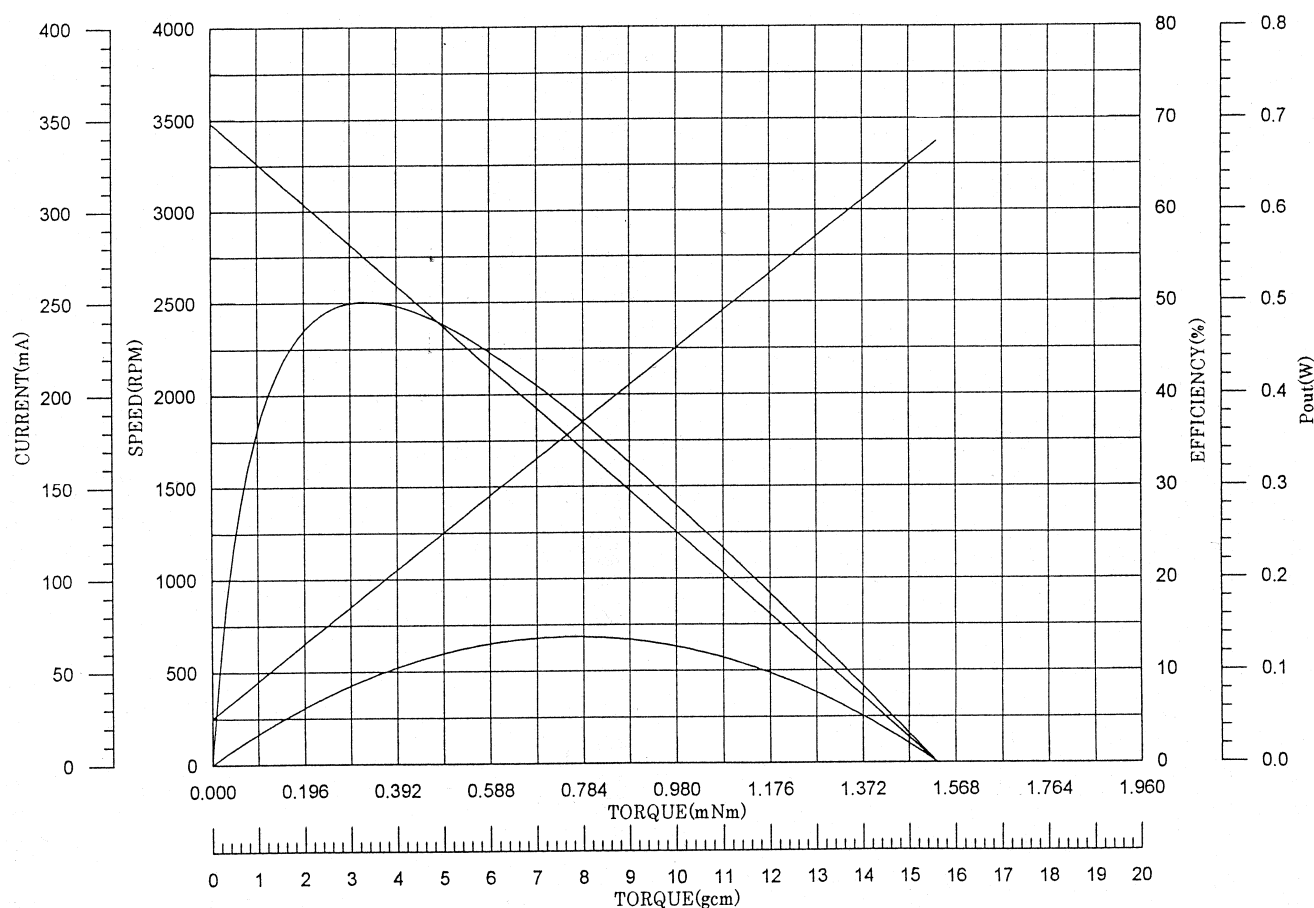
Figure 7.

Major characteristics of Sled motor (Made by MABUCHI)

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Standard operating conditions and electrical characteristics (for reference)

Standard operating conditions	Rated voltage (DC)		1.5 VDC
	Used voltage range (between motor terminals :DC)		1.5 ～ 3.0 V
	Rated load		0.0981 mN・m
Electrical characteristics	Speed	At rated voltage and load	7550 ± 2300 min^{-1}
	Current	At rated voltage and load	180 mA or less
	Initial torque	At rated voltage and by 2points	0.196 mN・m or more
	Initial current	At rated voltage	390 mA or less
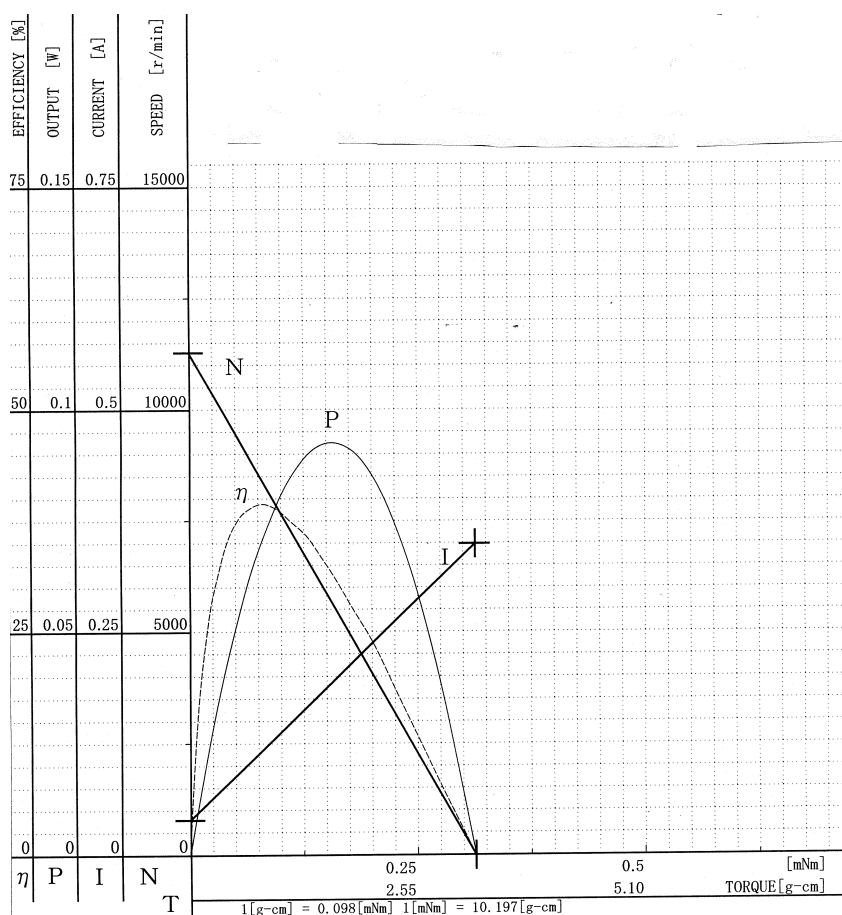
Motor characteristics diagram

1[g-cm] = 0.098[mNm] 1[mNm] = 10.197[g-cm]

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Others

9-1.   Precautions in use

APC Circuit

Vp-p

The output laser power must be controlled with the built-in monitor photodiode, since laser power changes with temperature.   To prevent the characteristics dispersion of the monitor photodiode, the relation between the potentiometer (VR) attached to the pick-up and the monitor photodiode is factory adjusted so that the RF output will be constant.
RF level will be 1 Vp-p when the attached standard test circuit is used.

Connections

Use the specified connectors for electrical connections.
The eye pattern may deteriorate if a digital noise source such as a microcomputer is positioned near the harness from the photodiode.   The laser may deteriorate if the actuator or laser diode connection is poor; securely connect these connecters.

Short - circuit of GND

No.3 GND(Vcc)   No.6 GND(LD)   No.12 GND(PDIC)

Pin No.3, 6 and 12 are not common nodes in the circuit of optical pick-up circuit itself. These lines shall be connected on customer's PWB.

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9-2   Handling instructions

This model is assembled and precisely adjusted in our special plant.
Never attempt to disassemble or readjust it.
Pay attention to the following instructions when handling this model.
Please inform service personnel and users about it.

General

Storage

Avoid storing this model in hot, humid or dusty conditions.

Handling

This model is a precise unit. Be careful not to subject it to shocks by dropping
or rough handling.

Laser diode

Shield your eyes from the laser beam

MAX

0.7×10^4 W/cm²

The output from the LD is only 1mW maximum after going through the objective
lens . However, the intensity of the focused beam reaches about
0.7×10^4 W/cm² . Never look directly into the LD or observe the laser beam
through another lens or mirror.   If you need to view the beam, use an infrared
viewer or an ITV camera.

Toxicity of As

GaAs+GaAlAs

$As_2 O_3$, $AsCl_3$

200

The LD chip is manufactured from GaAs and GaAlAs, which contains toxic As
(Arsenic).   The toxicity of As in this form is far lower than other As compounds
such as $As_2 O_3$ and $AsCl_3$, and the As content of one chip is very small.
However, avoid putting the chip in an acid or alkali solution, heating it over 200   ,
or putting it your mouth.   Defective LDs from the production line and parts
removed in servicing should be disposed of with due care.

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Avoid current surges and electrostatic discharges

10M　　　(DC 500V)　　　　　　　　　　　　320　　　(30W)

The LD may deteriorated if its output is too high and damage may occur if it is exposed
to large currents for even a short time.　 Protect the LD drive circuit from current surges
caused by switches or other sources.　 An electrostatic discharge from the human body
may destroy the LD instantaneously if it is handled carelessly.　 LD terminals are factory
‐strapped before shipment to protect LD from electrostatic discharges during transportation.
For safe handling of the LD, ground your body, measuring equipment, jigs, and tools during
installation.　 Use of a grounding mat on the workbench and floor is recommended.　 After
connector insertion, unstrap the LD terminal with a soldering iron with its metallic tip
grounded or worse insulation resistance is 10 megohms or more (at 500V DC)
five minutes after it is tuned on.　 The temperature of the soldering iron tip must be 320
or below (30W) and the unstrapping should be performed quickly.

Vcc　　　　　　　LD
Avoid the application of current to LD in the case when voltage is not applied to Vcc

Vcc　　　　　　　　　　　　　　　　　LD
　　　LD　　　　　　　　LD
Vcc　　　　　　　LD
LD may deteriorate if the current is applied to LD in the case when the regulated voltage
is not applied to Vcc, because the circuit of element does not operate and LD is applied
over current.　Do not apply the current to LD with voltage is not applied to Vcc.

　　　　　Actuator

　　　　　　　Actuator

The performance of the actuator may be affected if a magnetic material is located nearby,
since the actuator has a strong magnetic field.
Do not allow foreign materials to enter through gap.

　　　　　Handling

Hold the chassis when handling the drive unit. Note that the LD and PD may be damaged
if you come in contact with any of the circuit boards.

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FO-OP-94094

9-3.　　　　　　　　　　　Conformity of main parts to safety standards(UL standard)

TENTATIVE
2002 August 23

This model is designed to conform with the safety standards of various countries.　Since approval depends on the mode of use, however, it is not approved as a unit.　Therefore, apply for approval after mounting the optical drive unit in a player and check it for safety after mounting, too.

Optical Pick-up

Parts Name	Material Manufacturer	Grade	Generic Name	Type No.	ID Mark
HOE 　HOE FPC	SI FLEX CO LTD	94V-0	——	——	⅏ _Si_ F 5a
Slide base	DAINIPPON INK & 　　CHEMICALS INC	94V-0	PPS	FZ-3000-X0	——
	SUMITOMO BAKELITE CO LTD	94V-0	PPS	FM-MK113	——

Drive unit

Parts Name	Material Manufacturer	Grade	Generic Name	Type No.	ID Mark
MD Chassis	ASAHI KASEI CORP	94V-1	PPE	L543V	——

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4-ch Motor Driver for Portable CD Players
Monolithic IC MM1538

Outline

This driver IC contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players. QFP-44 is used for the package, making it ideal for smaller sets.

Features

(1) Built-in 4ch H bridge driver, and PWM control of load drive voltage is made possible by external components.
(2) DC-DC converter control circuit on chip.
(3) With reset output inversion output pin.
(4) Empty detection level can be switched between rechargeable battery and dry battery.
(5) Constant current charging; current value can be varied using external resistor.
(6) Built-in power transistor for charging.
(7) Built-in independent thermal shutdown circuit.

Package

QFP-44

Applications

Portable CD radio cassette recorders

Block Diagram
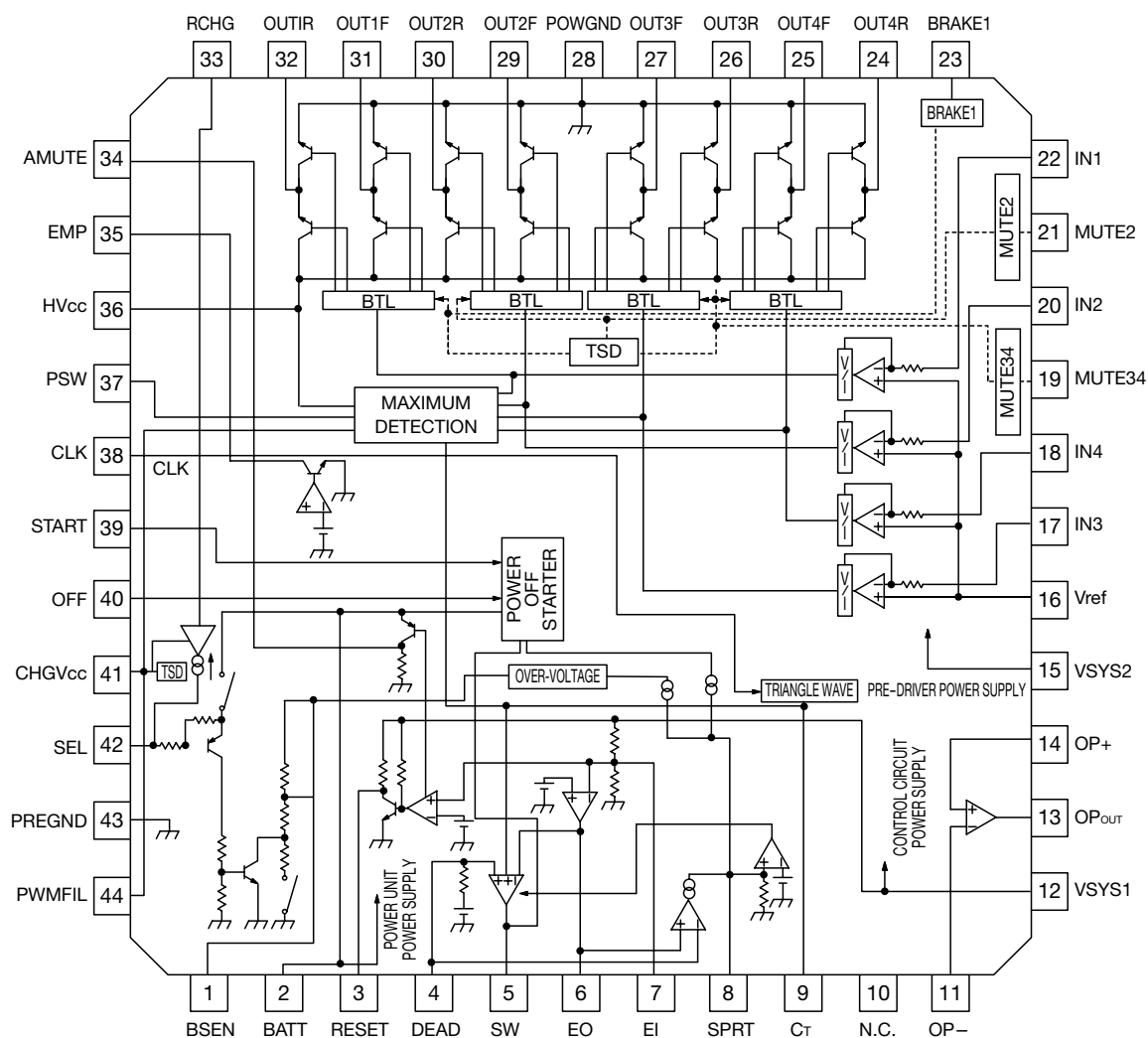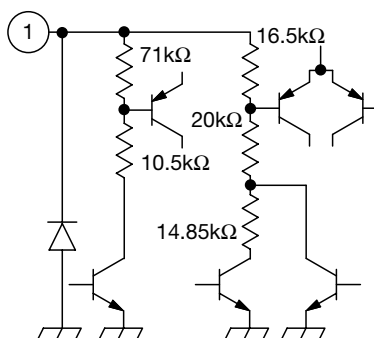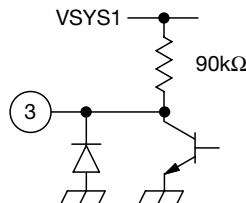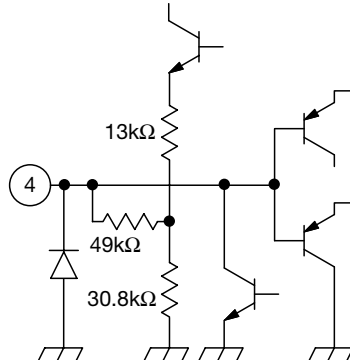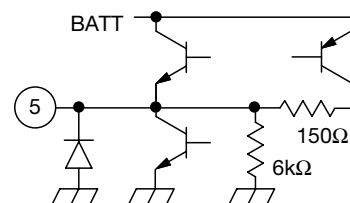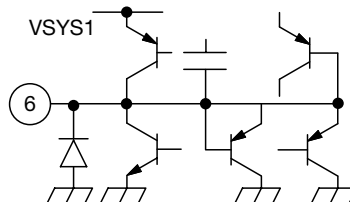
Pin Assignment
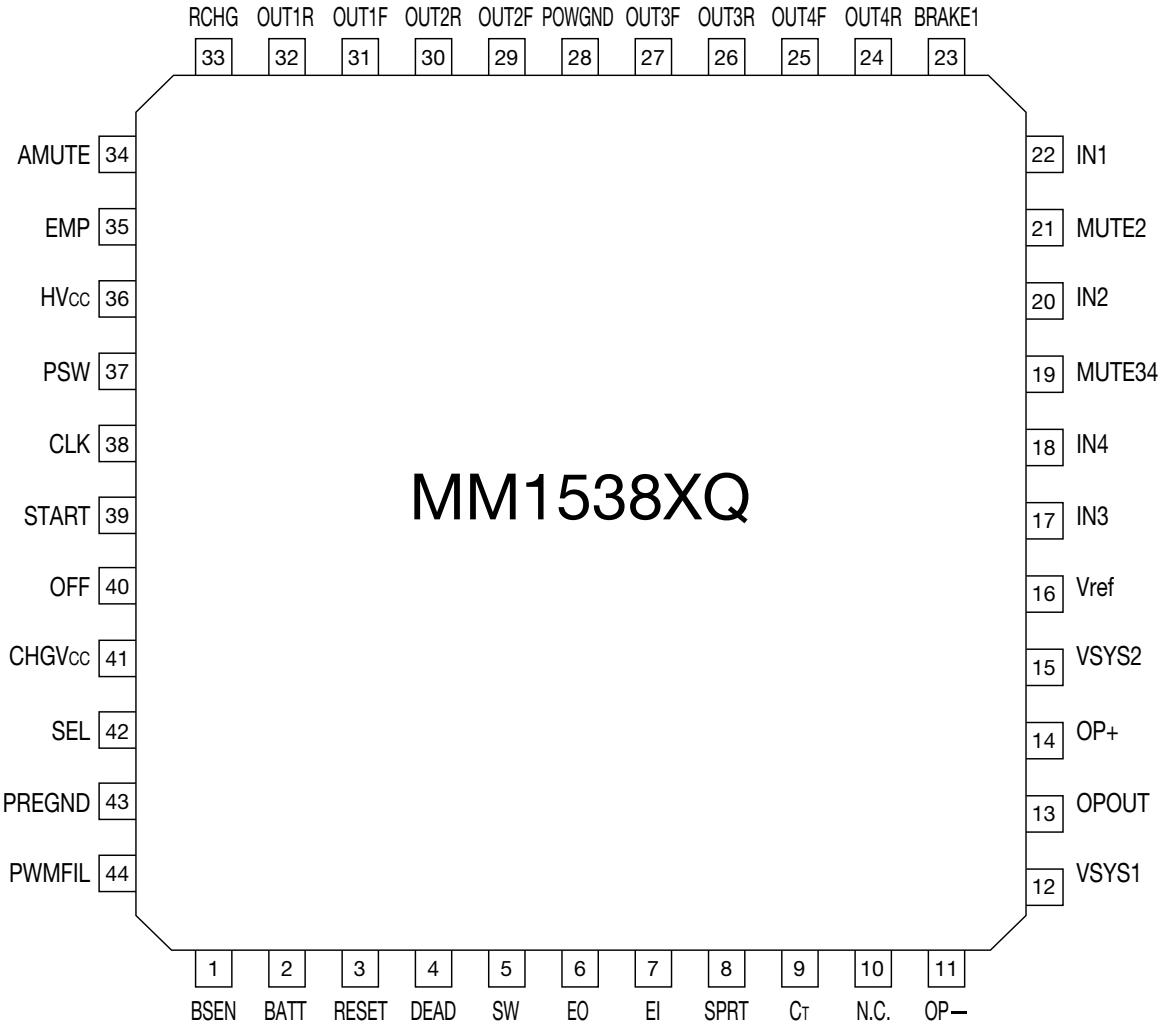
1	BSEN	23	BRAKE1
2	BATT	24	OUT4R
3	RESET	25	OUT4F
4	DEAD	26	OUT3R
5	SW	27	OUT3F
6	EO	28	POWGND
7	EI	29	OUT2F
8	SPRT	30	OUT2R
9	C_T	31	OUT1F
10	N.C.	32	OUT4R
11	OP–	33	RCHG
12	VSYS1	34	AMUTE
13	OPOUT	35	EMP
14	OP+	36	HV_{CC}
15	VSYS2	37	PSW
16	Vref	38	CLK
17	IN3	39	START
18	IN4	40	OFF
19	MUTE34	41	$CHGV_{CC}$
20	IN2	42	SEL
21	MUTE2	43	PREGND
22	IN1	44	PWMFIL
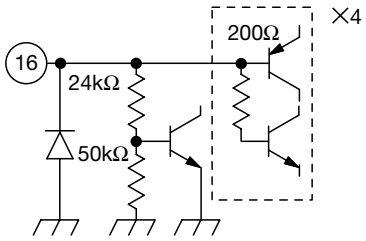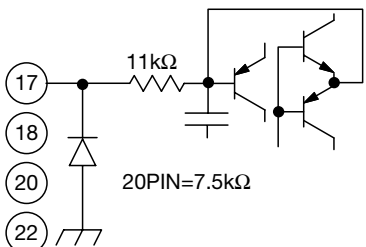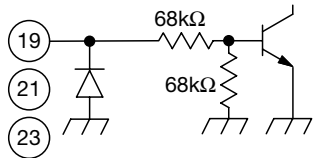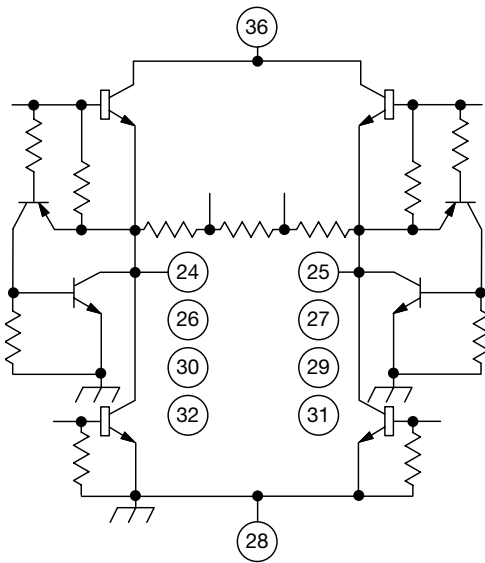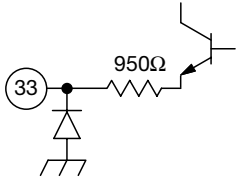
Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
1	BSEN	Input	Battery Voltage Monitor	
2	BATT	Input	Battery Power Supply Input	Power Supply
3	RESET	Output	Reset Detect Output	
4	DEAD	Input	DEAD Time Setting	
5	SW	Output	Transistor Drive For Voltage Multiplier	
6	EO	Output	Error Amplifier Output	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
7	EI	Input	Error Amplifier Input	
8	SPRT	Output	Short Circuit Protection Setting	
9	CT	Output	Triangular–Wave Output	
10	N.C.			
11 14	OP– OP+	Input	Op Amp Negative Input Op Amp Positive Input	
12	VSYS1	Input	Control Circuit Power Supply Input	Control Circuit Power Supply
13	OPOUT	Output	Op Amp Output	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
15	VSYS2	Input	Driver Pre–step Power Supply	Pre–Drive Power Supply
16	Vref	Input	Reference Voltage Input	
17	IN3	Input	ch3 Control Signal Input	
18	IN4		ch4 Control Signal Input	
20	IN2		ch2 Control Signal Input	
22	IN1		ch1 Control Signal Input	
19	MUTE34	Input	ch3 and 4 Mute	
21	MUTE2		ch2 Mute	
23	BRAKE1		ch1 Brake	
24	OUT4R	Output	ch4 Negative Output	
25	OUT4F		ch4 Positive Output	
26	OUT3R		ch3 Negative Output	
27	OUT3F		ch3 Positive Output	
29	OUT2F		ch2 Positive Output	
30	OUT2R		ch2 Negative Output	
31	OUT1F		ch1 Positive Output	
32	OUT1R		ch1 Negative Output	
28	POWGND		Power Block Power Supply Ground	
36	HVcc	Input	H–Bridge Power Supply Input	
33	RCHG	Input	Charge Current Setting	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
34	AMUTE	Output	Reset Invert Output	
35	EMP	Output	Empty Detect Output	
37	PSW	Output	PWM Transistor Drive	
38	CLK	Input	External Clock Synchronizing Input	
39	START	Input	Voltage Multiplier DC–DC Converter Start	
40	OFF	Input	Voltage Multiplier DC–DC Converter OFF	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
41	CHGVcc	Input	Charging Circuit Power Supply Input	Charging Circuit Power Supply
42	SEL	Input Output	Empty Detect Level Switch	
43	PREGND		Pre Section Power Supply Ground	Pre Section Power Supply Ground
44	PWMFIL	Input	PWM Phase Compensation	

* The positive and negative outputs are the polarity with respect to the input

Absolute Maximam Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} *1	13.5	V
Driver Output Current	I_O	500	mA
Power Dissipation	Pd	625 *2	mW
Operating Temperature	T_{OPR}	−30 ~ +85	℃
Storage Temperature	T_{STG}	−55 ~ +150	℃

*1 Vcc shows input voltage of VSYS1,VSYS2,HVcc,BATT,and CHGVcc.

*2 Reduced by 5mW for each increase in Ta of 1℃ over 25℃.

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Control Circuit Power Supply Voltage	VSYS1	2.7	3.2	5.5	V
Pre-Driver Circuit Power Supply Voltage	VSYS2	2.7	3.2	5.5	V
H-Bridge Power Supply Voltage	HV_{CC}		PWM	BATT	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Charging circuit Power Supply Voltage	$CHGV_{CC}$	3.0	4.5	8.0	V
Operating Temperature	Ta	−10	25	70	℃

Electrical Characteristics (unless otherwise specified, Ta=25℃ , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<Common Section>						
BATT Stand-by Current	I_{ST}	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No load)	I_{BAT}	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No load)	I_{SYS1}	HVcc=0.45V, MUTE34=3.2V, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No load)	I_{SYS2}	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No load)	I_{CGVCC}	CHGVcc=4.5V, Rout=OPEN		0.65	2.00	mA
<H−Bridge Driver Part>						
Voltage Gain ch1,ch3.ch4	G_{VC134}		12	14	16	dB
Voltage Gain ch2	G_{VC2}		21.5	23.5	24.5	dB
Gain Error By Polarity	$\triangle G_{VC}$		−2	0	2	dB
Input pin resistance ch1,ch3,ch4	R_{IN134}	IN=1.7V and 1.8V	9	11	13	kΩ
Input pin resistance ch2	R_{IN2}	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	V_{OUT}	RL=8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	V_{satL}	Io=−300mA, IN=0 and 3.2V		240	400	mV
Saturation Voltage (Upper)	V_{satU}	Io=−300mA, IN=0 and 3.2V		240	400	mV
Input Offset Voltage	V_{OI}		−8	0	8	mV
Output Offset Voltage ch1,ch3,ch4	V_{OO134}	Vref=IN=1.6V	−50	0	50	mV
Output Offset Voltage ch2	V_{OO2}	Vref=IN=1.6V	−130	0	130	mV
Dead Zone	V_{DB}		−10	0	10	mV
BRAKE1ON Threshold Voltage	V_{BRON}	IN1=1.8V	2.0			V
BRAKE1OFF Threshold Voltage	V_{BROFF}	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	V_{M2ON}	IN2=1.8V	2.0			V

Electrical Characteristics

(unless otherwise specified, Ta=25℃ , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
\<H−Bridge Driver Part\>						
MUTE2 OFF Threshold Voltage	V_{M2OFF}	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	V_{M34ON}	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V_{M34OFF}	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	V_{refON}	IN1=IN2=IN3=IN4=1.8V	1.2			V
Vref OFF Threshold Voltage	V_{refOFF}	IN1=IN2=IN3=IN4=1.8V			0.8	V
BRAKE1 Brake Current	I_{BRAKE1}	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
\<PWM Power Supply Driving\>						
PSW Sink Current	I_{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V_{SHIF}	IN1=1.8V, HVcc−OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I_{HLK}	HVcc=9.0V, VSYS1=VSYS2=BATT=0V		0	5	μA
PWM Amp Transfer Gain	G_{PWM}	IN1=1.8V, HVcc=1.2 ~ 1.4V	1/60	1/50	1/40	1/kΩ
\<DC−DC Converter\>						
\<Error Amp\>						
VSYS1 Threshold Voltage	V_{S1TH}		3.05	3.20	3.35	V
EO Pin Output Voltage "H"	V_{EOH}	EI=0.7V, Io=−100μA	1.4	1.6		V
EO Pin Output Voltage "L"	V_{EOL}	EI=1.3V, Io=100μA			0.3	V
\<Short Circuit Protection\>						
SPRT Pin Voltage	V_{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I_{SPR1}	EI=0.7V	6	10	16	μA
OFF=L SPRT Pin Current2	I_{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA
SPRT Pin Current3 Over−Voltage	I_{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA
SPRT Pin Impedance	R_{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V_{SPTH}	EI=0.7V, C_T=0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V_{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
\<Transistor Driving\>						
SW Pin Output Voltage1 "H"	V_{SW1H}	BATT=C_T=1.5V, VSYS1=VSYS2=0V, Io=−2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage2 "H"	V_{SW2H}	C_T=0V, Io=−10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage2 "L"	V_{SW2L}	C_T=2.0V, Io=10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f_{SW1}	C_T=470pF, VSYS1=VSYS2=0V Starting Time	65	80	95	kHz
SW Pin Oscillating Frequency2	f_{SW2}	C_T=470pF, CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency3	f_{SW3}	C_T=470pF		88.2		kHz
SW Pin Minimum Pulse Width	T_{SWmin}	C_T=470pF, EO=0.5V→ 0.7V Sweep	0.01		0.60	μs
Pulse Duty Start	D_{SW1}	C_T=470pF, VSYS1=VSYS2=0V	40	50	60	%
Max.Pulse Duty At Self-Running	D_{SW2}	C_T=470pF, EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	D_{SW3}	C_T=470pF, EI=0.7V	65	75	85	%
\<Interface\>						
OFF Pin Threshold Voltage	V_{OFTH}	EI=1.3V			VSYS1-2.0	V
OFF Pin Bias Current	I_{OFF}	OFF=0V	75	95	115	μA
START Pin ON Threshold Voltage	V_{STATH1}	VSYS1=VSYS2=0V, C_T=2.0V			BATT−1.0	V
START Pin OFF Threshold Voltage	V_{STATH2}	VSYS1=VSYS2=0V, C_T=2.0V	BATT−0.3			V

Electrical Characteristics

(unless otherwise specified, Ta=25℃ , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
\<Interface>						
START Pin Bias Current	I_{START}	START=0V	10	20	30	μA
			13	16	19	
CLK Pin Threshold Voltage"H"	V_{CLKTHH}		2.0			V
CLK Pin Threshold Voltage"L"	V_{CLKTHL}				0.8	V
CLK Pin Bias Current	I_{CLK}	CLK=3.2V			10	μA
\<Dead Time>						
DEAD Pin Impedance	R_{DEAD}		52	65	78	kΩ
DEAD Pin Output Voltage	V_{DEAD}		0.78	0.88	0.98	V
\<Starter Circuit>						
Starter Switching Voltage	V_{STNM}	VSYS1=VSYS2=0V→3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SNHS}	START=0V	130	200	300	mV
Discharge Release	V_{DIS}		1.63	1.83	2.03	V
\<Empty Detection>						
EMP Detection Voltage 1	V_{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage 2	V_{EMPT2}	ISEL=−2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	ISEL=−2μA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	Io=1mA, BSEN=1V			0.5	V
EMP Pin Output Leak Current	I_{EMPL}	BSEN=2.4V			1.0	μA
BSEN Pin Input Resistance	R_{BSEN}	VSEL=0V	17	23	27	kΩ
BSEN Pin Leak Current	I_{BSENL}	VSYS1=VSYS2=0V, BSEN=4.5V			1.0	μA
SEL Pin Detection Voltage	V_{SELTH}	V_{SELTH}=BATT−SEL, BSEN=2.0V	1.5			V
SEL Pin Detection Current	I_{SELT}		−2			μA
\<Reset Circuit>						
VSYS1 RESET Threshold Voltage Ratio	H_{SRT}	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}		25	50	100	mV
RESET Pin Output Voltage	V_{RST}	Io=1mA, VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	R_{RST}		72	90	108	kΩ
AMUTE Pin Output Voltage 1	V_{AMT1}	Io=−1mA, VSYS1=VSYS2=2.8V	BATT−0.4		BATT	V
AMUTE Pin Output Voltage 2	V_{AMT2}	Io=−1mA, START=0V, VSYS1=VSYS2=0V	BATT−0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	R_{AMT}		77	95	113	kΩ
\<Op Amp>						
Input Bias Current	I_{BIAS}	OP+=1.6V			300	nA
Input Offset Voltage	V_{OIOP}		−5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	RL=OPEN	2.8			V
Low level Output Voltage	V_{OLOP}	RL=OPEN			0.2	V
Output Drive Current (Source)	I_{SOU}	50Ω GND		−6.5	−3.0	mA
Output Drive Current (Sink)	I_{SIN}	50Ω VSYS1	0.4	0.7		mA
Open Loop Voltage Gain	GVO	V_{IN}=−75dBV, f=1kHz		70		dB
Slew Rate	SR			0.5		V/μs
\<Battery Charging Circuit>						
RCHG Pin Bias Voltage	V_{RCHG}	CHGVcc=4.5V, RCHG=1.8kΩ	0.71	0.81	0.91	V

Electrical Characteristics

(unless otherwise specified, Ta=25℃ , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<Battery Charging Circuit>						
RCHG Pin Output Resistance	R_{RCHG}	CHGVcc=4.5V, RCHG=0.5 and 0.6V	0.75	0.95	1.20	kΩ
SEL Pin Leak Current 1	I_{SELLK1}	CHGVcc=4.5V, RCHG=OPEN, BATT=4.5V			1.0	µA
SEL Pin Leak Current 2	I_{SELLK2}	CHGVcc=0.6V, RCHG=1.8kΩ, BATT=4.5V			1.0	µA
SEL Pin Saturation Voltage	V_{SELCG}	CHGVcc=4.5V, Io=300mA, RCHG=0Ω		0.45	1.00	V

Measuring Circuit

Switching Position Table

Item	SW No.									
	1	4	5	6	7	8	22	24	25	26
BATT Stand-by Current	–	–	–	–	–	–	–	–	–	–
BATT Supply Current (No load)	–	–	–	–	–	–	a	–	a	–
VSYS1 Supply Current (No load)	–	–	–	a	–	–	a	–	a	–
VSYS2 Supply Current (No load)	–	–	–	–	–	–	a	–	a	–
CHGVcc Supply Current (Noload)	–	–	–	–	–	–	–	–	–	–
VSYS1 Threshold Voltage	–	–	a	–	–	–	–	–	–	–
EO Pin Output Voltage "H"	–	–	a	a	–	–	–	–	–	–
EO Pin Output Voltage "L"	–	–	a	a	–	–	–	–	–	–
SPRT Pin Voltage	–	–	–	a	a	–	–	–	–	–
SPRT Pin Current1 EO="H"	–	–	–	a	b	–	–	–	–	–
SPRT Pin Current2 OFF="L"	–	–	–	a	b	–	–	–	–	a
SPRT Pin Current3 Over-Voltage	a	–	–	a	b	–	–	–	–	–
SPRT Pin Impedance	–	–	–	–	b	–	–	–	–	–
SPRT Pin Threshold Voltage	–	–	–	a	a	a	–	–	–	–
Over-Voltage Protection Detect	a	–	–	–	a	–	–	–	–	–
SW Pin Output Voltage1 "H"	–	a	–	–	–	a	–	–	a	–
SW Pin Output Voltage2 "H"	–	a	–	a	b	a	–	–	–	–
SW Pin Output Voltage2 "L"	–	a	–	–	–	a	–	–	–	–
SW Pin Oscillating Frequency 1	–	b	–	–	–	b	–	–	a	–
SW Pin Oscillating Frequency 2	–	b	–	–	–	b	–	b	–	–
SW Pin Oscillating Frequency 3	–	b	–	–	–	b	–	a	–	–
SW Pin Minimum Pulse Width	–	b	b	–	–	b	–	–	–	–
Pulse Duty Start	–	b	–	–	–	b	–	b	a	–
Max. Pulse Duty At Self-Running	–	b	–	–	–	b	–	b	–	–
Max. Pulse Duty At CLK Synchronization	–	b	–	a	–	b	–	a	–	–

– : Turn off switch

Switching Position Table

Item	SW No.									
	2	3	4	6	7	8	20	24	25	26
DEAD Pin Impedance	–	b	–	–	–	–	–	–	–	–
DEAD Pin Output Voltage	–	a	–	–	–	–	–	–	–	–
OFF Pin Threshold Voltage	–	–	–	a	a	–	–	–	–	a
OFF Pin Bias Current	–	–	–	–	–	–	–	–	–	a
START Pin ON Threshold Voltage	–	–	a	–	–	a	–	–	a	–
START Pin OFF Threshold Voltage	–	–	a	–	–	a	–	–	a	–
START Pin Bias Current	–	–	–	–	–	–	–	–	a	–
CLK Pin Threshold Voltage"H"	–	–	a	–	–	b	–	b	–	–
CLK Pin Threshold Voltage"L"	–	–	a	–	–	b	–	b	–	–
CLK Pin Bias Current	–	–	–	–	–	–	–	a	–	–
Starter Switching Voltage	–	–	a	–	–	–	–	–	a	–
Starter Switching Hysteresis Width	–	–	a	–	–	–	–	–	a	–
Discharge Release Voltage	–	–	–	–	a	–	–	–	–	–
VSYS1 Pin RESET Threshold Voltage Ratio	b	–	–	–	–	–	–	–	–	–
RESET Detection Hysteresis Width	b	–	–	–	–	–	–	–	–	–
RESET Pin Output voltage	b	–	–	–	–	–	–	–	–	–
RESET Pin PULL UP Resistance	a	–	–	–	–	–	–	–	–	–
AMUTE Pin Output Voltage 1	–	–	–	–	–	–	b	–	–	–
AMUTE Pin Output Voltage 2	–	–	–	–	–	–	b	–	a	–
AMUTE Pin PULL DOWN Resistance	–	–	–	–	–	–	a	–	–	–

– : Turn off switch

Switching Position Table

Item	SW No.						
	1	9	10	11	12	21	27
EMP Detection Voltage 1	a	–	–	–	–	a	a
EMP Detection Voltage 2	a	–	–	–	–	a	b
EMP Detection Hysteresis Voltage 1	a	a	–	–	–	a	a
EMP Detection Hysteresis Voltage 2	a	–	–	–	–	a	b
EMP Pin Output Voltage	a	–	–	–	–	b	–
EMP Pin Output Leak Current	a	–	–	–	–	c	–
BSEN Pin Input Resistance	a	–	–	–	–	–	a
BSEN Pin Leak Current	a	–	–	–	–	–	–
SEL Pin Detection Voltage	a	–	–	–	–	a	a
SEL Pin Detection Current	a	–	–	–	–	a	b
Input Bias Current	–	–	a	–	–	–	–
Input Offset Voltage	–	–	d	–	–	–	–
"H" Level Output Voltage	–	b	c	–	–	–	–
"L" Level Output Voltage	–	a	c	–	–	–	–
Output Drive Current (Source)	–		d	b	–	–	–
Output Drive Current (Sink)	–	–	d	a	–	–	–
Open Loop Voltage Gain	–	–	b	–	a	–	–
Slew Rate	–	–	d	–	a	–	–

– : Turn off switch

Switching Position Table

Item		13	14	15	16	17	18	22
		_	_	SW	No.	_	_	_
Voltage Gain	ch1R	–	–	–	b	b	b	a
	ch2R	–	–	b	–	b	b	a
	ch3R	b	–	–	–	b	b	a
	ch4R	–	b	–	–	b	b	a
Gain Error By Polarity	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Input pin resistance	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Maximum Output Voltage	ch1R	–	–	–	b	b	b	a
	ch2R	–	–	b	–	b	b	a
	ch3R	b	–	–	–	b	b	a
	ch4R	–	b	–	–	b	b	a
Saturation Voltage (Lower)	ch1F	–		–	b	a	–	a
	ch1R	–		–	b	–	a	a
	ch2F	–		b	–	a	–	a
	ch2R	–		b	–	–	a	a
	ch3F	b		–	–	a	–	a
	ch3R	b		–	–	–	a	a
	ch4F	–	b	–	–	a	–	a
	ch4R	–	b	–	–	–	a	a
Saturation Voltage (Upper)	ch1F	–	–	–	b	a	–	a
	ch1R	–	–	–	b	–	a	a
	ch2F	–	–	b	–	a	–	a
	ch2R	–	–	b	–	–	a	a
	ch3F	b	–	–	–	a	–	a
	ch3R	b	–	–	–	–	a	a
	ch4F	–	b	–	–	a	–	a
	ch4R	–	b	–	–	–	a	a
Input Offset Voltage	ch1	–	–	–	a	–	–	a
	ch2	–	–	a	–	–	–	a
	ch3	a	–	–	–	–	–	a
	ch4	–	a	–	–	–	–	a
Output Offset Voltage	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Dead Zone	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a

– : Turn off switch

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Switching Position Table

Item		SW No.								
		13	14	15	16	17	18	22	23	28
BRAKE1 ON Voltage	ch1	–	–	–	b	b	b	a	–	–
BRAKE1 OFF Voltage	ch1	–	–	–	b	b	b	a	–	–
MUTE2 ON Voltage	ch2	–	–	b	–	b	b	a	–	–
MUTE2 OFF Voltage	ch2	–	–	b	–	b	b	a	–	–
MUTE34 ON Voltage	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
MUTE34 OFF Voltage	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
Vref ON Voltage	ch1	–	–	–	b	b	b	a	–	–
	ch2	–	–	b	–	b	b	a	–	–
	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
Vref OFF Voltage	ch1	–	–	–	b	b	b	a	–	–
	ch2	–	–	b	–	b	b	a	–	–
	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
BREAK1 Brake Current	ch1	–	–	–	b	b	b	a	–	–
PWM Sink Current		–	–	–	b	–	–	a	b	a
HVcc Level Shift Voltage		–	–	–	b	b	b	b	a	b
HVcc Leak Current		–	–	–	–	b	b	a	–	–
PWM Amp Transfer Gain		–	–	–	b	b	b	a	–	–

Item	SW No.	
	19	27
CHGSET Pin Bias Voltage	a	–
CHGSET Pin Output Resistance	b	–
SEL Pin Leak Current 1	–	a
SEL Pin Leak Current 2	a	a
SEL Pin Saturation Voltage	b	b

– : Turn off switch

Switching Position Table
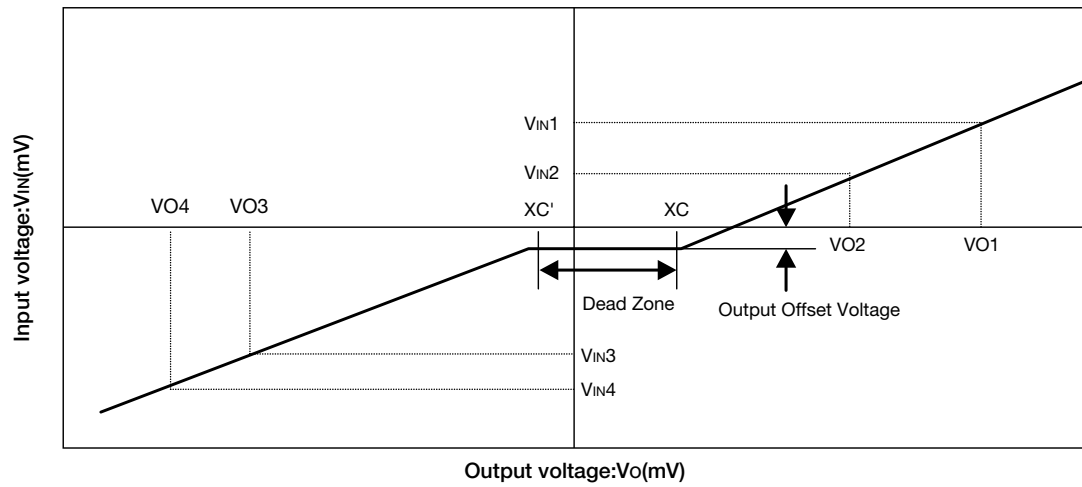
◎ Voltage Gain

$$G_{VC}(+) = 20 \log \frac{VO1 - VO2}{V_{IN}1 - V_{IN}2}$$

$$G_{VC}(-) = 20 \log \frac{VO3 - VO4}{V_{IN}3 - V_{IN}4}$$

◎ Gain Error By Polarity

$$G_{VC} = G_{VC}(+) - G_{VC}(-)$$

◎ Dead Zone

$$XC - XC' = \frac{V_{IN}2 \cdot VO1 - V_{IN}1 \cdot VO2}{VO1 - VO2} - \frac{V_{IN}3 \cdot VO4 - V_{IN}4 \cdot VO3}{VO3 - VO4}$$

Application Circuit
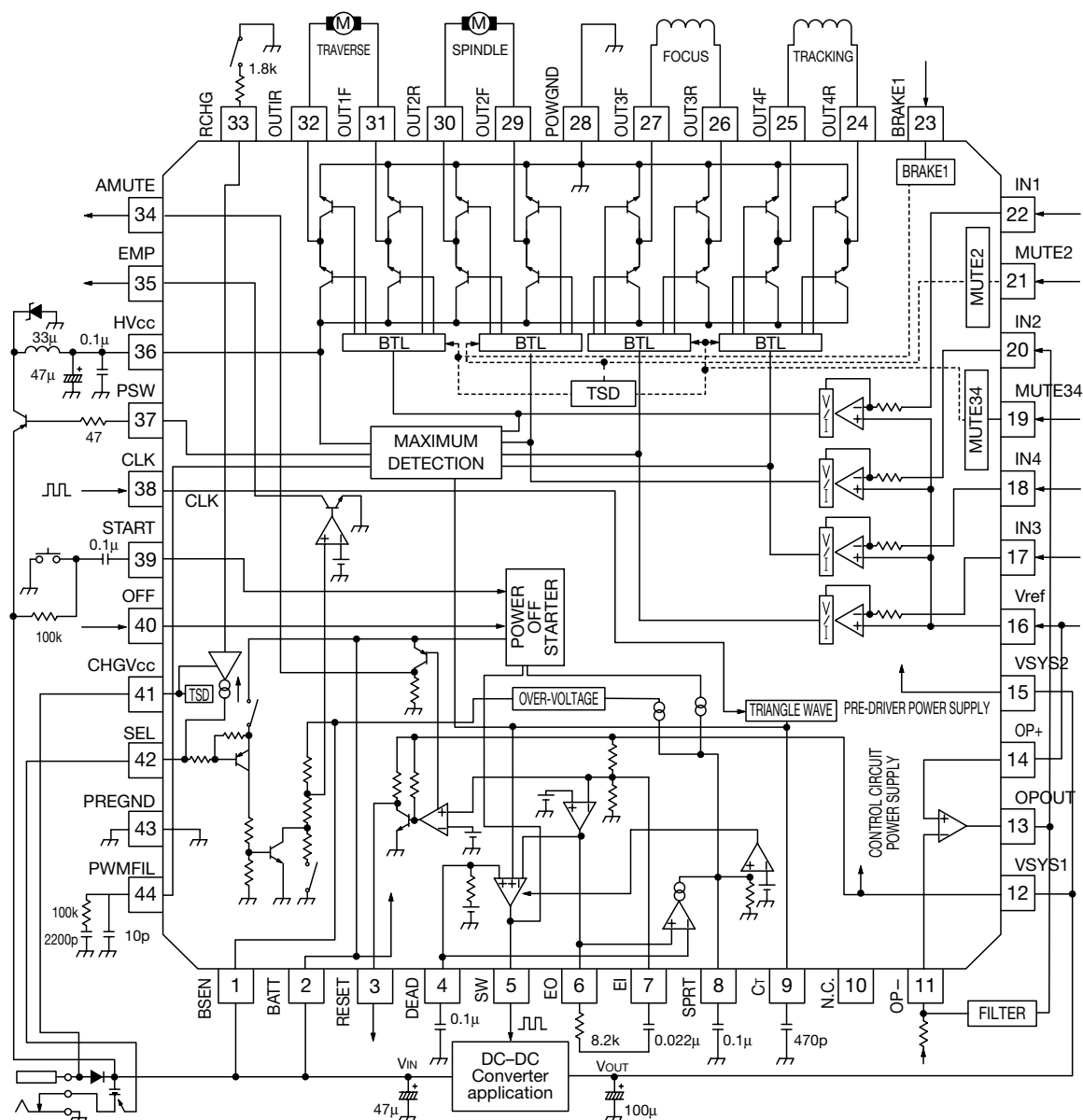
· We shall not be liable for any trouble or damege caused by using this circuit.
· In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefor.

Circuit operation

1 H-bridge driver block

(1) Gain setting

· The driver input resistance (ch 1,3 and 4) are 11kΩ typ. ,ch2 is 7.5kΩ typ. . Set the gain according to the following formula.

ch1 ch2 ch3	$GV = 20\log \left\| \dfrac{55k}{11k+R} \right\|$ (db)
ch2	$GV = 20\log \left\| \dfrac{110k}{7.5k+R} \right\|$ (db)

R:Externally-connected input

· The driver output stage power supply is HVcc(36PIN), and the bridge circuit power supply is VSYS2 (15PIN). Connect a bypass capacitor between these two power supplies(approximately 0.1μF).

(2) Mute function

· Of the four drivers,ch1 has a brake function,and the other channels have a mute function.
· When BRAKE1(23PIN)is set to high level, both ch1 outputs go low level, and the circuit enters brake mode.
· When MUTE2(21PIN)is set to high level, the ch2 output is muted.
· When MUTE34(19PIN)is set to high level, the ch3 and 4 outputs are muted.

(3) Vref drop mute

· When the voltage applied to Vref(16PIN)is 1.0V or less typ. , the driver outputs are set to high impedance.

(4) Thermal shutdown

· When the chip temperature reaches 150°C typ. the output current is cut. The chip starts operating again at about 120°C typ. .

2 PWM power supply drive block

· This detects the maximun output level from among the four channels, and supplies the load drive power supply(36PIN)for the PWM. The external components are a PNP transistor, coil, Schottky diode,and capacitor.
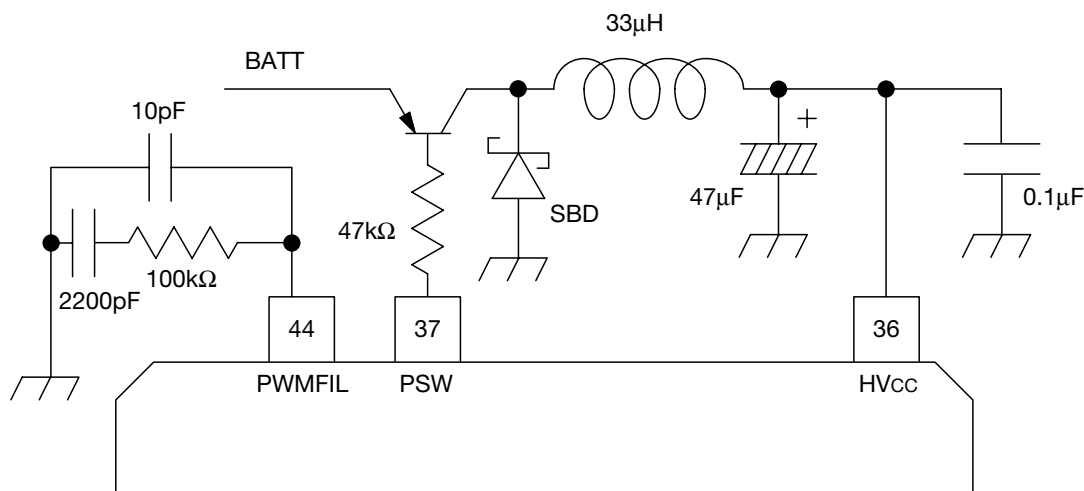
3 DC-DC converter block

(1) Output voltage

・ 3.2V typ. voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$VSYS1 = 1.2 \times \frac{\dfrac{R1 \cdot R3}{R1+R3} + \dfrac{R2 \cdot R4}{R2+R4}}{\dfrac{R2 \cdot R4}{R2+R4}} \quad (V)$$

R1=external resistor
R2=external resistor
R3=35kΩ
R4=21kΩ
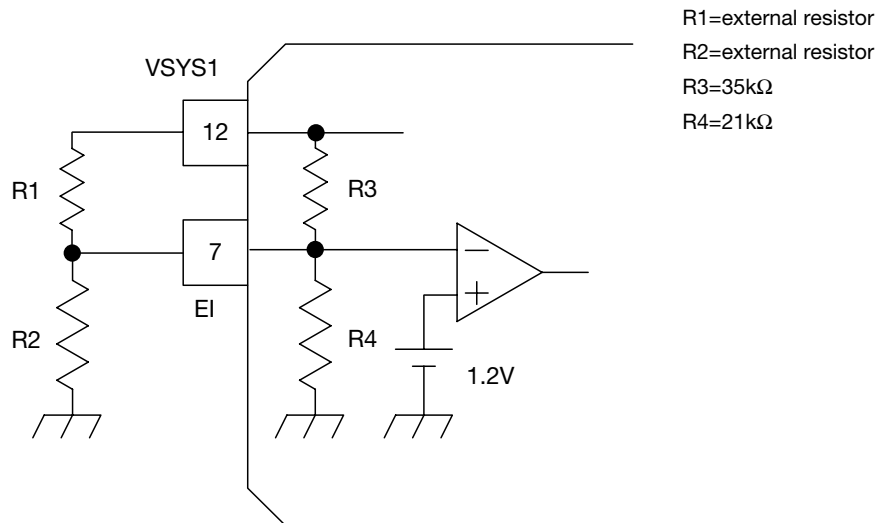
(2) Short protect function

・ When the error amplifier output(6PIN)has switched to the high-level state,SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops.The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t = CSPRT \times \frac{V_{TH}}{ISPRT} \ (sec) \quad (V_{TH}=1.2V, \ ISPRT=10\mu A)$$

(3) Soft start function

・ The soft start function operates when a capacitor is connected between DEAD(4PIN)and GND.
  Also, the maximum duty can be varied by connecting a resistor to 4PIN.

$$t = CDEAD \times R \ (sec) \quad (R=65k\Omega)$$

(4) Power off function

・ When low-level is applied to OFF(40PIN), SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t = CSPRT \ \frac{V_{TH}}{I_{OFF}} \ (sec) \quad (V_{TH}=1.2V, \ I_{OFF}=20\mu A)$$

(5) Over voltage protection circuit
- When the voltage applied to BSEN(1PIN)reaches 8.4V typ. , SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , theSW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t = CSPRT \times \frac{V_{TH}}{IHV} \text{ (sec)} \quad (V_{TH}=1.2V, I_{HV}=20\mu A)$$

4 Empty detector block

(1) Output voltage
- When the voltage applied to the BSEN(1PIN)falls below the detector voltage, EMP(35PIN)goes from high level to low level(open-collector output). The detector voltage has 50mV typ. of hysteresis to prevent output chattering. Use SEL(42PIN)to switch the detection voltage as shown below.

SEL	Detect Voltage	Return Voltage
L	2.20V typ.	2.25V typ.
High-Z	1.80V typ.	1.85V typ.

5 Reset circuit block

- At about 90% typ. of the DC-DC converter output voltage, RESET(3PIN)goes from low level to high level, and AMUTE(34PIN)goes from high level to low level. The reset voltage has 50mV typ. of hysteresis to prevent output chattering.

6 Charging circuit block

- The power supply for the charging circuit block is CHGV$_{CC}$(41PIN), and is independent from the other circuits.The resistance between RCHG(33PIN)and GND sets the charging current. This current is drawn from SEL(42PIN).

- A thermal shutdown circuit is provided,and when the chip temperature reaches 150°C typ. the charging current is cut. The chip starts operating again at about 120°C typ. .

Characteristics

■ Input Load Fluctuation

RL=∞

Output voltage:Vo(V) vs Input voltage:VIN(V)

8Ω   4Ω   20Ω   4Ω   8Ω   20Ω   ∞

·Ta=normal temperature
·BATT=HVcc=4V
·VSYS1=VSYS2=3.2V
·Vref=1.6V

■ Input Load Fluctuation (ch2)

RL=∞

Output voltage:Vo(V) vs Input voltage:VIN(V)

4Ω   8Ω   20Ω   20Ω   8Ω   4Ω   ∞

·Ta=normal temperature
·BATT=HVcc=4V
·VSYS1=VSYS2=3.2V
·Vref=1.6V

■ Daed Zone

Input voltage:VIN(mV) vs Out voltage:Vo(mV)

·Ta=normal temperature
·BATT=HVcc=4V
·VSYS1=VSYS2=3.2V
·Vref=1.6V

20Ω   8Ω   4Ω   8Ω   20Ω   4Ω

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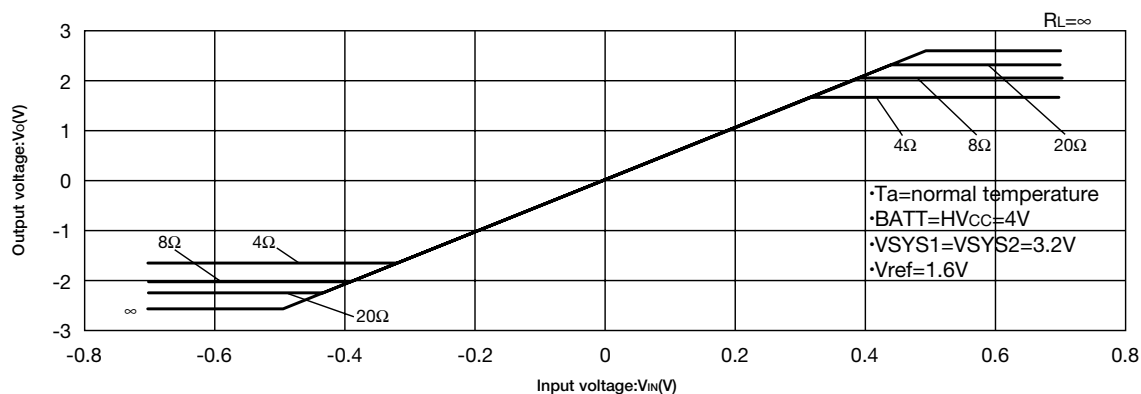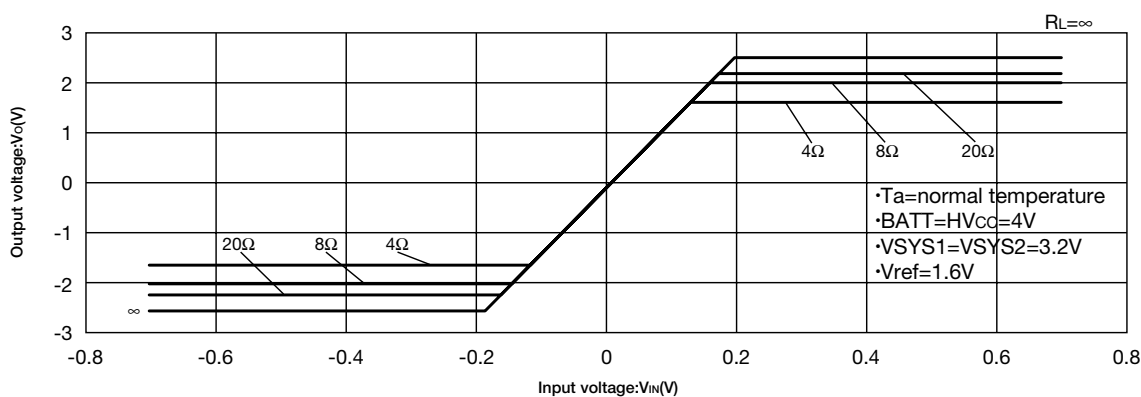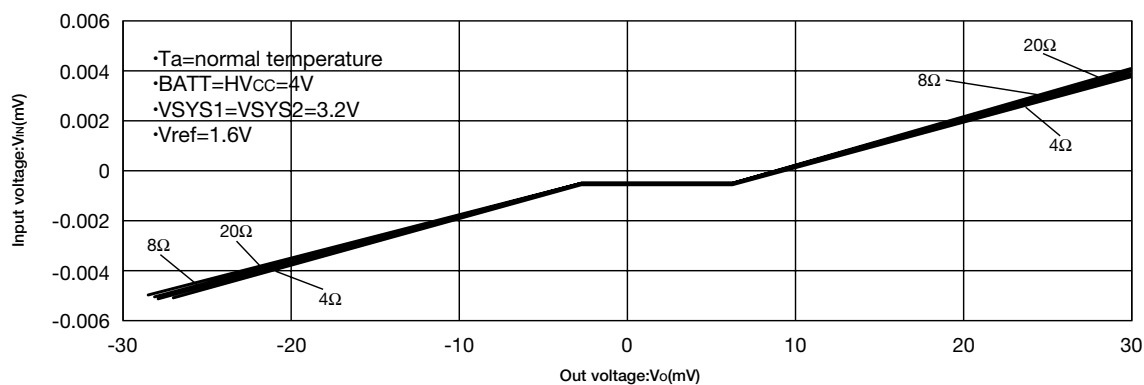
Characteristics

■ Error Amp Output Voltage

Dead Output voltageE:V_{DAED}(V)
Eo Output voltage:V_{EO}(V)

Ta=normal temperature
BATT=2.4V

EO PIN

DAED PIN

Control Circuit Power Supply voltage:VSYS1(V)

■ Resete Pin Voltage

Reset Output voltage:V_{RIST}(V)

Ta=normal temperature
BATT=2.4V

Control Circuit Power Supply voltage:VSYS1(V)
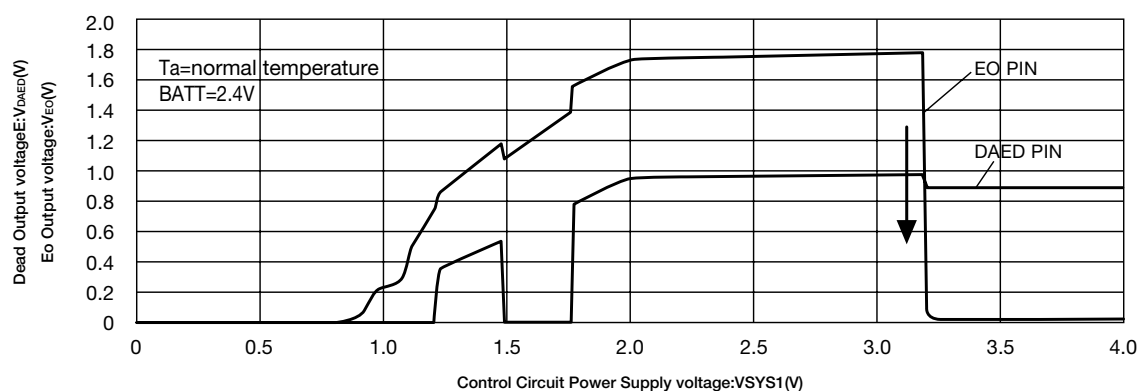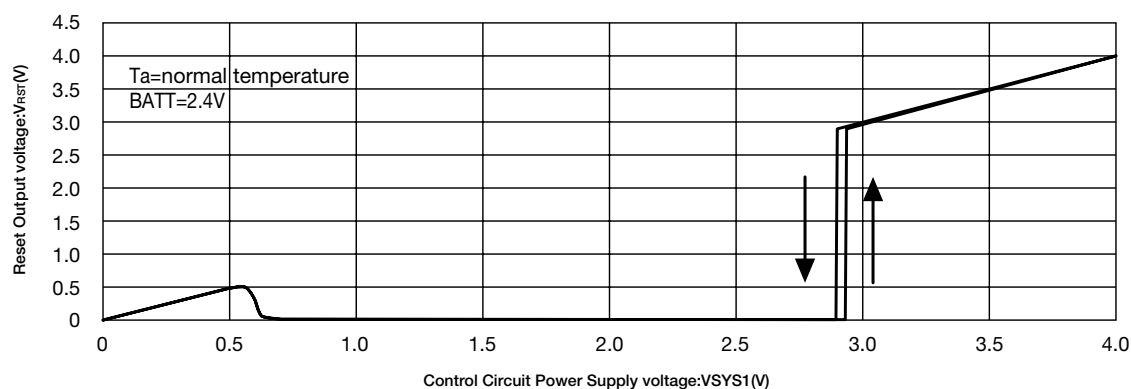
RF Amplifier for CD Players

Description

The CXA2550M/N is an IC developed for compact disc players. This IC incorporates an RF amplifier, focus error amplifier, tracking error amplifier, APC circuit and RF level control circuit. (The voltage-converted optical pickup output is supported.)

Features

- Low power consumption (35mW at 3.5V)
- APC circuit
- RF level control circuit
- Both single power supply and dual power supply operations possible.

Structure

Bipolar silicon monolithic IC

Applications

Compact disc players

CXA2550M
20 pin SOP (Plastic)
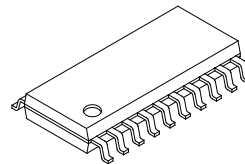
CXA2550N
20 pin SSOP (Plastic)
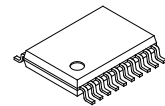
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12		V
• Operating temperature	Topr	−20 to +75		°C
• Storage temperature	Tstg	−65 to +150		°C
• Allowable power dissipation				
	P_D (SOP)	620		mW
	(SSOP)	370		mW

Operating Conditions

Supply voltage	$V_{CC} - V_{EE}$	3.0 to 4.0	V

Block Diagram and Pin Configuration (Top View)

E97514-PS

Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	AGCVTH	—		Reference level variable pin for RF level control. The reference level can be varied by the external resistor.
2	LD	O		APC amplifier output pin.
3	PD	I		APC amplifier input pin.
4 5	PD1 PD2	I I		Inversion input pin for RF I-V amplifiers. Connect these pins to the photodiodes A + C and B + D respectively. The current is supplied.
6	V_{EE}	—		V_{EE} pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
7 8	F E	I I		Inversion input pin for F and E I-V amplifiers. Connect these pins to the photodiodes F and E respectively. The current is supplied.
9	EI	—		Gain adjustment pin for I-V amplifier.
10	VC	O		DC voltage output pin of (Vcc + VEE)/2. Connect to GND for ±1.75 power supply; connect a smoothing capacitor for single +3.5V power supply.
11	TE	O		Tracking error amplifier output pin. E-F signal is output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
12	FE_BIAS	I		Bias adjustment pin for inverted side of focus error amplifier.
13	FE	O		Focus error amplifier output pin.
14	RFM	I		RF amplifier inverted side input pin. RF amplifier gain is determined by the resistor connected between this pin and RFO pin.
15	RF O	O		RF amplifier output pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
16	RF I	I		The RF amplifier output RFO is input with its capacitance coupled.
17	RFTC	—		External time-constant pin for RF level control.
18	AGCCONT	I		RF level control ON (limit level of 50%/30%)/OFF switching pin. OFF for Vcc, 30% for open or Vc and 50% for V$_{EE}$.
19	LD_$\overline{ON}$	I		APC amplifier ON/OFF switching pin. OFF for Vcc and ON for V$_{EE}$.
20	Vcc			Vcc pin.

Electrical Characteristics

(Ta = 25°C, V$_{CC}$ = 1.75V, V$_{EE}$ = −1.75V, V$_C$ = GND)

No.	Measurement item	Symbol	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	I1	I2	E1	E2	E3	E4	Measurement pin	Description of I/O waveform and measurement method	Min.	Typ.	Max.	Unit
1	Current consumption	Icc							O	O							20	Input GND	6.37	9.8	13.23	mA
2	Current consumption	IEE							O	O							6	Input GND	−13.23	−9.8	−6.37	mA
3	Offset voltage 1 (RF amplifier)	V15-1															15	Input resistance 33kΩ, Output DC measurement	−50.0	−10	60.0	mV
4	Voltage gain	V15-2			O												15	Input 1kHz 120mVp-p, Output AC measurement	16.7	19.7	22.7	dB
5	Frequency response	V15-3															15	Input 3MHz 120mVpp, Output AC measurement	−3	—	—	dB
6	Maximum output amplitude H	V15-4		O	O			O					300mV				15	Output DC measurement	1.45	—	—	V
7	Maximum output amplitude L	V15-5		O	O			O					−300mV				15	Output DC measurement	—	—	−1.25	V
8	Offset voltage (FE amplifier)	V13-1															13	Input resistance 33kΩ, Output DC measurement	−120.0	0	120.0	mV
9	Voltage gain 1	V13-2		O													13	Input 1kHz 120mVp-p, Output AC measurement	16.4	19.4	22.4	dB
10	Voltage gain 2	V13-3			O												13	Input 1kHz 120mVp-p, Output AC measurement	16.4	19.4	22.4	dB
11	Voltage gain difference	V13-4															13	V13-4 = V13-2 − V13-3	−3.0	0	3.0	dB
12	Maximum output amplitude L	V13-5			O			O					300mV				13	Output DC measurement	—	—	−1.25	V
13	Maximum output amplitude H	V13-6		O				O					300mV				13	Output DC measurement	1.25	—	—	V
14	Offset voltage 1 (TE amplifier)	V11-1															11	Input resistance 390kΩ, Output DC measurement	−50	0	50	mV
15	Voltage gain 1	V11-2				O											11	Input 1kHz 240mVp-p, Output AC measurement	7.3	10.3	13.3	dB
16	Voltage gain 2	V11-3					O										11	Input 1kHz 240mVp-p, Output AC measurement	7.3	10.3	13.3	dB
17	Voltage gain difference	V11-4															11	V11-4 = V11-2 − V11-3	−3.0	0	3.0	dB
18	Maximum output amplitude H	V11-5				O		O					1V				11	Output DC measurement	1.25	—	—	V
19	Maximum output amplitude L	V11-6					O	O					1V				11	Output DC measurement	—	—	−1.25	V
20	Output voltage 1 (APC)	V2-1										450µA			2.7V	2.0V	2	Output DC measurement	−830	−330	170	mV
21	Output voltage 2	V2-2										570µA			2.7V	2.0V	2	Output DC measurement	470	970	1470	mV
22	Output voltage 3	V2-3										0µA			2.7V	0.5V	2	LD OFF, Output DC measurement	1400	1590	—	mV
23	Maximum output amplitude	V2-5	O								0.8mA	0µA			2.7V	2.0V	2	Output DC measurement	−600	—	100	mV

No.	Measurement item		Symbol	SW conditions								Bias conditions						Measurement pin	Description of I/O waveform and measurement method	Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	I1	I2	E1	E2	E3	E4						
24	RF level control	50% limit	V2-7		O	O							800µA	50mV		0.5V/2.7V	2.0V	2	Level control: 50% – Level control OFF	−1900	−1322	−100	mV
25		30% limit	V2-8		O	O							700µA	50mV		1.3V/2.7V	2.0V	2	Level control: 30% – Level control OFF	−1700	−1163	−200	mV
26		−50% limit	V2-9						O		O		230µA		800mV	0.5V/2.7V	2.0V	2	Level control: −50% – Level control OFF	700	1471	1900	mV
27		−30% limit	V2-10						O		O		320µA		800mV	2.2V/2.7V	2.0V	2	Level control: −30% – Level control OFF	700	1204	1700	mV
28	AGCCONT	High Level	V18-1															18		2.7	—	—	V
29		Middle Level	V18-2															18		1.3	—	2.2	V
30		Low Level	V18-3															18		—	—	0.5	V
31	Center output voltage		V10-1							O								10	Output DC measurement	−100	—	100	mV

Note) O in the SW conditions 7 represents the OFF state.

Electrical Characteristics Measurement Circuit
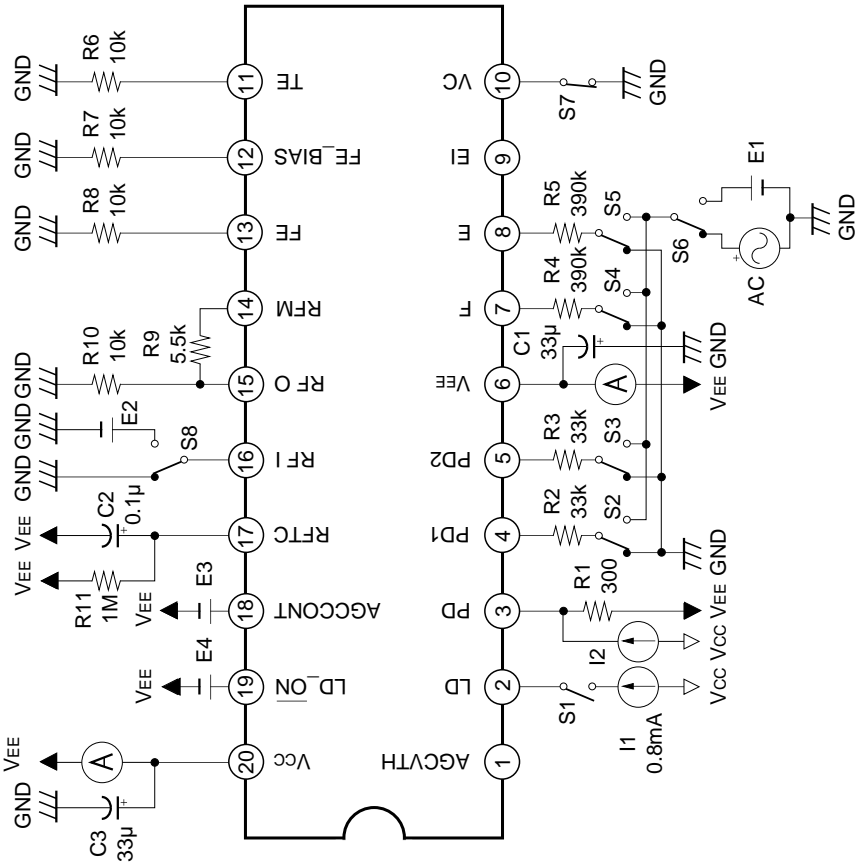
Description of Functions

RF Amplifier

The photodiode current input to the input pins (PD1, PD2) are current-to-voltage (I-V) converted by the equivalent resistance of 58kΩ at PD I-V amplifiers, respectively. The signal is added by the RF summing amplifier and then the I-V converted output voltage of the photodiode (A + B + C + D) is output to RFO pin. This pin is used check the eye pattern.
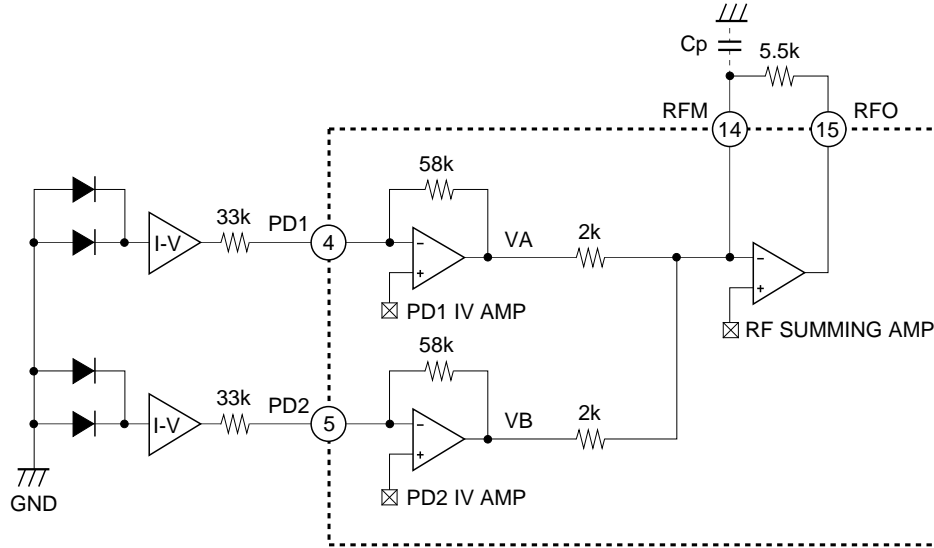
The frequency response of the RF output signal can be equalized by adding the capacitance (Cp) to RFI pin. The low frequency component of the RFO output voltage is as follows;

$$V_{RFO} = -2.75 \times (V_A + V_B)$$
$$= 159.5 \text{k}\Omega \times (i_{PD1} + i_{PD2})$$

Focus Error Amplifier

The difference between the RF I-V amplifier output VA and VB is obtained and the I-V converted voltage of the photodiode (A + C − B − D) is output.
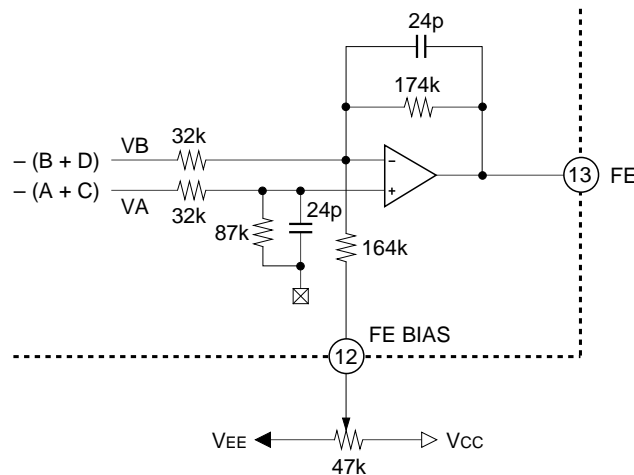
The FE output voltage (low frequency) is as follows;

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315 \text{k}\Omega$$

Tracking Error Amplifier

Each signal current from the photodiodes E and F is I-V converted and input to Pins 7 and 8 via a resistor which determines the gain. The signal is amplified by the gain amplifier, operated by the tracking error amplifier and then the (F-E) signal is output to Pin 11.
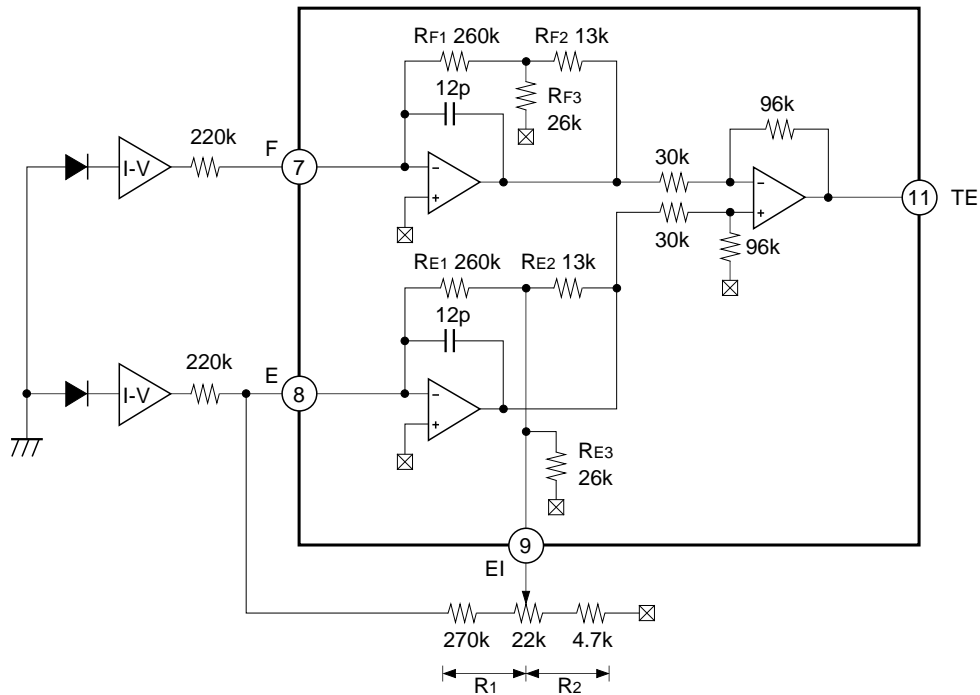
The balance adjustment is performed by varying the combined resistance value of the feedback resistors, which are T type-configured at the E I-V amplifier, by using the external resistance value of EI pin.

$$\text{F I-V amplifier feedback resistance value} = R_{F1} + R_{F2} + \frac{R_{F1} \times R_{F2}}{R_{F3}} = 403\text{k}\Omega$$

$$\text{E I-V amplifier feedback resistance value} = (R_{E1} \mathbin{/\!/} R_1) + R_{E2} + \frac{(R_{E1} \mathbin{/\!/} R_1) \times R_{E2}}{(R_{E3} \mathbin{/\!/} R_2)}$$

Leave EI pin open when the balance adjustment is not executed in this IC.
The gain for F I-V and E I-V amplifiers becomes the same when EI pin is left open.

Center Voltage Generation Circuit

This circuit provides the center potential when this IC is used at single power supply. The maximum current is approximately ±3mA. The output impedance is approximately 50Ω.
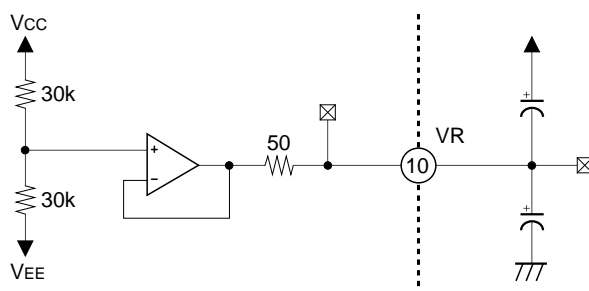
APC & Laser Power Control
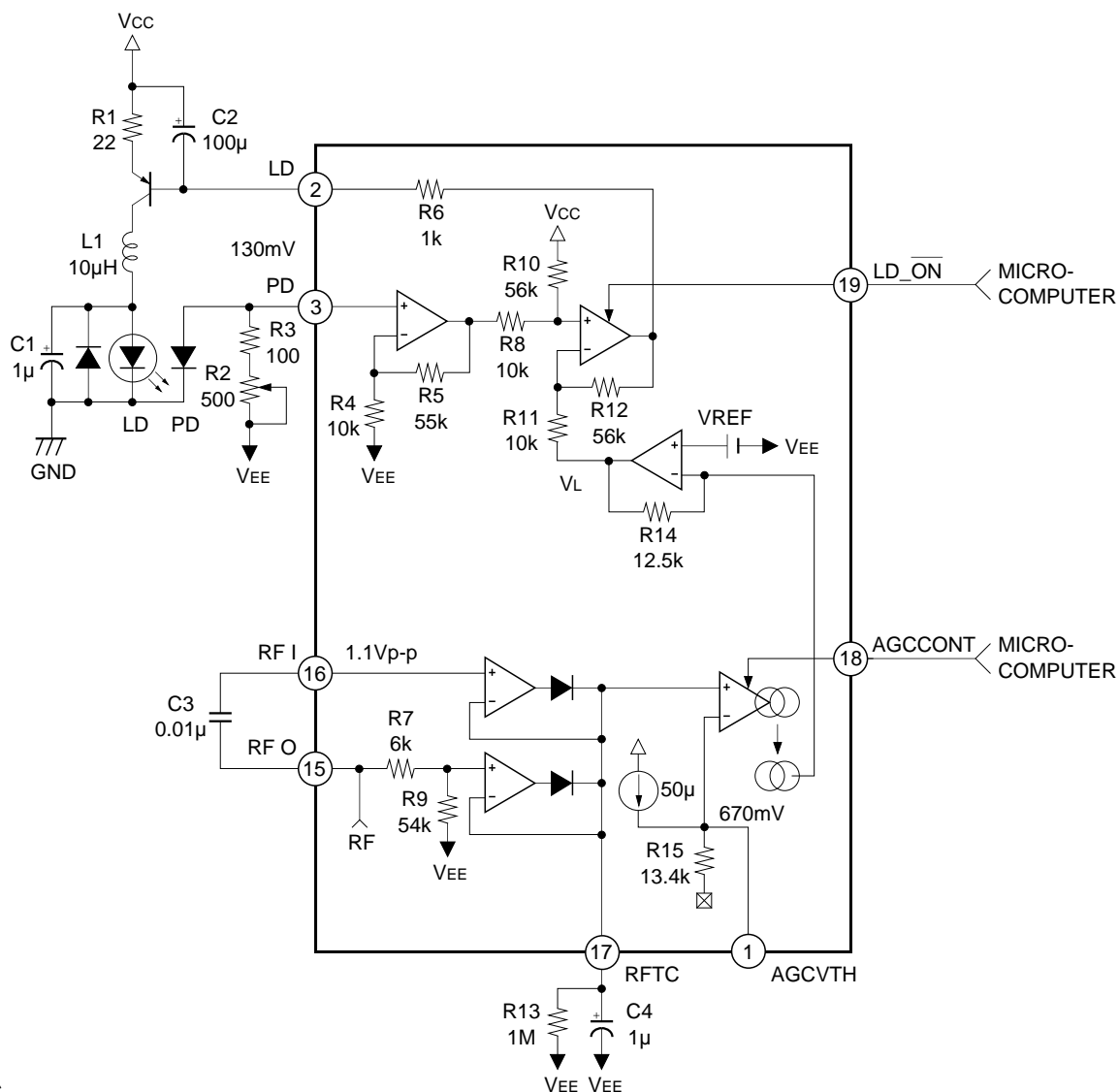
• APC

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. The APC circuit is used to maintain the optical power output at a constant level. The laser diode current is controlled according to the monitor photo diode output.

APC is set to ON by connecting the LD_$\overline{ON}$ pin to Vcc; OFF by connecting it to Vcc.

Application Circuit

• For single power supply +3.5V

• For dual power supply ±1.75V

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.
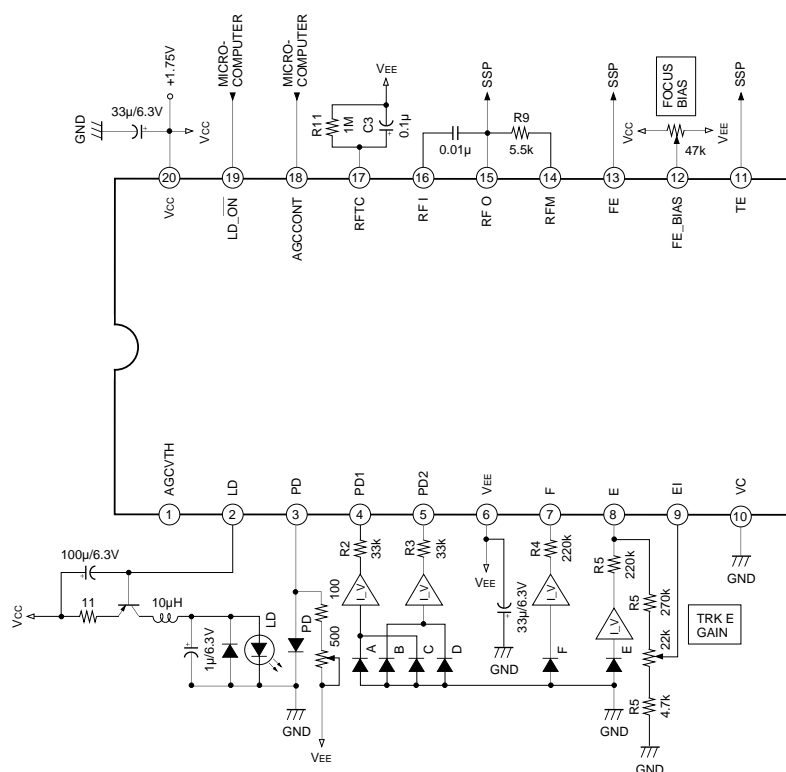
• LASER POWER CONTROL (LPC)

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations.

The RF O and RF I levels are compared and the larger of the two is smoothed by the RFTC's external CR.

This signal is then compared with the reference level.

The laser power is controlled by attaching an offset to V_L according to the results of comparison with the reference level.

Set the reference level to 670mV. (center voltage reference)

When the reference level is changed, connect the external resistor to the AGCVTH pin (Pin 1). The reference level can be lowered by connecting the resistor between Pin 1 and the center output voltage or between Pin 20 and V_{CC}.

The AGCCONT pin (pin 18) is used to switch the level of the laser power control circuit; OFF, ON (laser power limit of 30%) and ON (laser power limit of 50%)

Note) For the laser power limit, 50% is recommended for PD IC; 30% for LC.

AGCCONT	LPC	LPC limit	V_L variable range
H (V_{CC})	OFF	—	Approximately 1.27V
M (VC or OPEN)	ON	30%	Approximately 1.27V ± 350mV
L (V_{EE})	ON	50%	Approximately 1.27V ± 570mV

Notes on Operation

1. Power supply

The CXA2550M/N can be used either at dual power supply or single power supply. The table below shows the connection of power supply for each case.

	V_{CC}	V_{EE}	VC
Dual power supply	+power supply	−power supply	GND
Single power supply	Power supply	GND	OPEN

2. RF amplifier

In this circuit, the IC internal phase compensation value is set so as to support the voltage output-type pickup. Therefore, when the current output-type pickup is used, the capacitance of optical pickup and leads etc. are attached to PD1 and PD2 pins and oscillation may occur.

3. laser power control

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations. Therefore, use this circuit in the state where the focus servo is applied.

The laser life is shortened by increasing the laser power when the less light is reflected from the disc. It is recommended that the typical laser power value is set lower to maintain the laser life.

Take care of the laser maximum ratings when using the laser power control circuit.

Package Outline   Unit: mm

CXA2550M

20PIN SOP (PLASTIC) 300mil
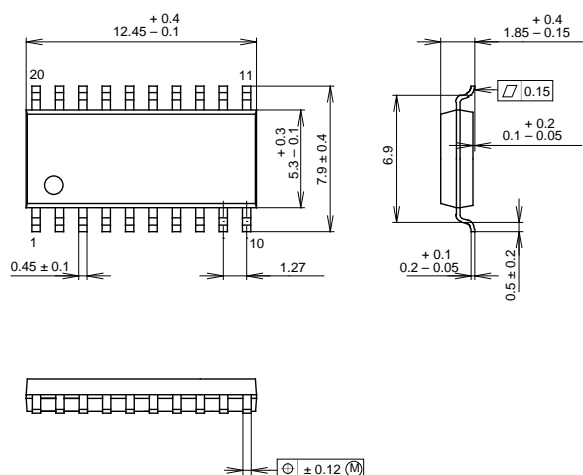
SONY CODE	SOP-20P-L01
EIAJ CODE	∗SOP020-P-0300-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

CXA2550N

20PIN SSOP (PLASTIC)

DETAIL **A**
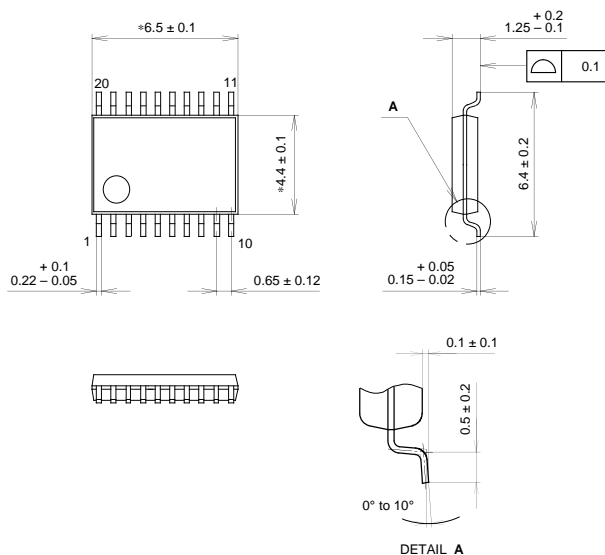
NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g

SONY

CXD3068Q

CD Digital Signal Processor with Built-in Digital Servo

Preliminary

80 pin QFP (Plastic)

Description

The CXD3068Q is a digital signal processor LSI for CD players. This LSI incorporates a digital servo.

Features

- All digital signal processings during playback are performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter free
  - 0.5× to 4× continuous playback possible
  - Allows relative rotational velocity readout
- Wide capture range playback mode
  - Spindle rotational velocity following method
  - Supports 1× to 4× playback variable pitch playback
- Bit clock, which strobes the EFM signal, is generated by the digital PLL.
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
  Supported during 4× playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub-Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface output
- Digital level meter, peak meter
- Bilingual supported
- VCO control mode
- CD TEXT data demodulation
- EFM playability reinforcement function

Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment function
- Surf jump function supporting micro two-axis
- Tracking filter: 6 stages
  Focus filter: 5 stages
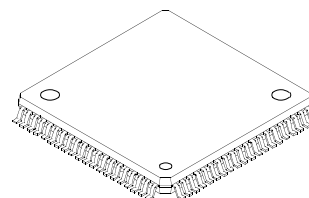
Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +4.6 V
- Input voltage V_I −0.5 to +4.6 V
  (V_{SS} − 0.5V to V_{DD} + 0.5V)
- Output voltage V_O −0.5 to +4.6 V
  (V_{SS} − 0.5V to V_{DD} + 0.5V)
- Storage temperature T_{stg} −55 to +150 °C
- Supply voltage difference
  V_{SS} − AV_{SS} −0.3 to +0.3 V
  V_{DD} − AV_{DD} −0.3 to +0.3 V

Note) AV_{DD} includes XV_{DD} and AV_{SS} includes XV_{SS}.

Recommended Operating Conditions

- Supply voltage V_{DD} 2.7 to 3.6 V
- Operating temperature
  T_{opr} −20 to +75 °C

I/O Capacitance

- Input pin C_I 9 (Max.) pF
- Output pin C_O 11 (Max.) pF
- I/O pin $C_{I/O}$ 11 (Max.) pF

Note) Measurement conditions $V_{DD} = V_I = 0V$
$f_M = 1MHz$

Block Diagram

Top pin labels: XTAI (71), XTAO (72), XTSL (69), V16M (29), VPCO (60), VCTL (58), XUGF (11), GFS (13), BMPH (68), WRCK (10), WDCK (17), C2PO (14), LRCK (65), PCMD (66), BCK (67), MUTE (3)

Right side: TES1 (37), TEST (36), XRST (2), MD2 (63), DOUT (64)

Left side pins:
- RSTO (27)
- C4M (18)
- RFAC (50)
- ASYI (49)
- ASYO (48)
- ASYE (62)
- BIAS (57)
- XPCK (12)
- FLO (53)
- FLI (54)
- PCO (55)
- CLTV (52)
- MDP (25)
- LOCK (24)
- PWM (23)
- SENS (7)
- DATA (4)
- XLAT (5)
- CLOK (6)
- SCOR (15)
- SBSO (79)
- EXCK (80)
- SCSY (78)
- SQSO (76)
- SQCK (77)
- RFDC (43)
- CE (42)
- TE (41)
- SE (40)
- FE (39)
- VC (38)
- IGEN (46)

Blocks:
- Clock Generator
- Asymmetry Corrector
- Digital PLL
- Digital CLV
- CPU Interface
- EFM demodulator
- Error Corrector
- 32K RAM
- Sub Code Processor
- D/A Interface
- Digital OUT
- Servo Auto Sequencer
- OP Amp Analog SW
- A/D Converter
- SERVO Interface
- MIRR DFCT FOK
- SERVO DSP: FOCUS SERVO, TRACKING SERVO, SLED SERVO
- PWM GENERATOR: FOCUS PWM GENERATOR, TRACKING PWM GENERATOR, SLED PWM GENERATOR

Signal processor block

Servo block

Right side lower pins:
- SOUT (73)
- SOCK (74)
- XOLT (75)
- SCLK (8)
- COUT (19)
- SSTP (26)
- ATSK (9)
- MIRR (20)
- DFCT (21)
- FOK (22)
- FFDR (33)
- FRDR (34)
- TFDR (31)
- TRDR (32)
- SFDR (29)
- SRDR (30)

Bottom: AVDD (44)

Pin Configuration

Top (pins 60–41): VPCO (60), V16M (59), VCTL (58), BIAS (57), AVDD1 (56), PCO (55), FILI (54), FILO (53), CLTV (52), AVSS1 (51), RFAC (50), AGY1 (49), AGYO (48), AVDD0 (47), IGEN (46), AVSS0 (45), ADIO (44), RFDC (43), CE (42), TE (41)

Left (pins 61–80): DVDD2 (61), AGYE (62), MD2 (63), DOUT (64), LRCK (65), PCMD (66), BCK (67), EMPH (68), XTSL (69), DVSS2 (70), XTAI (71), XTAO (72), SOUT (73), SOCK (74), XOLT (75), SQSO (76), SQCK (77), SCSY (78), SBSO (79), EXCK (80)

Right (pins 40–21): SE (40), FE (39), VC (38), TES1 (37), TEST (36), DVSS1 (35), FRDR (34), FFDR (33), TRDR (32), TFDR (31), SRDR (30), SFDR (29), DVDD1 (28), RSTO (27), SSTP (26), MDP (25), LOCK (24), PWMI (23), FOK (22), DFCT (21)

Bottom (pins 1–20): DVDD0 (1), XRST (2), MUTE (3), DATA (4), XLAT (5), CLOK (6), SENS (7), SCLK (8), ATSK (9), WRDK (10), XUGF (11), XPCK (12), GFS (13), C2PO (14), SCOR (15), C4M (16), WRCK (17), DVSS0 (18), COUT (19), MIRR (20)

Pin Description

Pin No.	Symbol	I/O		Description
1	DV$_{DD}$0	—		Digital power supply.
2	XRST	I		System reset. Reset when low.
3	MUTE	I		Mute input (low: off, high: on)
4	DATA	I		Serial data input from CPU.
5	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
6	CLOK	I		Serial data transfer clock input from CPU.
7	SENS	O	1, 0	SENS output to CPU.
8	SCLK	I		SENS serial data readout clock input.
9	ATSK	I/O	1, 0	Anti-shock input/output.
10	WFCK	O	1, 0	WFCK output.
11	XUGF	O	1, 0	XUGF output. MNT0 or RFCK is output by switching with the command.
12	XPCK	O	1, 0	XPCK output. MNT1 is output by switching with the command.
13	GFS	O	1, 0	GFS output. MNT2 or XROF is output by switching with the command.
14	C2PO	O	1, 0	G2PO output. MNT3 or GTOP is output by switching with the command.
15	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
16	C4M	O	1, 0	4.2336MHz output. 1/4 frequency division output for V16M in CAV-W mode or variable pitch mode.
17	WDCK	O	1, 0	Word clock output. f = 2Fs. GRSCOR is output by the command switching.
18	DV$_{SS}$0	—	—	Digital GND.
19	COUT	I/O	1, 0	Track count signal I/O.
20	MIRR	I/O	1, 0	Mirror signal I/O.
21	DFCT	I/O	1, 0	Detect signal I/O.
22	FOK	I/O	1, 0	Focus OK signal I/O.
23	PWMI	I		Spindle motor external control input.
24	LOCK	I/O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Input when LKIN = 1.
25	MDP	O	1, Z, 0	Spindle motor servo control output.
26	SSTP	I		Disc innermost track detection signal input.
27	FSTO	O	1, 0	2/3 frequency division output for XTAI pin.
28	DV$_{DD}$1	—	—	Digital power supply.
29	SFDR	O	1, 0	Sled drive output.
30	SRDR	O	1, 0	Sled drive output.
31	TFDR	O	1, 0	Tracking drive output.
32	TRDR	O	1, 0	Tracking drive output.
33	FFDR	O	1, 0	Focus drive output.

Pin No.	Symbol	I/O		Description
34	FRDR	O	1, 0	Focus drive output.
35	DVss1	—	—	Digital GND.
36	TEST	I		Test. Normally, GND.
37	TES1	I		Test. Normally, GND.
38	VC	I		Center voltage input.
39	FE	I		Focus error signal input.
40	SE	I		Sled error signal input.
41	TE	I		Tracking error signal input.
42	CE	I		Center servo analog input.
43	RFDC	I		RF signal input.
44	ADIO	O	Analog	Test. No connected.
45	AVss0	—	—	Analog GND.
46	IGEN	I		Constant current input for operational amplifier.
47	AVDD0	—	—	Analog power supply.
48	ASYO	O	1, 0	EFM full-swing output. (low = Vss, high = VDD)
49	ASYI	I		Asymmetry comparator voltage input.
50	RFAC	I		EFM signal input.
51	AVss1	—	—	Analog GND.
52	CLTV	I		Multiplier VCO1 control voltage input.
53	FILO	O	Analog	Master PLL filter output (slave = digital PLL).
54	FILI	I		Master PLL filter input.
55	PCO	O	1, Z, 0	Master PLL charge pump output.
56	AVDD1	—	—	Analog power supply.
57	BIAS	I		Asymmetry circuit constant current input.
58	VCTL	I		Wide-band EFM PLL VCO2 control voltage input.
59	V16M	I/O	1, 0	Wide-band EFM PLL VCO2 oscillation output. Serves as wide-band EFM PLL clock input by switching with the command.
60	VPCO	O	1, Z, 0	Wide-band EFM PLL charge pump output.
61	DVDD2	—	—	Digital power supply.
62	ASYE	I		Asymmetry circuit on/off (low = off, high = on).
63	MD2	I		Digital Out on/off control (low = off, high = on).
64	DOUT	O	1, 0	Digital Out output.
65	LRCK	O	1, 0	D/A interface. LR clock output. f = Fs
66	PCMD	O	1, 0	D/A interface. Serial data output (two's complement, MSB first).
67	BCK	O	1, 0	D/A interface. Bit clock output.

Pin No.	Symbol	I/O		Description
68	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
69	XTSL	I		Crystal selection input. Low when the crystal is 16.9344MHz; high when it is 33.8688MHz.
70	DVss2	—	—	Digital GND.
71	XTAI	I		Crystal oscillation circuit input. When the master clock is input externally, input it from this pin.
72	XTAO	O		Crystal oscillation circuit output.
73	SOUT	O	1, 0	Serial data output in servo block.
74	SOCK	O	1, 0	Serial data readout clock output in servo block.
75	XOLT	O	1, 0	Serial data latch output in servo block.
76	SQSO	O	1, 0	Sub-Q 80-bit, PCM peak or level data outputs. CD TEXT data output.
77	SQCK	I		SQSO readout clock input.
78	SCSY	I		GRSCOR resynchronization input.
79	SBSO	O	1, 0	Sub-Q P to W serial output.
80	EXCK	I		SBSO readout clock input.

Notes)
- PCMD is a MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs. (during normal speed)
- C2PO represents the data error status.
- XROF is generated when the 32K RAM exceeds the ±28F jitter margin.

Combination of Monitor Pin Outputs

Command bit		Output data			
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT0	MNT1	MNT2	MNT3
1	0	RFCK	XPCK	XROF	GTOP

Electrical Characteristics

1. DC Characteristics $(V_{DD} = AV_{DD} = 3.3 \pm 0.3V, V_{SS} = AV_{SS} = 0V, Topr = -20 \text{ to } +75°C)$

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH1}		$0.7V_{DD}$			V	*1, *9
	Low level	V_{IL1}				$0.2V_{DD}$	V	
Input voltage (2)	High level	V_{IH2}	$V_I \le 5.5V$	$0.8V_{DD}$			V	*2
	Low level	V_{IL2}				$0.2V_{DD}$	V	
Input voltage (3)	High level	V_{IH3}	$V_I \le 5.5V$ Schmitt input	$0.8V_{DD}$			V	*3
	Low level	V_{IL3}				$0.2V_{DD}$	V	
Input voltage (4)		V_{IN4}	Analog input	V_{SS}		V_{DD}	V	*4, *5
Output voltage (1)	High level	V_{OH1}	$I_{OH} = -4mA$ $I_{OL} = 4mA$	$V_{DD} - 0.4$		V_{DD}	V	*6, *8, *9
	Low level	V_{OL1}		0		0.4	V	
Output voltage (2)	High level	V_{OH2}	$I_{OH} = -0.28mA$ $I_{OH} = 0.36mA$	$V_{DD} - 0.5$		V_{DD}	V	*7
	Low level	V_{OL2}		0		0.4	V	
Input leak current (1)		I_{LI1}	$V_I = V_{SS}$ or V_{DD}	−10		10	µA	*1, *4
Input leak current (2)		I_{LI2}	$V_I = 0$ to $5.5V$	−10		10	µA	*2, *3
Input leak current (3)		I_{LI3}	$V_I = V_{SS}$ or V_{DD}	−40		40	µA	*9
Input leak current (4)		I_{LI4}	$V_I = 0.25V_{DD}$ to $0.75V_{DD}$	−40		40	µA	*5
Tri-state pin output leak current		I_{LO}	$V_I = V_{SS}$ or V_{DD}	−40		40	µA	*8

1-1. Applicable pins and classification

*1 CMOS level input pins:
   TEST, TES1
*2 CMOS level input pins:
   MUTE, SCSY, PWMI, DATA, XLAT, SSTP, XTSL
*3 CMOS Schmitt input pins:
   ASYE, EXCK, V16M, SQCK, XRST, CLOK, SCLK
*4 Analog input pins (1):
   VCTL, ASYI, CLTV, FILI
*5 Analog input pins (2):
   VC, FE, SE, TE, CE, RFDC
*6 Normal output pins (1):
   V16M, SQSO, C4M, WDCK, FSTO, SOUT, SOCK, XOLT, FSTO, SQSO, WFCK, XUGF, XPCK, GFS,
   C2PO, SCOR, SFDR, SRDR, TFDR, TRDR, FRDR, ASYO, DOUT, LRCK, PCMD, BCK, EMPH
*7 Normal output pin (2):
   FILO
*8 Tri-state output pins:
   VPCO, SENS, MDP, FFDR, PCO
*9 Normal input/output pins:
   ATSK, COUT, MIRR, DFCT, FOK, LOCK

Note) When the external pull-down resistors are connected to the pins *2 and *3, the resistance applied to these pins should be 5kΩ or less in total.

2. AC Characteristics

(1) XTAI pin

(a) When using self-excited oscillation

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTAI pin

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	V_{DD} − 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns
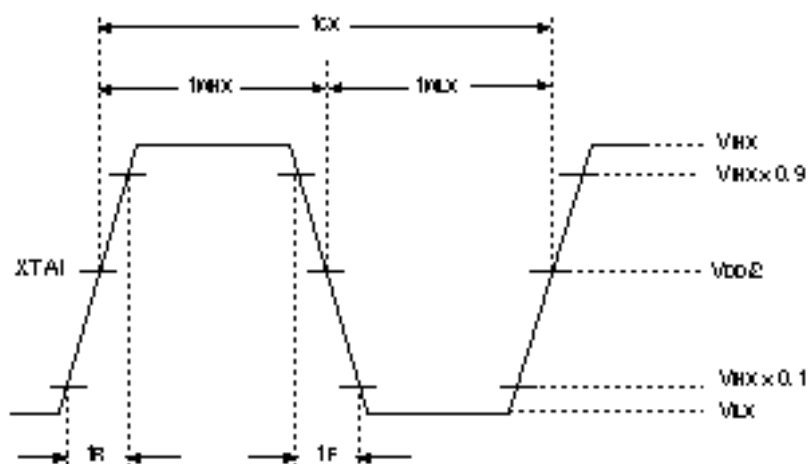
(c) When inputting sine waves to XTAI pin via a capacitor

(Topr = −20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

(2) CLOK, DATA, XLAT, SQCK and EXCK pins

(V_{DD} = AV_{DD} = 3.3 ± 0.3V, V_{SS} = AV_{SS} = 0V, T_{opr} = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65 **Note)**	MHz
EXCK SQCK pulse width	t_{WT}	750 **Note)**			ns
COUT frequency (for input) *	f_T			65	kHz
COUT pulse width (for input) *	t_{WT}	7.5			µs

* Only when $44 and $45 are executed.
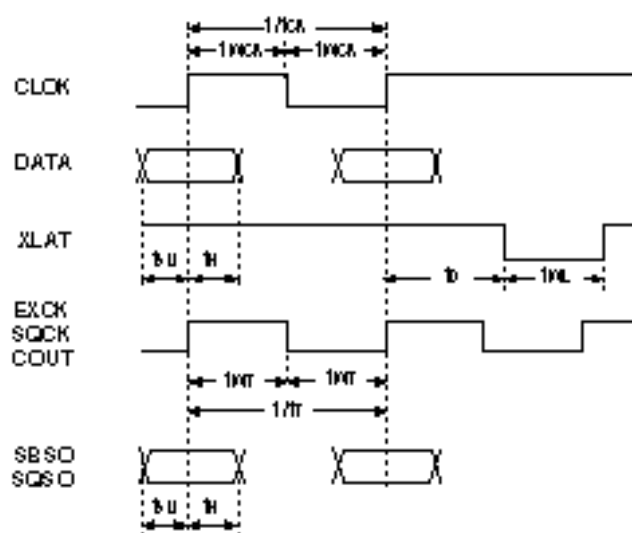
Note) In quasi double-speed playback mode, except when SQSO is Sub Q Read, the SQCK maximum operating frequency is 300kHz and its minimum pulse width is 1.5µs.

(3) SCLK pin
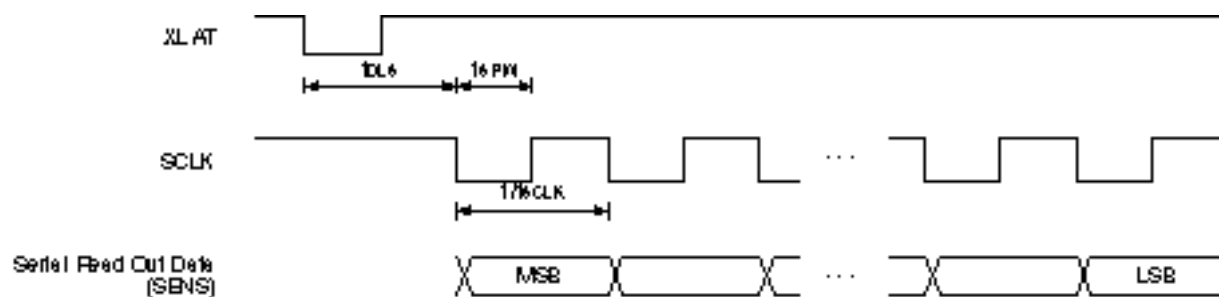
Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	fSCLK			16	MHz
SCLK pulse width	tSPW	31.3			ns
Delay time	tDLS	15			μs

(4) COUT, MIRR and DFCT pins

Operating frequency (VDD = AVDD = 3.3 ± 0.3V, VSS = AVSS = 0V, Topr = −20 to +75°C)

Signal	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	fCOUT	40			kHz	*1
MIRR maximum operating frequency	fMIRR	40			kHz	*2
DFCT maximum operating frequency	fDFCTH	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2
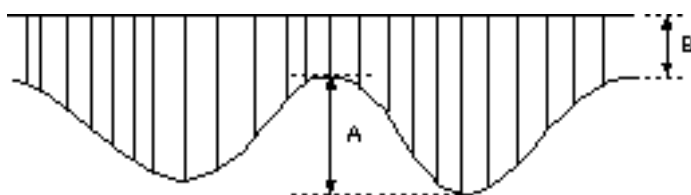
When the RF signal continuously satisfies the following conditions during the above traverse.

- A = 0.11VDD to 0.23VDD

- $\dfrac{B}{A + B} \leq 25\%$

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

Contents

Explanation of abbreviations   AVRG: Average
            AGCNTL: Auto gain control
            FCS: Focus
            TRK: Tracking
            SLD: Sled
            DFCT: Defect

[1] CPU Interface

§ 1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below.
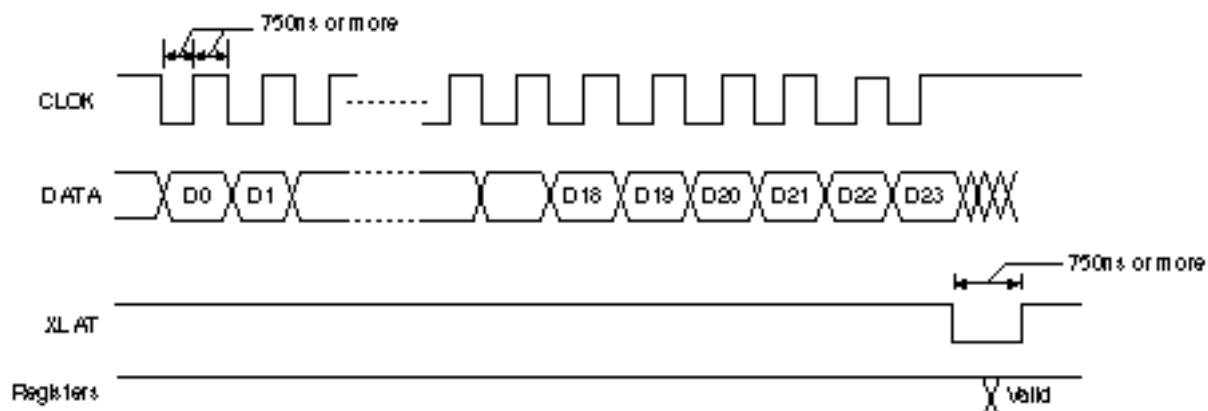
• The internal registers are initialized by a reset when XRST = 0.

Note) Be sure to set SQCK to high when XLAT is low.

§ 1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8 bits
3	8 to 24 bits
4 to 6	16 bits
7	20 bits
8	28 bits
9	28 bits
A	28 bits
B	24 bits
C	28 bits
D	20 bits
E	20 bits

Command Table ($0X to 1X)

Reg-ister	Command	Address D23 to D20	Data 1 D19	D18	D17	D16	Data 2 D15	D14	D13	D12	Data 3 D11	D10	D9	D8	Data 4 D7	D6	D5	D4	Data 5 D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			0	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			0	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEACH VOLTAGE UP
1	TRACKING CONTROL	0 0 0 1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
			—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don't care

Command Table ($2X to 3X)

Reg-ister	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Reg-ister	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL ($\pm 1 \times$ basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL ($\pm 2 \times$ basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL ($\pm 3 \times$ basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL ($\pm 4 \times$ basic value)

—: Don't care

Command Table ($340X)

Reg-ister	Command	Address 1 D23 to D20	Address 2 D19 to D16	Address 3 D15 to D12	Address 4				Data 1				Data 2				
					D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Reg-ister	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Command Table ($342X)

Reg-ister	Command	Address 1 D23 to D20	Address 2 D19 to D16	Address 3 D15 to D12	Address 4 D11	D10	D9	D8	Data 1 D7	D6	D5	D4	Data 2 D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) NOT USED

Command Table ($343X)

Register	Command	Address 1 D23 to D20	Address 2 D19 to D16	Address 3 D15 to D12	Address 4 D11	D10	D9	D8	Data 1 D7	D6	D5	D4	Data 2 D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) SLED INPUT GAIN (when TGup2 is accessed with SFSK = 1)
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) NOT USED
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) NOT USED

Command Table ($344X)

Reg-ister	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 1 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) TRACKING HOLD INPUT GAIN (when TGup2 is accessed with THSK = 1)
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) NOT USED
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) NOT USED

Command Table ($348X to 34FX)

Reg-ister	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
							1	0	0	0	PGFS1	PGFS0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0	PGFS, PFOK, RFAC
							1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
							1	1	0	0	THBON	FHBON	TLB1ON	FLB1ON	TLB2ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0	Booster
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	0	IDFSL3	IDFSL2	IDFSL1	IDFSL0	0	0	IDFT1	IDFT0	0	0	0	0	

	Address 2				Data 1		Data 2				Data 3				
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
					1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—	FCS Bias Limit
	1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FCS Bias Data
					0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	Traverse Center Data

—: Don't care

Command Table ($35X to 3FX)

Register	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23 D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0011	1	1	1	1	1	0	0	0	SYG3	SYG2	SYG1	SYG0	FI FZB3	FI FZB2	FI FZB1	FI FZB0	FI FZA3	FI FZA2	FI FZA1	FI FZA0	System GAIN

Register	Command	Address					Data 1				Data 2				Data 3				Data 4				
		D23 D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0	FCS search, AGF
			0	1	1	0	TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0	TRK jump, AGT
			0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT	FZC, AGC, SLD move
			1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0	DC measure, cancel
			1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0	Serial data read out
			1	0	1	0	0	FBON	FBSS	FBUP	FBV1	FBV0	FIFZC	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0	FCS Bias, Gain, Surf jump/brake
			1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0	Mirr, DFCT, FOK
			1	1	0	0	COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0	TZC, Cout, Bottom, Mirr
			1	1	0	1	SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0	SLD filter
			1	1	1	0	F1NM	F1DM	F3NM	F3DM	TINM	TIUM	T3NM	T3UM	DF1S	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D	Filter
			1	1	1	1	0	AGC4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	0	0	AGHF	ASOT	Clock, others

Note) Be sure to set D4 (Data2) of $3F to 1 for CXD3068Q.

Command Table ($4X to EX)

Register	Command	Address D3	D2	D1	D0	Data1 D3	D2	D1	D0	Data2 D3	D2	D1	D0	Data3 D3	D2	D1	D0	Data4 D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0				
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	TR3	TR2	TR1	TR0	0	0	0	0	0	0	0	0				
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	0	0	0	0				
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT0	VCO SEL2	KSL3	KSL2	KSL1	KSL0	0	VCO1 CS0	XVCO2 THRU	0
9	Function specification	1	0	0	1	1	DSPB ON/OFF	ASEQ ON/OFF	1	BiliGL MAIN	BiliGL SUB	FLFC	1	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	PCT1	PCT2	0	SOC2	0	0	0	0	0	1	0	0
A	EFM playability reinforcement setting					1	0	1	1	ARDTEN	1	1	1	1	0	1	0	0	0	1	0
A	Sync expanding specification					1	1	0	0	AVW	0	SFP5	SFP4	SFP3	SFP2	SFP1	SFP0				
A	Sleep setting					1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP								
A	Variable pitch					1	1	1	0	VARI ON	VARI USE	0	0								
B	Traverse monitor counter setting	1	0	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0	SFP3	SFP2	SFP1	SFP0	SRP3	SRP2	SRP1	SRP0
D	CLV CTRL	1	1	0	1	0	TB	TP	CLVS Gain	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0
E	SPD mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	0	INV VPCO

Don't care

CXD3068Q

Reg-ister	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5 D7	D6	D5	D4	Data 6 D3	D2	D1	D0	Data 7 D3	D2	D1	D0
8	MODE specification	1 0 0 0					ERC4	SCOR SEL	SCSY	SOCT1	TXON	TXOUT	OUTL1	OUTL0	—	—	—	—
9	Function specification	1 0 0 1					0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1 0 1 0	0 0 ∗ ∗				0	0	0	0	0	0	0	0	—	—	—	—
A	EFM playability reinforcement setting		1 0 1 1				1	0	0	0	0	0	0	0	1	0	0	0
B	Traverse monitor counter setting	1 0 1 1					0	0	MTSL1	MTSL0	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0					EDC7	EDC6	EDC5	EDC4	EDC3	EDC2	EDC1	EDC0	—	—	—	—

§ 1-3. CPU Command Presets

—: Don't care

Command Preset Table ($0X to 34X)

Reg-ister	Command	Address D23 to D20	Data 1 D19	D18	D17	D16	Data 2 D15	D14	D13	D12	Data 3 D11	D10	D9	D8	Data 4 D7	D6	D5	D4	Data 5 D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF

Reg-ister	Command	Address D23 to D20	Data 1 D19	D18	D17	D16	Data 2 D15	D14	D13	D12	Data 3 D11	D10	D9	D8	Data 4 D7	D6	D5	D4	Data 5 D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)

Reg-ister	Command	Address 1 D23 to D20	D19	D18	D17	D16	Address 2 D15	D14	D13	D12	Address 3 D11	D10	D9	D8	Data 1 D7	D6	D5	D4	Data 2 D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	1	0	0	0									See "Coefficient ROM Preset Values Table".							KRAM DATA ($3400XX to $344fXX)

—: Don't care

SONY

CXD3068Q

Command Preset Table ($348X to 34FX)

Reg-ister	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
							1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGFS, PFOK, RFAC
							1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
							1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Booster
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
							Address 2				Data 1				Data 2				Data 3				
							D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
											1	0	0	0	0	0	0	0	0	0	0	0	FCS Bias Limit
							1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	FCS Bias Data
											0	0	0	0	0	0	0	0	0	0	0	0	Traverse Center Data

Command Preset Table ($35X to 3FX)

SONY

Reg-ister	Command	Address1					Address2				Data1				Data2				Data3				
		D23 D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0011	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	System GAIN

Reg-ister	Command	Address					Data1				Data2				Data3				Data4				
		D23 D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	FCS search, AGF
			0	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	TRK jump, AGT
			0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0	FZC, AGC, SLD move
			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DC measure, cancel
			1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Serial data read out
			1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FCS Bias, Gain, Surf jump/brake
			1	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	Mirr, DFCT, FOK
			1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	TZC, Cout, Bottom, Mirr
			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLD filter
			1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Filter
			1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Clock, others

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CXD3068Q

Command Preset Table ($4X to EX)

Reg-ister	Command	Address D3	D2	D1	D0	Data1 D3	D2	D1	D0	Data2 D3	D2	D1	D0	Data3 D3	D2	D1	D0	Data4 D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0				
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0				
7	Auto sequence(N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0
A	EFM playability reinforcement setting					1	0	1	1	0	1	1	1	1	0	1	0	0	0	1	0
A	Sync expanding specification					1	1	0	0	0	0	0	0	1	1	0	0				
A	Sleep setting					1	1	0	1	0	0	0	0								
A	Variable pitch					1	1	1	0	0	0	0	0								
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Spindle servo coefficient setting	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
D	CLV CTRL	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
E	SPD mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Don't care

Command Preset Table ($4X to EX)

Reg-ister	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6				Data 7			
							D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
8	MODE specification	1 0 0 0					0	0	0	0	0	0	0	0	—	—	—	—
9	Function specification	1 0 0 1					0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1 0 1 0	0 0 * *				0	0	0	0	0	0	0	0	—	—	—	—
	EFM playability reinforcement setting		1 0 1 1				0	0	0	0	0	0	0	0	0	0	0	0
B	Traverse monitor counter setting	1 0 1 1					0	0	0	0	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0					0	0	0	0	0	0	0	0	—	—	—	—

—: Don't care

SONY

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

* Fix indicates that normal preset values should be used.

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

§ 1-4. Description of SENS Signals

SENS output

Microcomputer serial register (latching not required)	ASEQ = 0	ASEQ = 1	Output data length
$0X	Z	FZC	—
$1X	Z	AS (Anti Shock)	—
$2X	Z	TZC	—
$30 to 37	Z	SSTP	—
$38	Z	AGOK*	—
$38	Z	XAVEBSY*	—
$3904	Z	TE Avrg Reg.	9 bits
$3908	Z	FE Avrg Reg.	9 bits
$390C	Z	VC Avrg Reg.	9 bits
$391C	Z	TRVSC Reg.	9 bits
$391D	Z	FB Reg.	9 bits
$391F	Z	RFDC Avrg Reg.	8 bits
$3A	Z	FBIAS Count STOP	—
$3B to 3F	Z	SSTP	—
$4X	Z	XBUSY	—
$5X	Z	FOK	—
$6X	Z	0	—
$AX	GFS	GFS	—
$BX	COMP	COMP	—
$CX	COUT	COUT	—
$EX	$\overline{OV64}$	$\overline{OV64}$	—
$7X, 8X, 9X, DX, FX	Z	0	—

* $38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

SENS output	
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COMP	Counts the number of tracks set with Reg.B. High when Reg.B is latched, low when the initial Reg.B number is counted through COUT.
COUT	Counts the number of tracks set with Reg.B. High when Reg.B is latched, toggles each time the Reg.B number is counted through COUT. While $44 and $45 are being executed, toggles with each COUT 8-count instead of the Reg.B number.
$\overline{\text{OV64}}$	Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-On	0	1	1	1
1 Track Jump	1	0	0	RXF
10 Track Jump	1	0	1	RXF
2N Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0   Forward

RXF = 1   Reverse

• When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.

• When the Track jump commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

MAX timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

• To disable the MAX timer, set the MAX timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequencer track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

This command is used to set N when a 2N-track jump is executed, to set M when an M-track move is executed and to set the jump count when fine search is executed for auto sequencer.

• The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.

• When the track jump count is from 0 to 15, the COUT signal is counted for 2N-track jumps and M-track moves; when the count is 16 or over, the MIRR signal is counted. For fine search, the COUT signal is counted.

$8X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
MODE specification	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT0	VCO SEL2

Command bit	C2PO timing	Processing
CDROM = 1	1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital Out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital Out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital Out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital Out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output for 48-bit slot
0	0	0	0	OFF	0dB
0	0	0	1	OFF	0dB
0	0	1	0	OFF	0dB
0	0	1	1	OFF	0dB
0	1	0	0	OFF	−∞dB
0	1	0	1	OFF	−∞dB
0	1	1	0	OFF	−∞dB
0	1	1	1	OFF	−∞dB
1	0	0	0	0dB	0dB
1	0	0	1	0dB	−∞dB
1	0	1	0	−∞dB	0dB
1	0	1	1	−∞dB	−∞dB
1	1	0	0	−∞dB	−∞dB
1	1	0	1	−∞dB	−∞dB
1	1	1	0	−∞dB	−∞dB
1	1	1	1	−∞dB	−∞dB

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Function
ASHS = 0	The command transfer rate to DSSP block from auto sequencer is set to normal speed.
ASHS = 1	The command transfer rate to DSSP block from auto sequencer is set to half speed.

* See "§ 4-8. Playback Speed" for settings.

Command bit		Processing
SOCT0	SOCT1	
0	—	Sub-Q is output from the SQSO pin.
1	0	Each signal is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-4.)
1	1	The error rate is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-6.)

—: Don't care

Command	Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	VCO SEL1	ASHS	SOCT0	VCO SEL2	KSL3	KSL2	KSL1	KSL0

See the previous page.

Command bit	Processing
VCOSEL1 = 0	Multiplier PLL VCO1 is set to normal speed.
VCOSEL1 = 1	Multiplier PLL VCO1 is set to approximately twice the normal speed.

Command bit		Processing
KSL3	KSL2	
0	0	Output of multiplier PLL VCO1 is 1/1 frequency-divided.
0	1	Output of multiplier PLL VCO1 is 1/2 frequency-divided.
1	0	Output of multiplier PLL VCO1 is 1/4 frequency-divided.
1	1	Output of multiplier PLL VCO1 is 1/8 frequency-divided.

Command bit	Processing
VCOSEL2 = 0	Wide-band PLL VCO2 is set to normal speed.
VCOSEL2 = 1	Wide-band PLL VCO2 is set to approximately twice the normal speed.

Command bit		Processing
KSL1	KSL0	
0	0	Output of wide-band PLL VCO2 is 1/1 frequency-divided.
0	1	Output of wide-band PLL VCO2 is 1/2 frequency-divided.
1	0	Output of wide-band PLL VCO2 is 1/4 frequency-divided.
1	1	Output of wide-band PLL VCO2 is 1/8 frequency-divided.

Command	Data 4				Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Mode specification	0	VCO1 CS0	VCO2 THRU	0	ERC4	SCOR SEL	SCSY	SOCT1	TXON	TXOUT	OUTL1	OUTL0

Command bit	Processing
VCO2 THRU = 0	V16M is output.
VCO2 THRU = 1	The wide-band EFM PLL clock can be input from the V16M pin.

* These bits select the internal or external connection for the VCO2 used in CAV-W or variable pitch mode.

Command bit	Processing
ERC4 = 0	C2 error double correction is performed when DSPB = 1.
ERC4 = 1	C2 error quadruple correction is performed even when DSPB = 1.

Command bit	Processing
SCOR SEL = 0	WDCK signal is output.
SCOR SEL = 1	GRSCOR (protected SCOR) is output.

* Used when outputting GRSCOR from the WDCK pin.

Command bit	Processing
SCSY = 0	No processing.
SCSY = 1	GRSCOR (protected SCOR) synchronization is applied again.

* Used to resynchronize GRSCOR.

The rising edge signal of this commnd bit is used internally. Therefore, when resynchronizing GRSCOR, first return the setting to 0 and then set to 1.

GRSCOR achieves the crystal accuracy by removing the jitter components included in the SCOR signal. This signal is synchronized with PCMDATA.

The resynchronization conditions are when GTOP = high or when the SCSY pin = high.

(same as when SCSY = 1 is sent by the $8X command.)

Command bit	Processing
TXON = 0	When CD TEXT data is not demodulated, set TXON to 0.
TXON = 1	When CD TEXT data is demodulated, set TXON to 1.

* See "$4-10. CD TEXT Data Demodulation"

Command bit	Processing
TXOUT = 0	Various signals except for CD TEXT is output from the SQSO pin.
TXOUT = 1	CD TEXT data is output from the SQSO pin.

* See "$4-10. CD TEXT Data Demodulation"

Command bit	Processing
OUTL1 = 0	WFCK, XPCK C4M, WDCK and FSTO are output. V16M is output when VCO2 THRU = 0.
OUTL1 = 1	WFCK, XPCK C4M, WDCK and FSTO outputs are set to low. The V16M output is low when VCO2 THRU = 0.

Command bit	Processing
OUTL0 = 0	PCMD, BCK, LRCK and EMPH are output.
OUTL0 = 1	PCMD, BCK, LRCK and EMPH outputs are low.

Command bit	Processing
VCO1CS0 = 0	Multiplier PLL VCO1 low speed is selected.
VCO1CS0 = 1	Multiplier PLL VCO1 high speed is selected.

* The CXD3068Q has two VCO1s, and this command selects one of these VCO1s.

* **Block Diagram of VCO Internal Path**
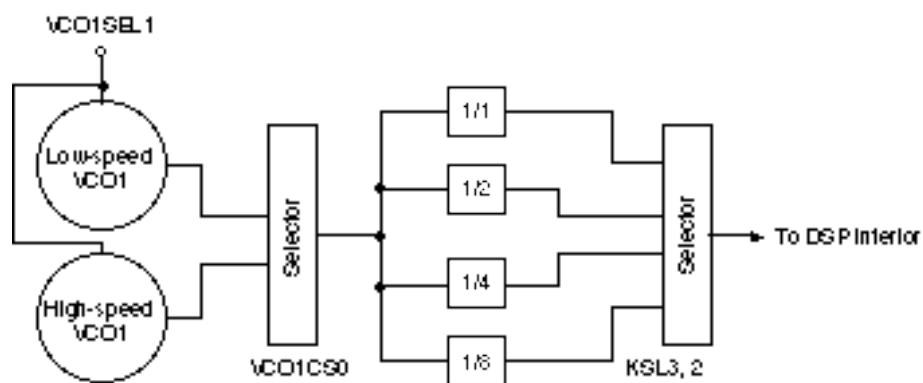
VCO1 Internal Path

$9X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Function specification	1	DSPB ON-OFF	A.SEQ ON-OFF	1	BiliGL MAIN	BiliGL SUB	FLFC	1

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error quadruple correction.
DSPB = 1	Double-speed playback, C2 error double correction. (quadruple correction when ERC4 = 1)

FLFC is normally 0.

FLFC is 1 in CAV-W mode, for any playback speed.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

$AX commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Audio CTRL	VARI ON	VARI USE	Mute	ATT	PCT1	PCT2	0	SOC2

Command bit	Processing
VARION = 0	Variable pitch mode is turned off. (The crystal is the reference to the internal clock.)
VARION = 1	Variable pitch mode is turned on. (The VCO2 is the reference to the internal clock.)

Command bit	Processing
VARIUSE = 0	When the variable pitch mode is not used, set VARIUSE to 0 .
VARIUSE = 1	When the variable pitch mode is used, set VARIUSE to 1.

* See "$DX commands" for the variable range and the usage example of the variable pitch.

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off.
ATT = 1	−12dB

Mute conditions

    (1) When register A mute = 1.
    (2) When Mute pin = 1.
    (3) When register 8 D.out Mute F = 1 and the Digital Out is on (MD2 pin = 1).
    (4) When GFS stays low for over 35 ms (during normal-speed).
    (5) When register 9 BiliGL MAIN = Sub = 1.
    (6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1ms time limit.

Command bit		Meaning	PCM Gain	ECC error correction ability
PCT1	PCT2			
0	0	Normal mode	$\times$ 0dB	C1: double; C2: quadruple
0	1	Level meter mode	$\times$ 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	$\times$ 0dB	C1: double; C2: double

Description of level meter mode (see Timing Chart 1-4.)
• When the LSI is set to this mode, it performs digital level meter functions.
• When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits are Sub-Q data (see "§ 2. Subcode Interface"). The last 16 bits are LSB first, which are 15-bit PCM data (absolute values) and an L/R flag.
  The L/R flag is high when the 15-bit PCM data is from the left channel and low when the data is from the right channel.
• The PCM data is reset and the L/R flag is reversed after one readout.
  Then maximum value measuring continues until the next readout.

Description of peak meter mode (see Timing Chart 1-5.)
- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the value is set in the LSI internal register again.
  In other words, the PCM maximum value detection register is not reset by the readout.
- To reset the PCM maximum value register to zero, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub-Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level ($-\infty$) for this mode.

Command bit	Processing
SOC2 = 0	The SENS signal is output from the SENS pin as usual.
SOC2 = 1	The SQSO pin signal is output from the SENS pin.

SENS output switching
- This command enables the SQSO pin signal to be output from the SENS pin.
  When SOC2 = 0, SENS output is performed as usual.
  When SOC2 = 1, the SQSO pin signal is output from the SENS pin.
  At this time, the readout clock is input to the SCLK pin.

Note) SOC2 should be switched when SQCK = SCLK = high.

$AB commands (preset: $AB7A28)

Command	Data 1				Data 2				Data 3				Data 4				Data 5			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
EFM playability reinforcement function	1	0	1	1	ARDTEN	1	1	1	1	0	1	0	0	0	1	0	1	0	0	0

Command	Data 6				Data 7			
	D3	D2	D1	D0	D3	D2	D1	D0
EFM playability reinforcement function	0	0	0	0	1	0	0	0

Command bit	Processing
ARDTEN = 0	Normal playback is performed.
ARDTEN = 1	EFM playability reinforcement function is turned on.

Note) Set these command bits when the disc is not played back.

$AC commands (preset: $AC0C)

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Sync expanding bit	1	1	0	0	AVW	0	SFP5	SFP4	SFP3	SFP2	SFP1	SFP0

Command bit	Processing
AVW = 0	Automatic expanding function of sync protection window width is turned off.
AVW = 1	Automatic expanding function of sync protection window width is turned on.

* During the period from 16th forward protection to the GFS rise, the sync protection window width (±6 channel clocks when WSEL = 0 and ±26 channel clocks when WSEL = 1) expands by 32 channel clocks whenever the inserted sync is generated. GTOP rises when the window width becomes maximum (in excess of 588 channel clocks).

Note) The sync forward protection times are not affected by SFP5 to SFP0.

Command bit	Processing
SFP5 to 0	Sets the frame sync forward protection times. The setting range is 1F to 3F (Hex).

* See "§4-2. Frame Sync Protection" for the protection of the frame sync.

Note) This command bit register is shared with the $CX commands and the command bit set last is valid. When the command bit is used in the existing state, set to the $CX commands. When the command bit is used with the $AC address, make the settings same as for SFP3 to SFP0 set with the $CX commands.

$AD commands (preset: $AD0)

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
AD (Sleep setting)	1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP

ADCPS: This bit sets the operating mode of the DSSP block A/D converter.

When 0, the operating mode of the DSSP block A/D converter is set to normal. (default)

When 1, the operating mode of the DSSP block A/D converter is set to power saving.

DSP SLEEP: This bit sets the operating mode of the DSP block.

When 0, the DSP block operates normally. (default)

When 1, the DSP block clock is stopped. This makes it possible to reduce power consumption.

DSSP SLEEP: This bit sets the operating mode of the DSSP block.

When 0, the DSSP block operates normally. (default)

When 1, the DSSP block clock is stopped. In addition, the A/D converter and operational amplifier in the DSSP block are set to standby mode. This makes it possible to reduce power consumption.

ASYM SLEEP: This bit sets the operating mode of the asymmetry correction circuit and VCO1.

When 0, the asymmetry correction circuit and VCO1 operate normally. (default)

When 1, the operational amplifier in the asymmetry correction circuit is set to standby mode. In addition, the multiplier PLL VCO1 oscillation is stopped. This makes it possible to reduce power consumption.

$AE commands (preset: $AE0)

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Audio CTRL	1	1	1	0	VARI ON	VARI USE	0	0

Command bit	Processing
VARION = 0	Variable pitch mode is turned off. (The crystal is the reference to the internal clock.)
VARION = 1	Variable pitch mode is turned on. (The VCO2 is the reference to the internal clock.)

Command bit	Processing
VARIUSE = 0	When the variable pitch mode is not used, set VARIUSE to 0.
VARIUSE = 1	When the variable pitch mode is used, set VAIRUSE to 1.

* See "$DX commands" for the variable range and the usage example of the variable pitch.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

• When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
• The traverse monitor count is set to monitor the traverse status from the SENS output as COMP and COUT.

This command sets the monitor output switching.

Command	Data 5			
	D3	D2	D1	D0
Traverse monitor count setting	0	0	MTSL1	MTSL0

Command bit		Output data			
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT0	MNT1	MNT2	MNT3
1	0	RFCK	XPCK	XROF	GTOP

$CX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0
CLV CTRL ($DX)				Gain CLVS				

• CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	−12dB
0	0	1	−6dB
0	1	0	−6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP : GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	−6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	−6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV1	Gain DCLV0	GDCLV
0	0	0dB
0	1	+6dB
1	0	+12dB

Command bit		Processing
PCC1	PCC0	
0	0	The VPCO signal is output.
0	1	The VPCO pin output is high impedance.
1	0	The VPCO pin output is low.
1	1	The VPCO pin output is high.

• This command controls the VPCO pin signal.

The VPCO output can be controlled with this setting.

Command	Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	SFP3	SFP2	SFP1	SFP0	SRP3	SRP2	SRP1	SRP0

Command bit	Processing
SFP3 to 0	Sets the frame sync forward protection times. The setting range is 1 to F (Hex).

Command bit	Processing
SRP3 to 0	Sets the frame sync backward protection times. The setting range is 1 to F (Hex).

* See "§ 4-2. Frame Sync Protection" regarding frame sync protection.

• The CXD3068Q can serially output the 40 bits (10 BCD codes) of error monitor data selected by EDC0 to 7 from the SQSO pin and monitor this data using a microcomputer.
The C1 and C2 error rate settings are sent one at a time by the $C commands by setting $8 commands SOCT0 and SOCT1 = 1. Then, the data can be read out from the SQSO pin by sending 40 SQCK pulses.

$CX commands

Command	Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	EDC7	EDC6	EDC5	EDC4	EDC3	EDC2	EDC1	EDC0

Error monitor commands

Command bit		Processing
EDC7 = 0	EDC6	The [No C1 errors, pointer reset] count is output when 0.
	EDC5	The [One C1 error corrected, pointer reset] count is output when 0.
	EDC4	The [No C1 errors, pointer set] count is output when 0.
	EDC3	The [One C1 error corrected, pointer set] count is output when 0.
	EDC2	The [Two C1 errors corrected, pointer set] count is output when 0.
	EDC1	The [C1 correction impossible, pointer set] count is output when 0.
	EDC0	7350 frame count cycle mode[1] when 1. 73500 frame count cycle mode[2] when 0.
EDC7 = 1	EDC6	The [No C2 errors, pointer reset] count is output when 0.
	EDC5	The [One C2 error corrected, pointer reset] count is output when 0.
	EDC4	The [Two C2 errors corrected, pointer reset] count is output when 0.
	EDC3	The [Three C2 errors corrected, pointer reset] count is output when 0.
	EDC2	The [Four C2 errors corrected, pointer reset] count is output when 0.
	EDC1	The [C2 correction impossible, pointer copy] count is output when 0.
	EDC0	The [C2 correction impossible, pointer set] count is output when 0.

[1] The number selected by C1 (EDC1 to 6) and C2 (EDC0 to 6) is added to C1 and C2 and output every 7350 frames.

[2] The number selected by C1 (EDC1 to 6) and C2 (EDC0 to 6) is added to C1 and C2 and output every 73500 frames.

$DX commands

Command	Data 1			
	D3	D2	D1	D0
CLV CTRL	0	TB	TP	Gain CLVS

└── See "$CX commands".

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS mode.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS mode.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command	Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0

The settings are as follows in CAV-W mode.

Command bit	Processing
VP0 to 7	The spindle rotational velocity is set.

Command bit		Processing
VPCTL1	VPCTL0	
0	0	The setting of VP0 to 7 is multiplied by 1.
0	1	The setting of VP0 to 7 is multiplied by 2.
1	0	The setting of VP0 to 7 is multiplied by 3.
1	1	The setting of VP0 to 7 is multiplied by 4.

* The above setting should be 0, 0 except for the CAV-W operating mode.

The rotational velocity R of the spindle can be expressed with the following equation.

R: Relative velocity at normal speed = 1

$$R = \frac{256 - n}{32} \times l$$

n: VP0 to 7 setting value

l: Multiple set by VPCTL0, 1

Command bit	Description
VP0 to 7 = F0 (H)	Playback at 1/2 (1) × speed
⋮	⋮
VP0 to 7 = E0 (H)	Playback at 1 (2) × speed
⋮	⋮
VP0 to 7 = C0 (H)	Playback at (4) × speed

Notes)

1. Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.

2. The values in parentheses are for when DSPB is 1.
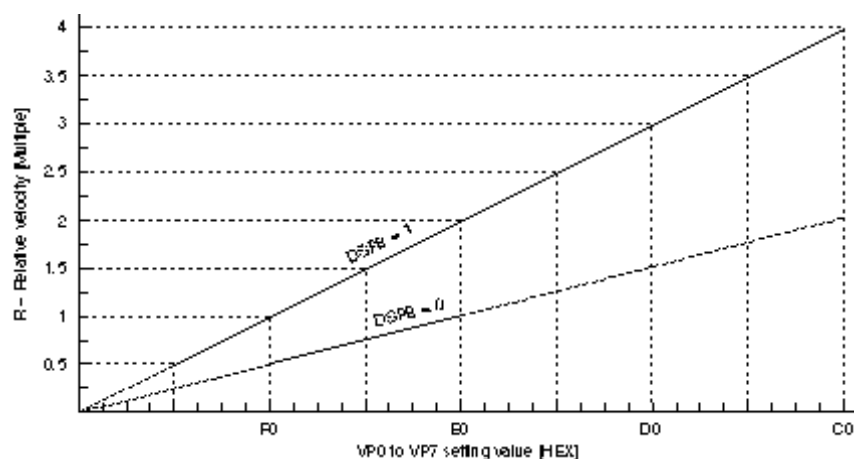
The setting in variable pitch mode is as shown below.

Command bit	Processing
VPCTL1 to 0, VP7 to 0	The pitch of variable pitch mode is set.

The setting of the pitch can be expressed with the equation below.

$$P = \frac{-n}{10} \ [\%]$$

P: Setting value of pitch

n: Setting value for VPCTL1, VPCTL0 and VP7 to VP0 (two's complementary, VPCTL1 is sign bit)

Command bit			Setting value of pitch [%]	Example of command setting
VPCTL1	VPCTL0	VP7 to 0		
1	0	00 (H)	+51.2	$D60080
		:	:	:
		FF (H)	+25.7	$D6FF80
1	1	00 (H)	+25.6	$D600C0
		:	:	:
		FF (H)	+0.1	$D6FFC0
0	0	00 (H)	0.0	$D60000
		:	:	:
		FF (H)	−25.5	$D6FF00
0	1	00 (H)	−25.6	$D60040
		:	:	:
		FF (H)	−48.7	$D6E740

The setting range of the pitch is −48.7 to +51.2%.

The pitch setting for + side should be within the playback speed of the recommended operating conditions.

The following is the example of the command in variable pitch mode.

$EX001	(Sets to CLV-N mode. The INV VPCO is set to 1.)
$AE4XX	(Sets to use variable pitch mode)
WAIT	(Wait time for VCO2 pull-in: until VCTL stabilizes.)
$AECXX	(Variable pitch mode is turned on. The VCO2 is the reference to the internal clock.)
$D60A00	(The pitch is set to -1.0%)
$D60000	(The pitch is set to 0.0%)
$AE4XX	(Variable pitch mode is turned off. The crystal is the reference to the internal clock.)

$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
SPD mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.[1]
1	0	0	0	KICK	Spindle forward rotation mode.[1]
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.[1]
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

[1] See Timing Charts 1-6 to 1-12.

Command bit									Mode	Description
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	INV VPCO		
0	0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	0	CLV-W	Used for playback in CLV-W mode.[2]
0	1	1	0	0	1	0	1	0	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	0	CAV-W	Spindle control with the external PWM.
0	0	0	0	0	1	0	1	1	VCO-C	VCO control[3]

[2] Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

[3] Fig. 3-3 shows the control flow with the microcomputer software in VCO-C mode.

Mode	LPWR	Command	Timing chart
CLV-N	0	KICK	1-6 (a)
		BRAKE	1-6 (b)
		STOP	1-6 (c)
CLV-W	0	KICK	1-7 (a)
		BRAKE	1-7 (b)
		STOP	1-7 (c)
	1	KICK	1-8 (a)
		BRAKE	1-8 (b)
		STOP	1-8 (c)
CAV-W	0	KICK	1-9 (a)
		BRAKE	1-9 (b)
		STOP	1-9 (c)
	1	KICK	1-10 (a)
		BRAKE	1-10 (b)
		STOP	1-10 (c)

Mode	LPWR	Timing chart
CLV-N	0	1-11
CLV-W	0	1-12
	1	1-13
CAV-W	0	1-14 (EPWM = 0)
	1	1-15 (EPWM = 0)
	0	1-16 (EPWM = 1)
	1	1-17 (EPWM = 1)

Command	Data 4			
	D3	D2	D1	D0
SPD mode	Gain CAV1	Gain CAV0	0	INV VPCO

Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	−6dB
1	0	−12dB
1	1	−18dB

• This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

SONY

LRCK

WDCK

48 bit slot

CDRDM= 0

C2PO

Rch 16bit C2 Pointer

Lch 16bit C2 Pointer

If C2 Pointer = 1,
data is NG

CDRDM= 1

C2PO

C2 Pointer for upper 8bits

C2 Pointer for lower 8bits

C2 Pointer for upper 8bits

C2 Pointer for lower 8bits

Rch C2 Pointer

Lch C2 Pointer

Level Meter Timing

Peak Meter Timing
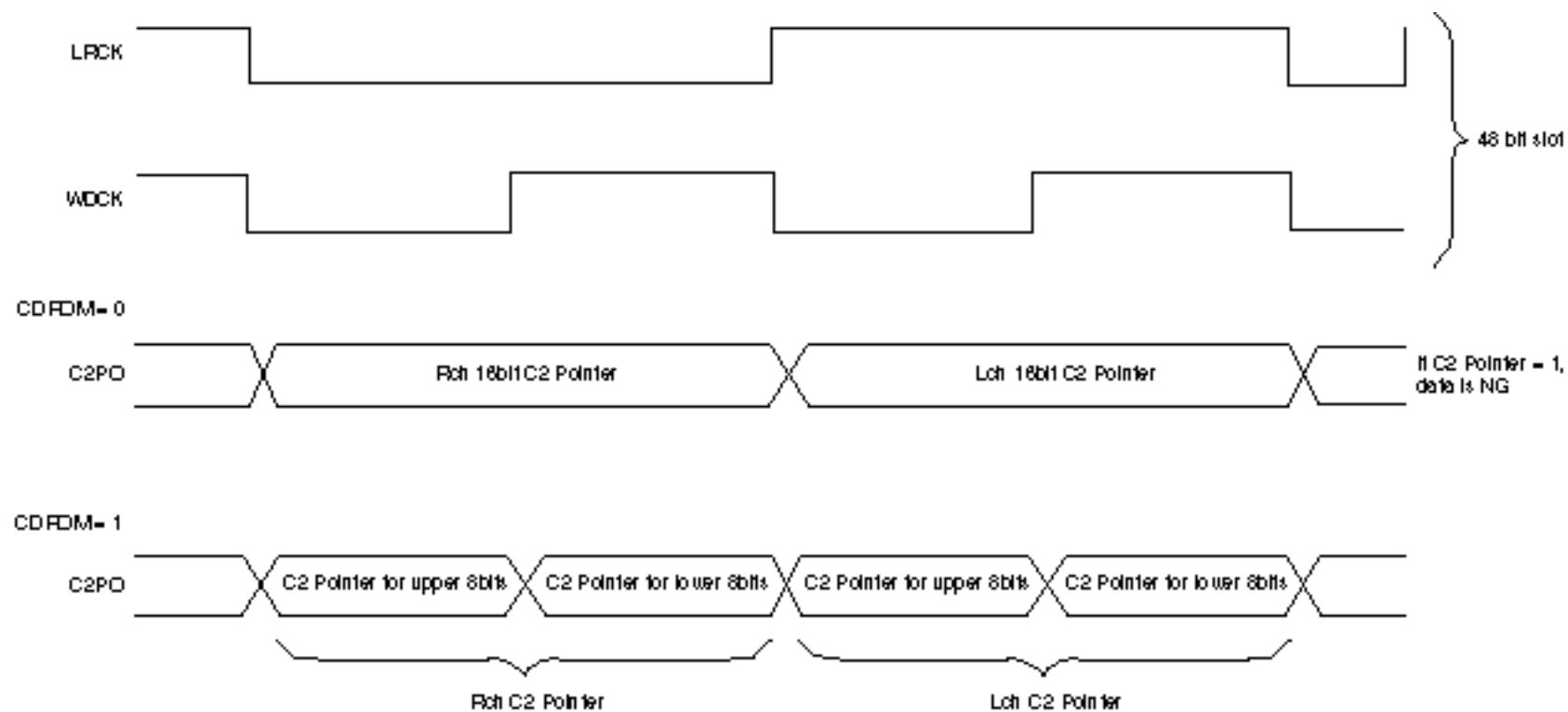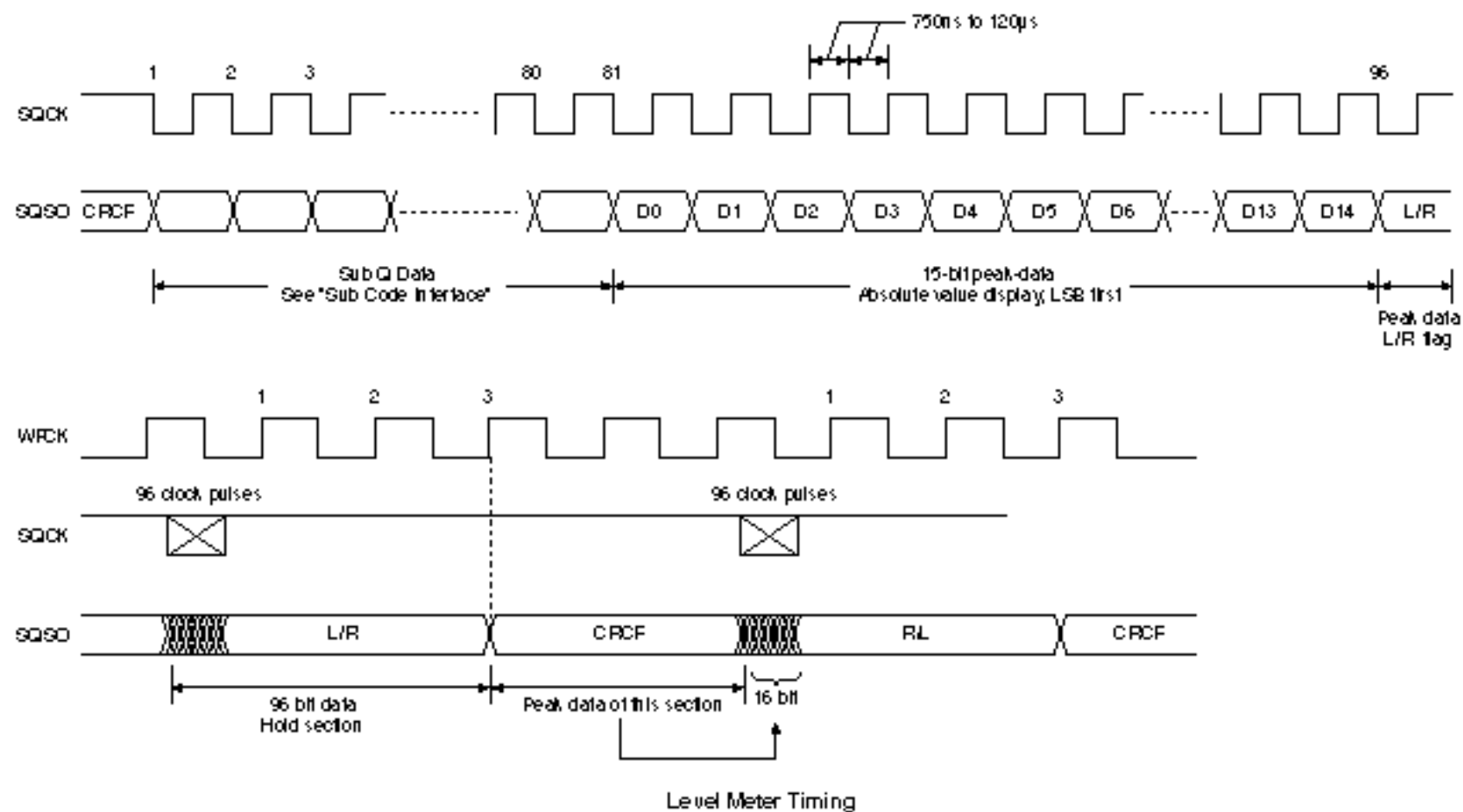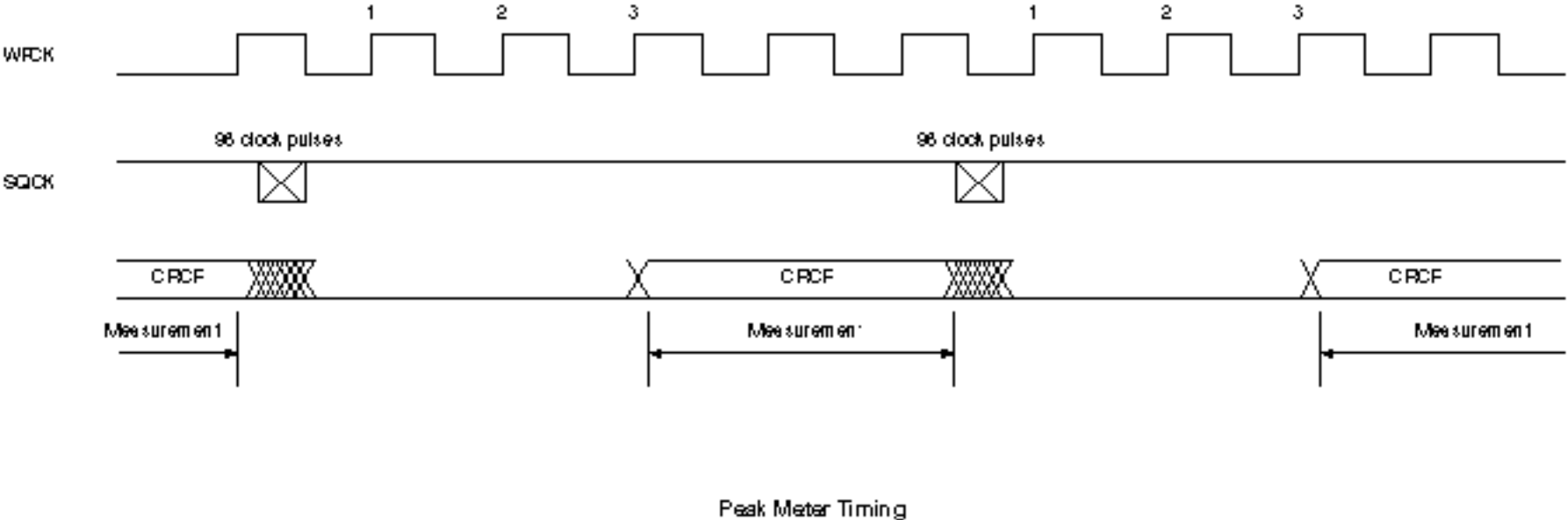
Timing Chart 1-6
CLV-N mode   LPWR = 0

(a) KICK   (b) BRAKE   (c) STOP
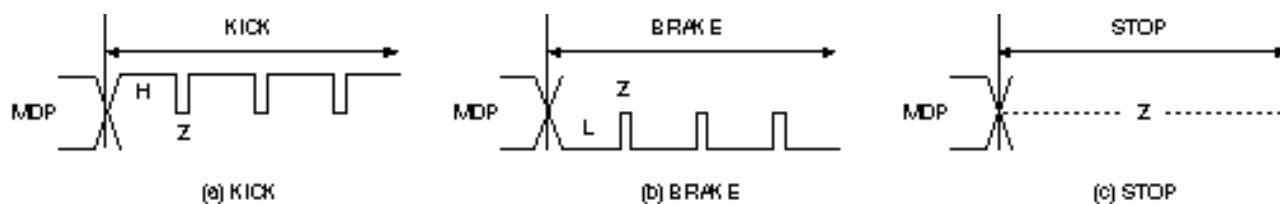
Timing Chart 1-7
CLV-W mode (when following the spindle rotational velocity)   LPWR = 0

(a) KICK   (b) BRAKE   (c) STOP
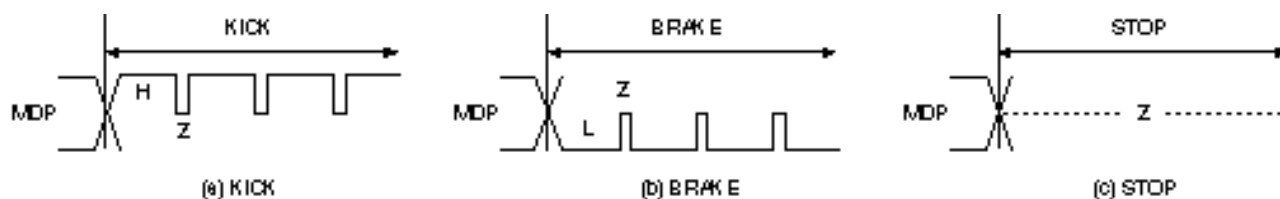
Timing Chart 1-8
CLV-W mode (when following the spindle rotational velocity)   LPWR = 1

(a) KICK   (b) BRAKE   (c) STOP
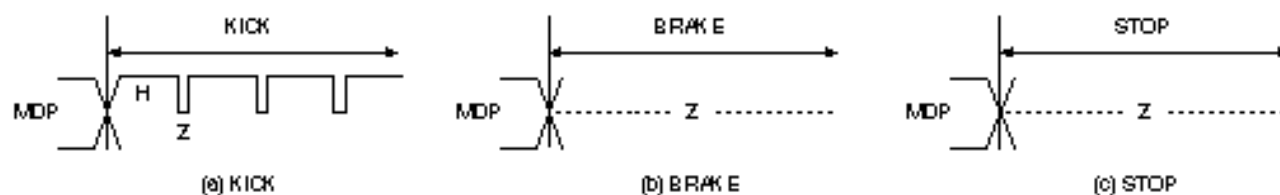
Timing Chart 1-9
CAV-W mode   LPWR = 0

(a) KICK   (b) BRAKE   (c) STOP
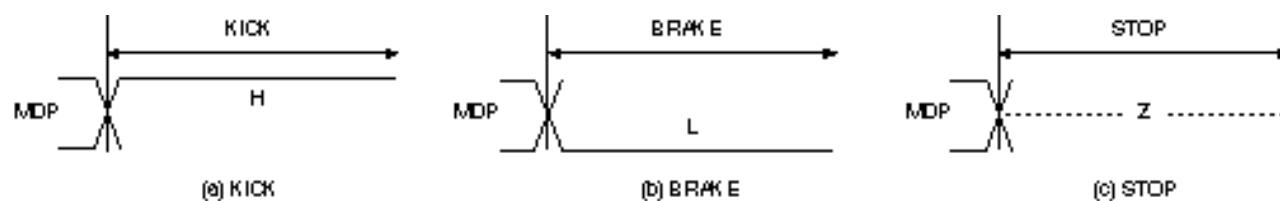
Timing Chart 1-10
CAV-W mode   LPWR = 1

(a) KICK   (b) BRAKE   (c) STOP
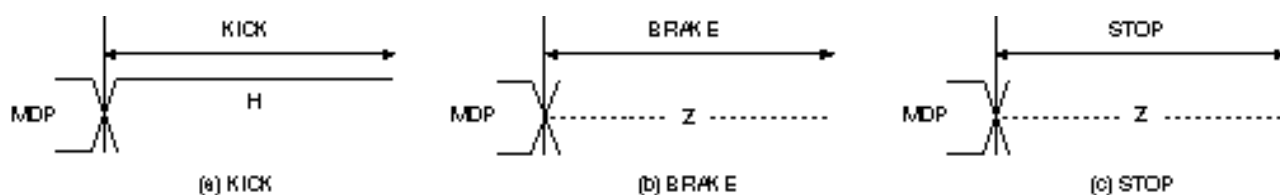
Timing Chart 1-11
CLV-N mode   LPWR = 0
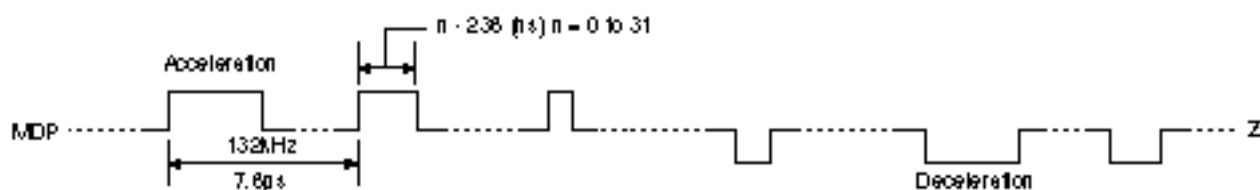
Timing Chart 1-12
CLV-W mode   LPWR = 0

Timing Chart 1-13
CLV-W mode   LPWR = 1

The BRAKE pulse is masked when LPWR = 1.
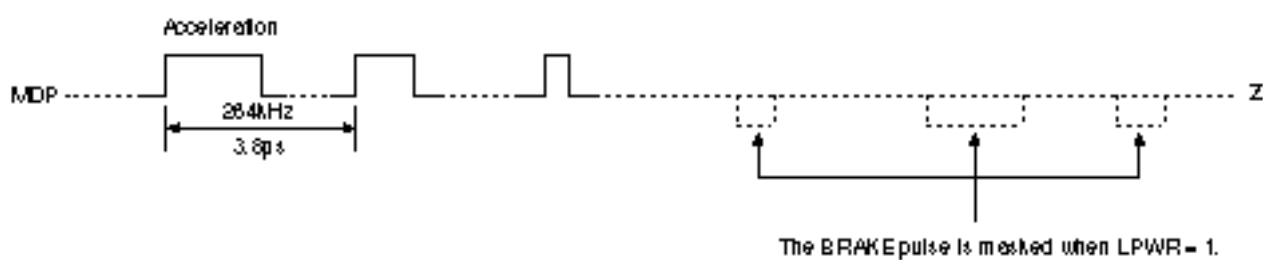
Timing Chart 1-14
CAV-W mode   EPWM = LPWR = 0
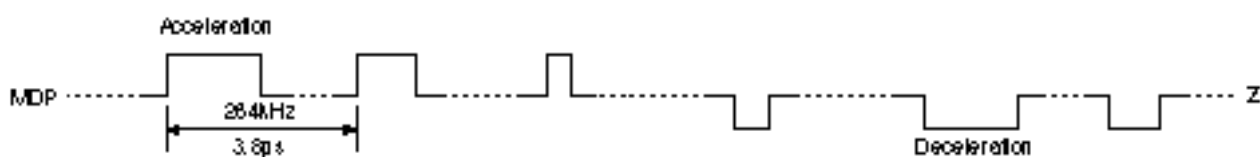
Timing Chart 1-15
CAV-W mode   EPWM = LPWR = 1

The BRAKE pulse is masked when LPWR = 1.
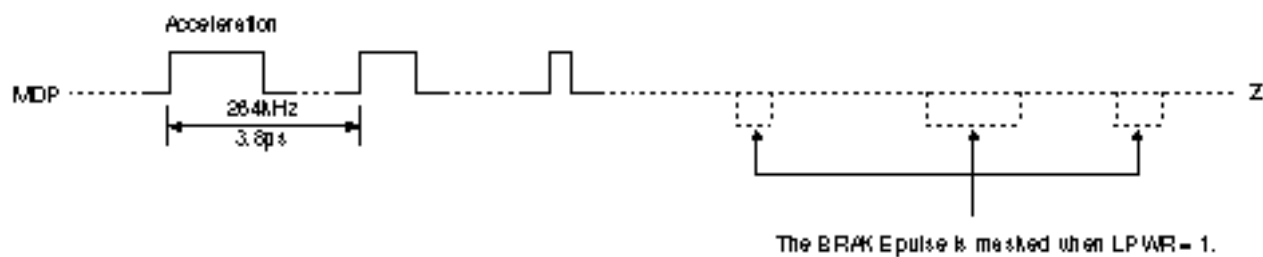
Timing Chart 1-16

CAV-W mode EPWM = 1, LPWR = 0

PWM

H

L

MDP

H

L

Acceleration

Deceleration
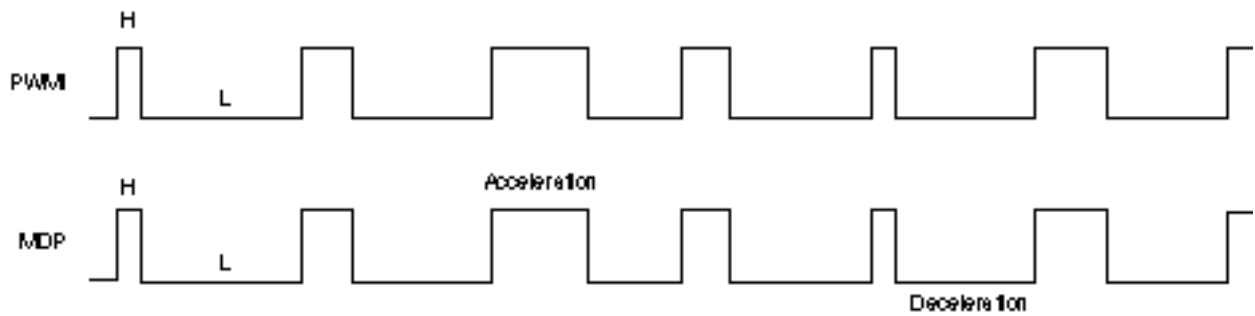
Timing Chart 1-17

CAV-W mode EPWM = LPWR = 1

PWM

H

L

MDP

H

Z

Acceleration

The BRAKE pulse is masked when LPWR = 1.
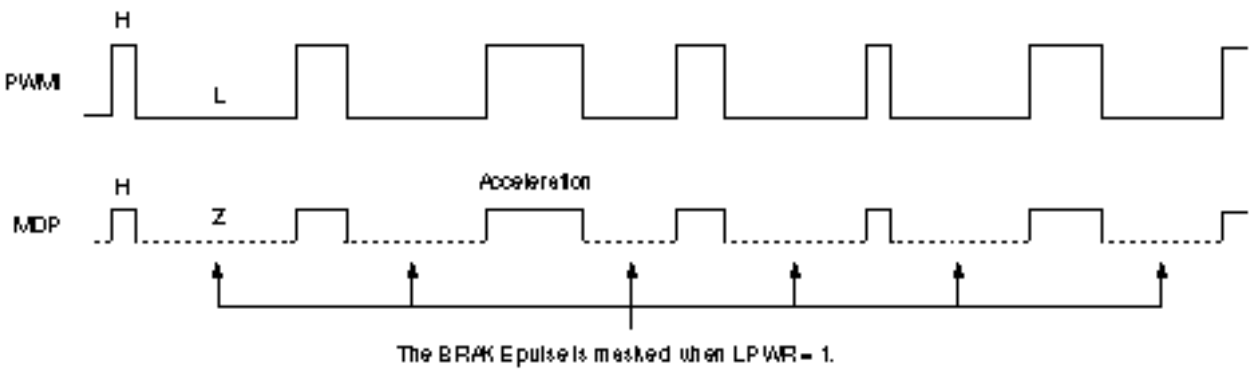
[2] Subcode Interface

There are two methods for reading out a subcode externally.

The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK.

Sub-Q can be read out after checking CRC of the 80 bits in the subcode frame.

Sub-Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

§ 2-1. P to W Subcode Readout

Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-1.)

§ 2-2. 80-bit Sub-Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit Sub-Q register.

- First, Sub-Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub-Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.

  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.

  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.

  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- The previously mentioned peak detection register can be connected to the shift-in of the 80-bit parallel/serial register.

  For ring control 1, input and output are shorted during peak meter and level meter modes.

  For ring control 2, input and output are shorted during peak meter mode.

  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.

  As a result, the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is stored in the memory in peak meter mode. (See Timing Chart 2-3.)
- The high and low intervals for SQCK should be between 750ns and 120µs.
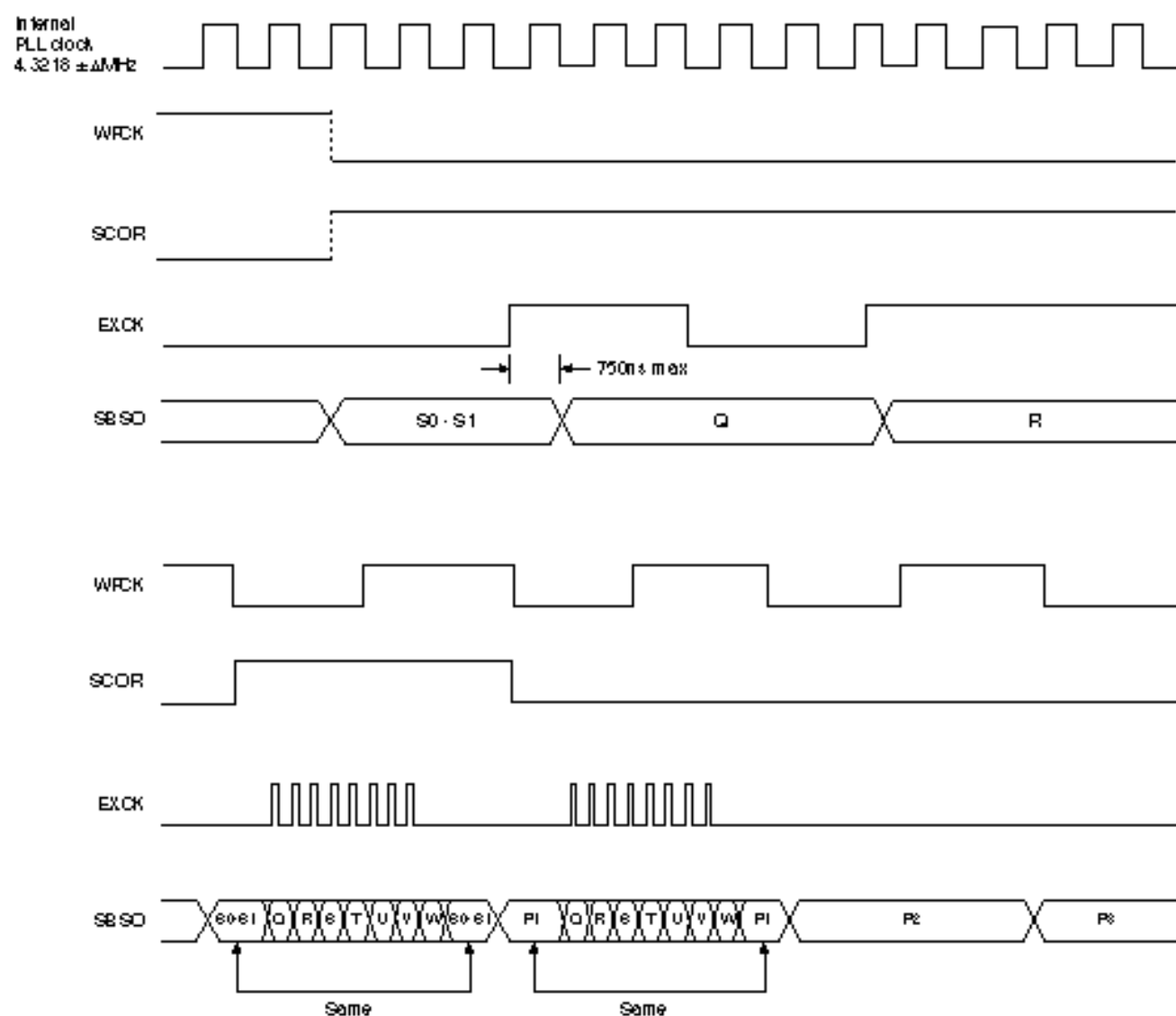
Timing Chart 2-1

Subcode P.Q.R.S.T.U.V.W Read Timing

Block Diagram 2-2
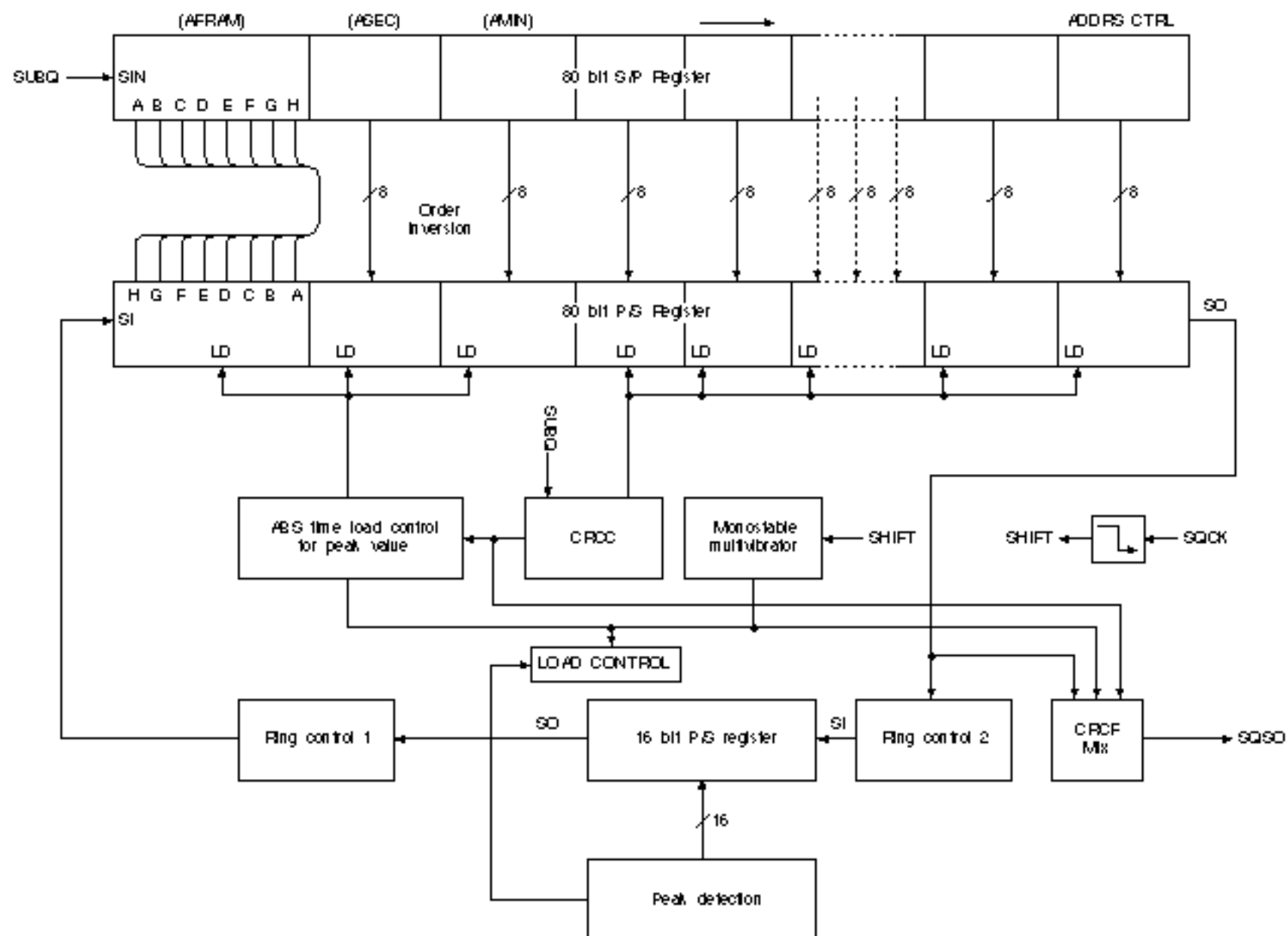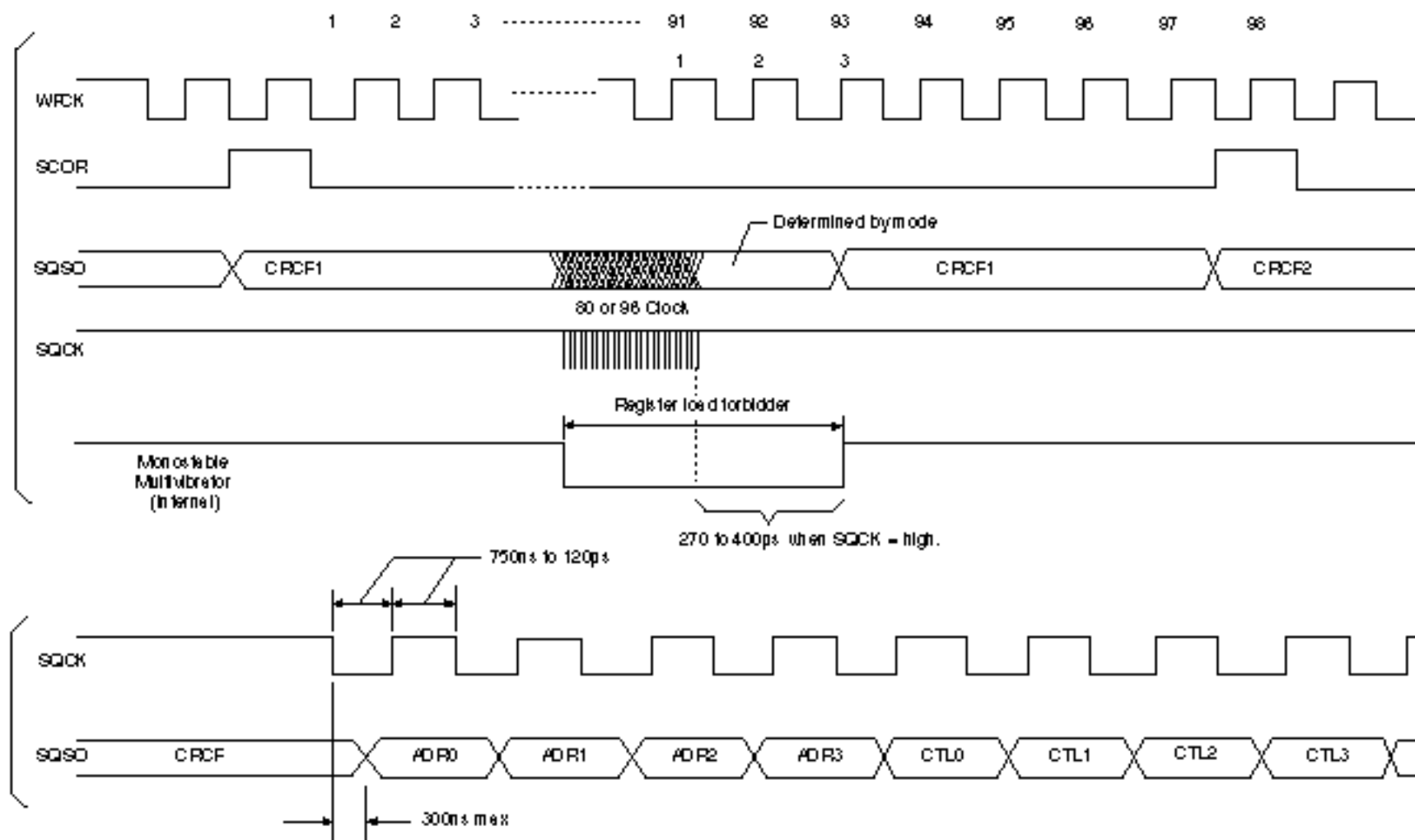
Timing Chart 2-4
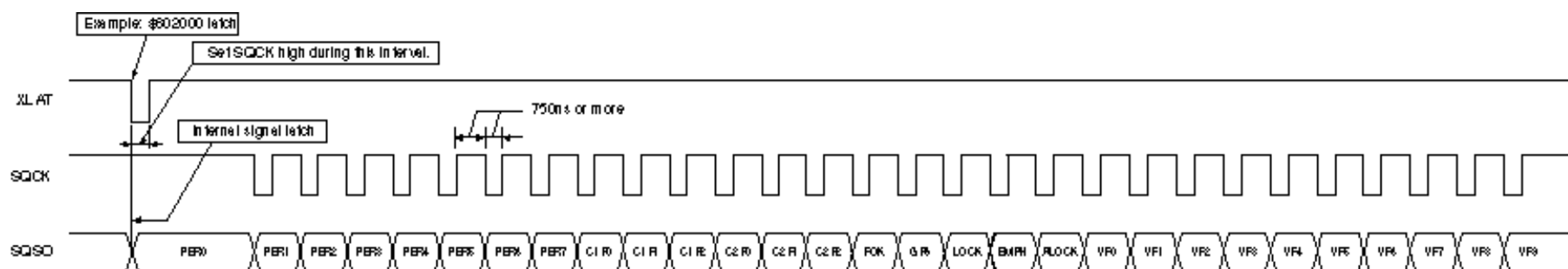
Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK.
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
VF0 to 9	Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See Timing Chart 2-5.) VF0 = LSB, VF9 = MSB.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors; C1 pointer reset
0	0	1	One C1 error corrected; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors; C1 pointer set
1	0	1	One C1 error corrected; C1 pointer set
1	1	0	Two C1 errors corrected; C1 pointer set
1	1	1	C1 correction impossible; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors; C2 pointer reset
0	0	1	One C2 error corrected; C2 pointer reset
0	1	0	Two C2 errors corrected; C2 pointer reset
0	1	1	Three C2 errors corrected; C2 pointer reset
1	0	0	Four C2 errors corrected; C2 pointer reset
1	0	1	—
1	1	0	C2 correction impossible; C1 pointer copy
1	1	1	C2 correction impossible; C2 pointer set

Timing Chart 2-5
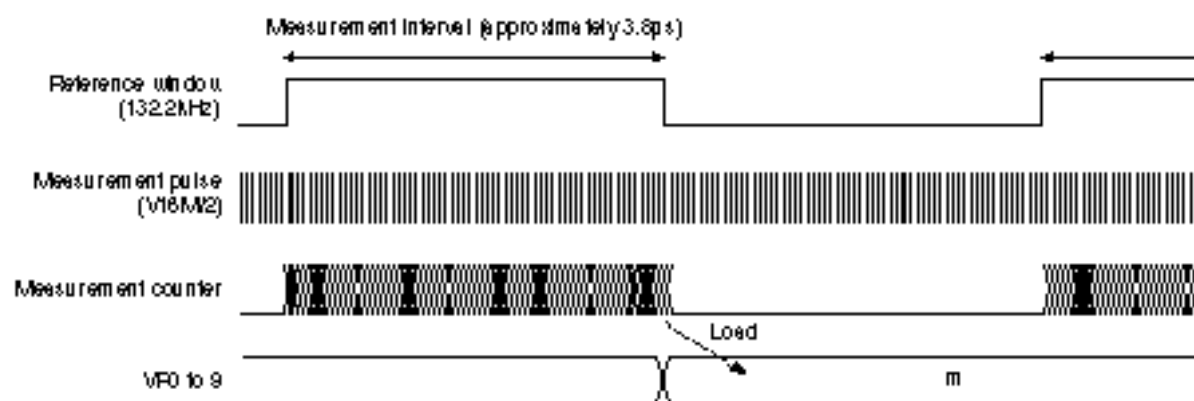
The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{(m + 1)}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 9 is the result obtained by counting V16M/2 pulses while the reference signal (132.2kHz) generated from XTAL (XTAI, XTAO) (384Fs) is high. This value is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).
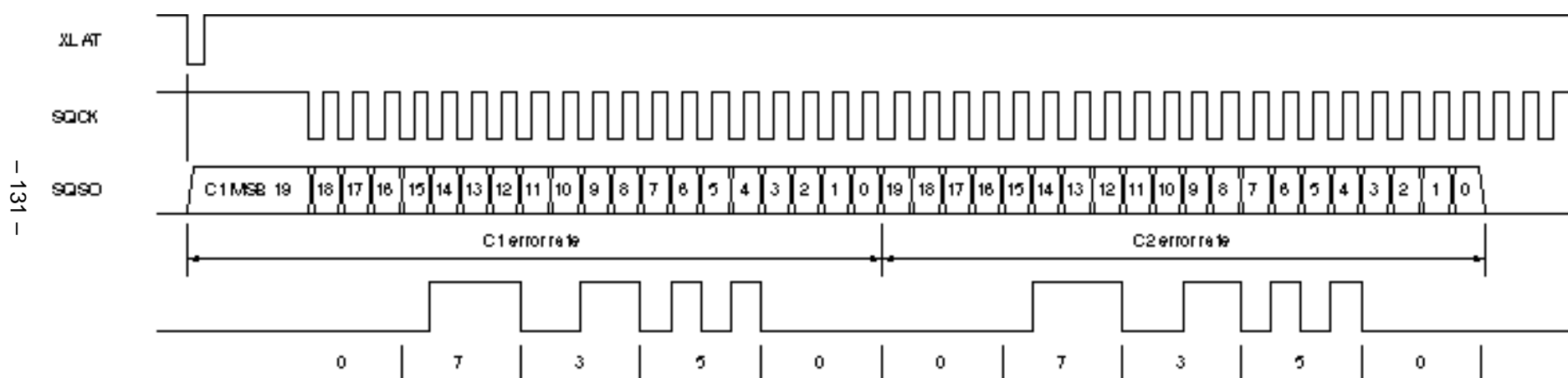
[3] Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§ 3-1. CLV-N Mode

This mode is compatible with the CXD2510Q, and operation is the same as for conventional control. The PLL capture range is ±150kHz.

§ 3-2. CLV-W Mode

This is the wide capture range mode. This mode allows the PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the V16M pin.)

When starting to rotate the disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $E665X to set CAV-W mode and kick the disc, then send $E60CX to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set high, deceleration pulses are not output, thereby achieving low power consumption mode.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§ 3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to the desired rotational velocity. The rotational velocity is determined by the VP0 to VP7 setting values or the external PWM. When controlling the spindle with VP0 to VP7, setting CAV-W mode with the $E665X command and controlling VP0 to VP7 with the $DX commands allows the rotational velocity to be varied from low speed to 4× speed. (See "$DX commands".) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. The reference frequency for the velocity measurement is a signal of 132.3kHz obtained by dividing XTAL (XTAI, XTAO) (384Fs) by 128. The velocity is obtained by counting the half of V16M pulses while the reference is high, and the result is output from the new CPU interface as 10 bits (VP0 to VP9). These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at 4× speed. These values match those of the 256 - n for control with VP0 to VP7. (See Table 2-5 and Fig. 2-6.)

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and others output from this LSI change according to the rotational velocity of the disc.

Note) The capture range for this mode is theoretically up to the signal processing limit.
Note) Set FLFC to 1 for this mode

§ 3-4. VCO-C Mode

This is VCO control mode. In this mode, the V16M oscillation frequency can be controlled by setting $D commands VP0 to VP7 and VPCTL0, 1. The V16M oscillation frequency can be expressed by the following equation.

$$V16M = \frac{l\,(256 - n)}{32}$$

n: VP0 to 7 setting value
l: VPCTL0, 1 setting value

The VCO1 oscillation frequency is determined by V16M. The VCO1 frequency can be expressed by the following equation.

• When DSPB = 0

$$VCO1 = V16M \times \frac{49}{24}$$

• When DSPB = 1

$$VCO1 = V16M \times \frac{49}{16}$$
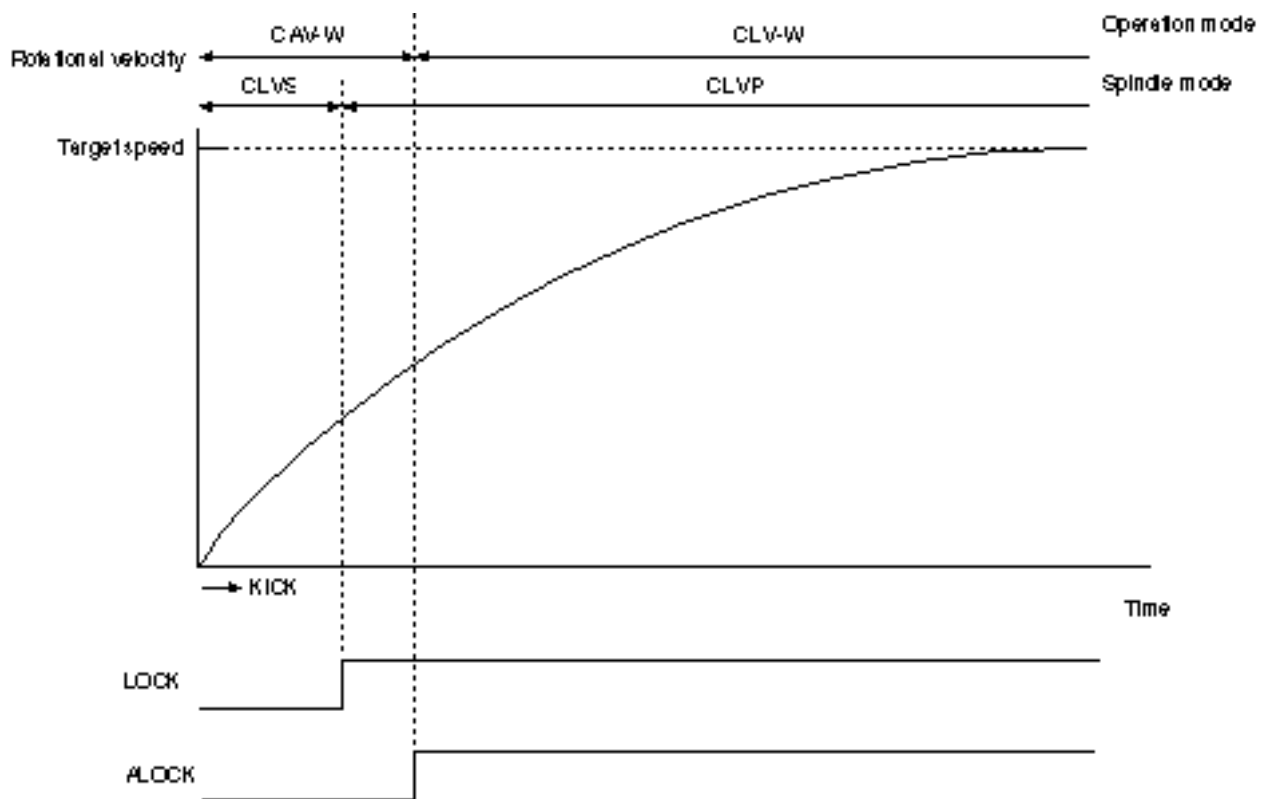
Fig. 3-1. Disc Stop to Regular Playback in CLV-W Mode

CLV-W Mode
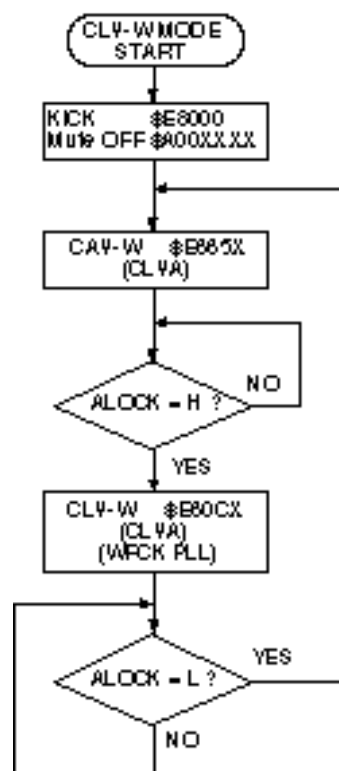
Fig. 3-2. CLV-W Mode Flow Chart

VCO-C Mode
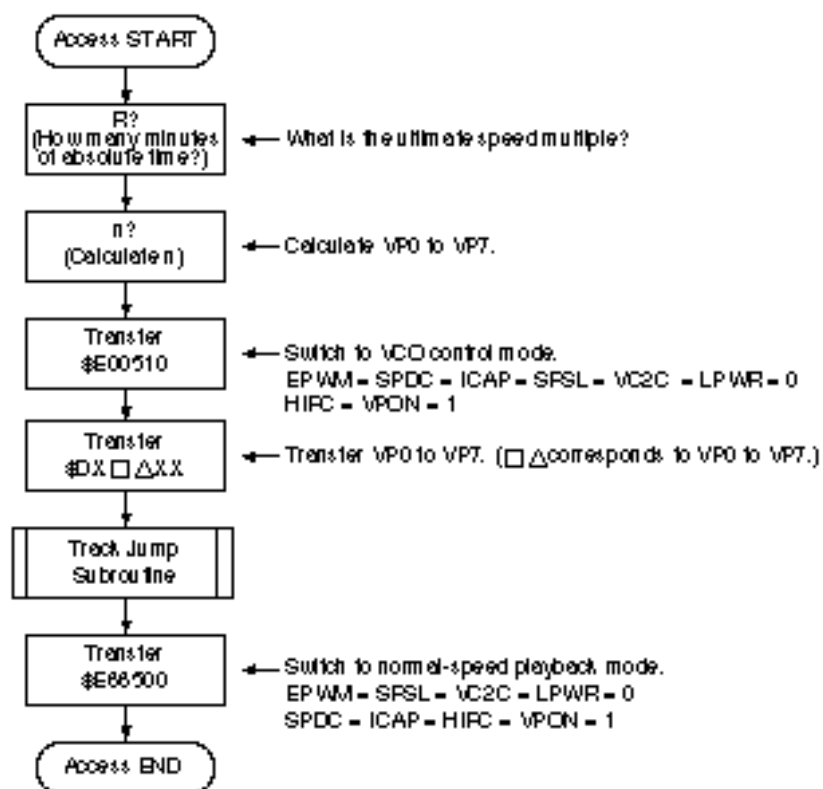
Fig. 3-3. Access Flow Chart Using VCO Control

[4] Description of other functions

§ 4-1. Channel Clock Regeneration by Digital PLL Circuit

• The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.

Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.

In an actual player, a PLL is necessary for regenerating the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.

The CXD3068Q has a built-in three-stage PLL.

• The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are necessary.

The output of this first-stage PLL is used as a reference for all clocks within the LSI.

• The second-stage PLL regenerates the high-frequency clock needed by the third-stage digital PLL.

• The third-stage PLL is a digital PLL that regenerates the actual channel clock.

• The digital PLL in CLV-N mode has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. High frequency components such as 3T and 4T may contain deviations. In such cases, turning the secondary loop off yields better playability. However, in this case the capture range becomes ±50kHz.

• A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

Block Diagram 4-1
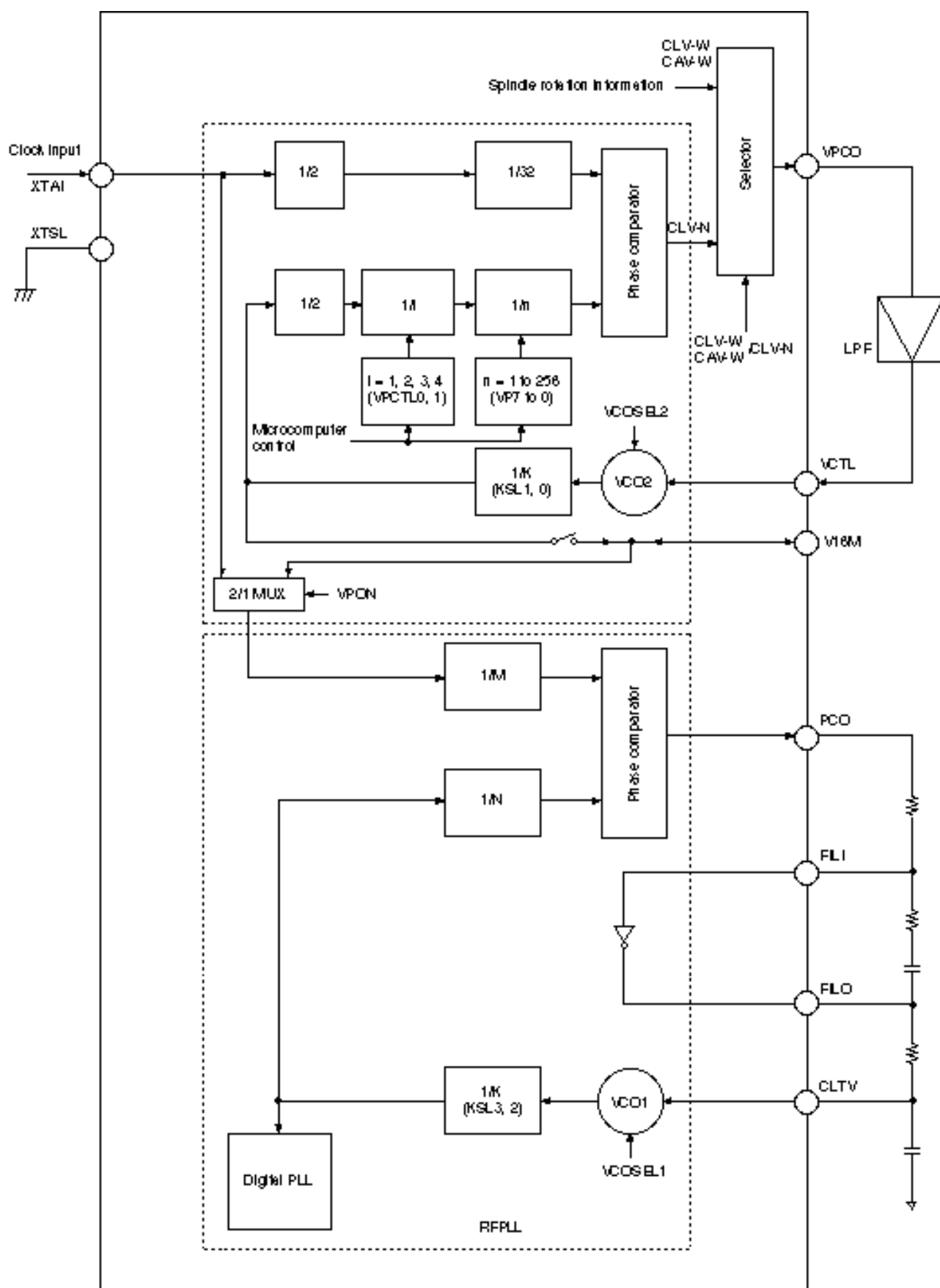
§ 4-2. Frame sync protection

- In normal speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD3068Q, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is set to 13[*], and the backward protection counter to 3[*]. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.
  In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.
  [*] Default values. These values can be set as desired by $C commands SFP0 to SFP3 and SRP0 to SRP3.

§ 4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD3068Q uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored externally.
  See Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description	
0	0	0	0	No C1 errors;	C1 pointer reset
0	0	0	1	One C1 error corrected;	C1 pointer reset
0	0	1	0	—	
0	0	1	1	—	
0	1	0	0	No C1 errors;	C1 pointer set
0	1	0	1	One C1 error corrected;	C1 pointer set
0	1	1	0	Two C1 errors corrected;	C1 pointer set
0	1	1	1	C1 correction impossible;	C1 pointer set
1	0	0	0	No C2 errors;	C2 pointer reset
1	0	0	1	One C2 error corrected;	C2 pointer reset
1	0	1	0	Two C2 errors corrected;	C2 pointer reset
1	0	1	1	Three C2 errors corrected;	C2 pointer reset
1	1	0	0	Four C2 errors corrected;	C2 pointer reset
1	1	0	1	—	
1	1	1	0	C2 correction impossible;	C1 pointer copy
1	1	1	1	C2 correction impossible;	C2 pointer set

Table 4-2.

Timing Chart 4-3

Normal-speed PB

400 to 500ns

RFCK

1 = Depend ention error condition

MNT3

C1 correction   C2 correction

MNT2

MNT1

MNT0

Strobe   Strobe
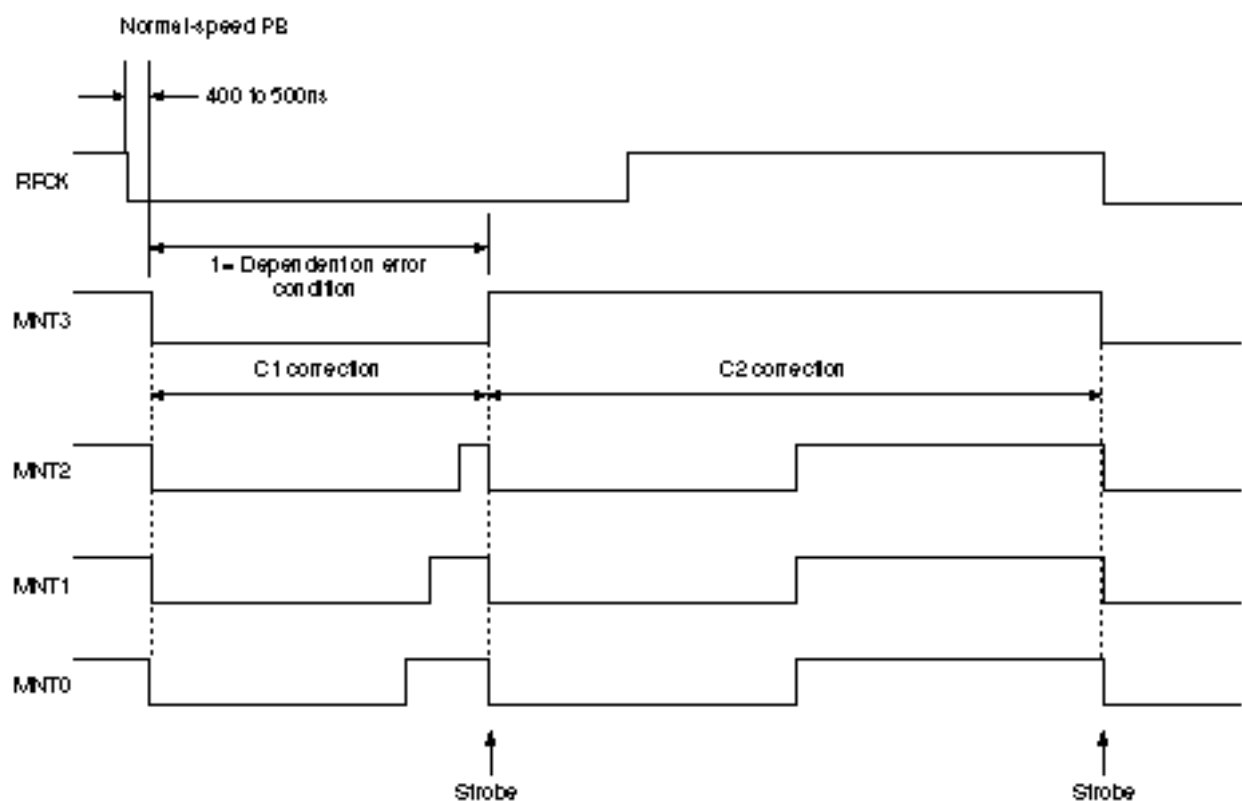
§ 4-4. DA Interface

• The CXD3068Q supports the 48-bit slot interface as the DA interface.

48-bit slot interface

This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.

When LRCK is high, the data is for the left channel.

48bit slot Normal-Speed Playback PSSL = L
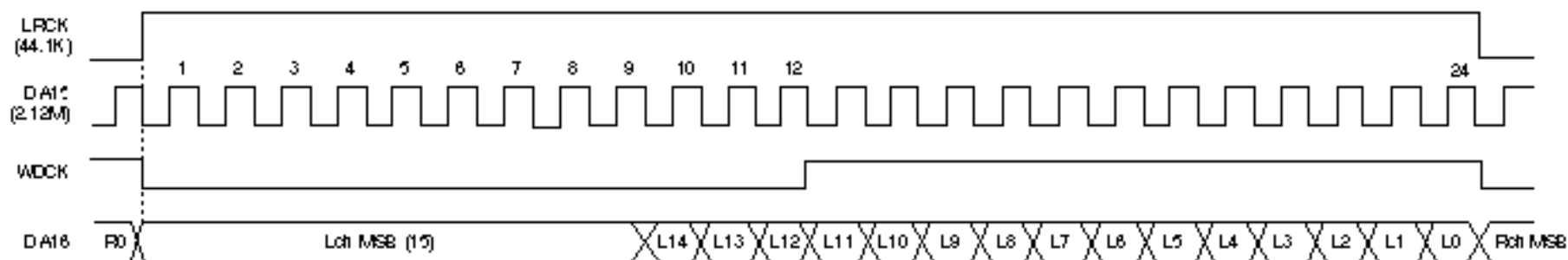
48bit slot Double-Speed Playback
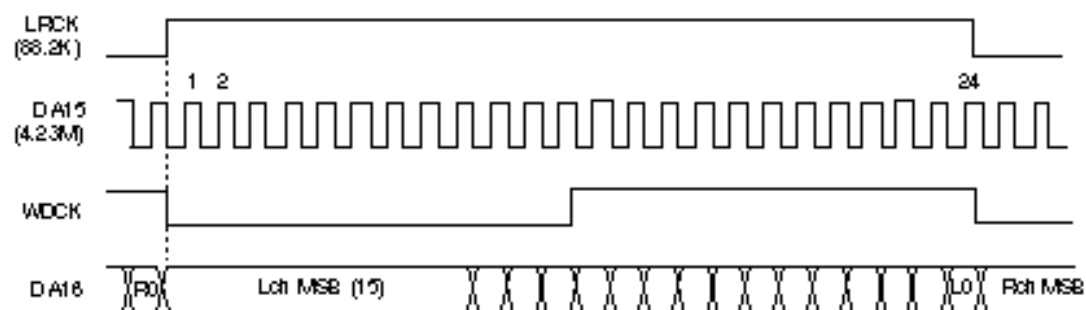
CXD3068Q

§ 4-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD3068Q supports type 2 form 1.

The channel status clock accuracy is automatically set to level II when using the crystal clock and to level III in CAV-W mode or variable pitch mode. In addition, Sub-Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3).

DOUT is output when the crystal is 34MHz and DSPB is set to 1 with XTSL high in CLV-N or CLV-W mode. Therefore, set MD2 to 0 and turn DOUT off.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	D0	D1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

bit0 to 3　Sub-Q control bits that matched twice with CRCOK

bit29　　　VPON or VARION: 1　X'tal 0

Table 4-5.

§ 4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump, fine search and M-track move are executed automatically.

The servo block operates according to the built-in program during the auto sequence execution (when XBUSY = low), so that commands from the CPU, that is $0, 1, 2 and 3 commands, are not accepted. ($4 to E commands are accepted.)

In addition, when using the auto sequence, turn the A.SEQ of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built into this LSI as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See [1] "$4X commands" concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.

Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

  Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

  If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-6. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

(b) Track jump

  1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not involved in this sequence.

  • 1-track jump

    When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-7. Set blind A and brake B with register 5.

  • 10-track jump

    When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed an accordance with Fig. 4-8. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

• 2N-track jump

When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-9. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used with N is 16 or more.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

• Fine search

When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-10. The differences from a 2N-track jump are that a higher precision is achieved by controlling the traverse speed, and a longer distance jump is achieved by controlling the sled. The track jump count is set with register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F with register 6 and overflow G with register 5. Also, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls with register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set with register 6.) Then, the tracking and sled servos are turned on.

Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count N − α for the traverse monitor counter which is set with register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

• M-track move

When $4E ($4F for REV) is received from the CPU, a FWD (REV) M-track move is performed in accordance with Fig. 4-11. M can be set to 2^{16} tracks. Like the 2N-track jump, COUT is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or more. The M-track move is executed by moving only the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servos are turned off after M tracks have been counted through COUT or MIRR unlike for the other jumps. Transfer $25 from the microcomputer after the actuator has stabilized.
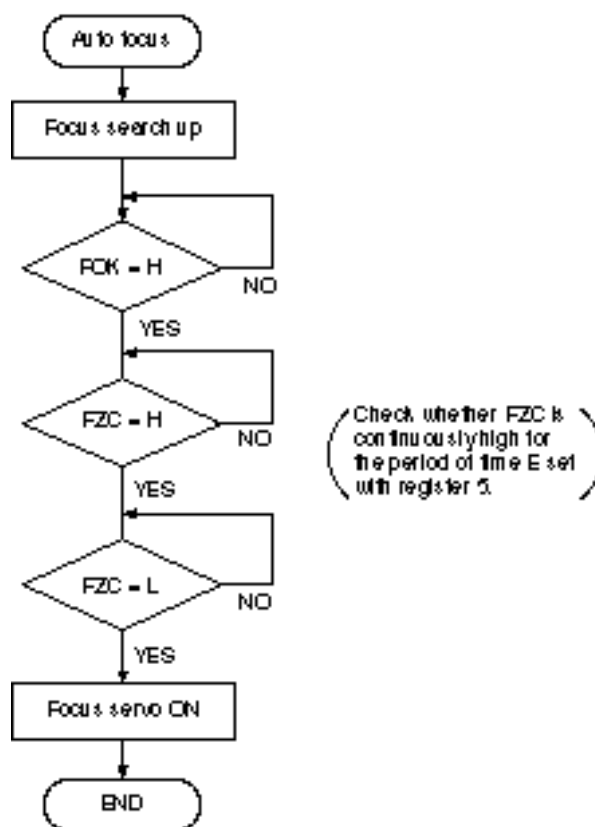
Fig. 4-6-(a). Auto Focus Flow Chart
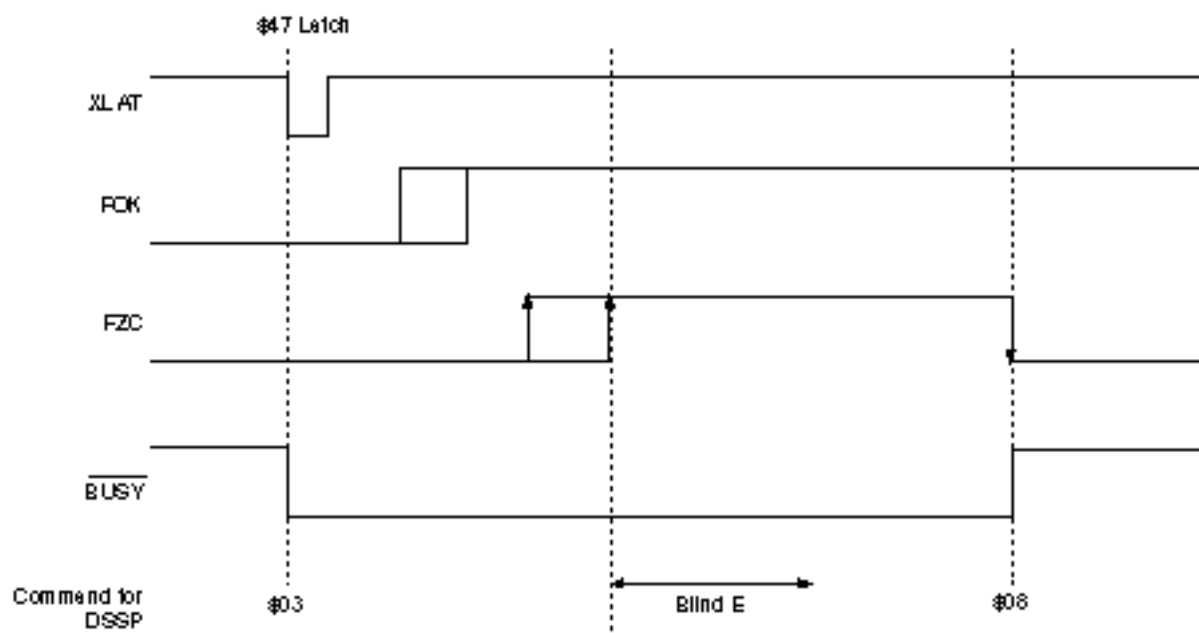
Fig. 4-6-(b). Auto Focus Timing Chart
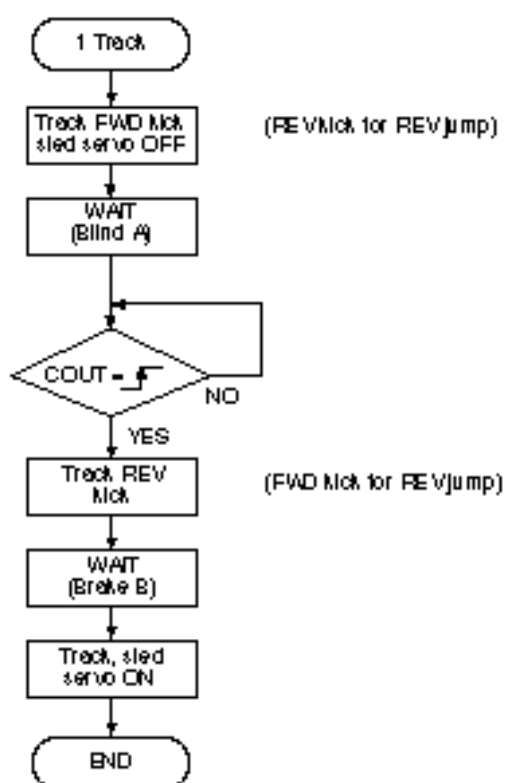
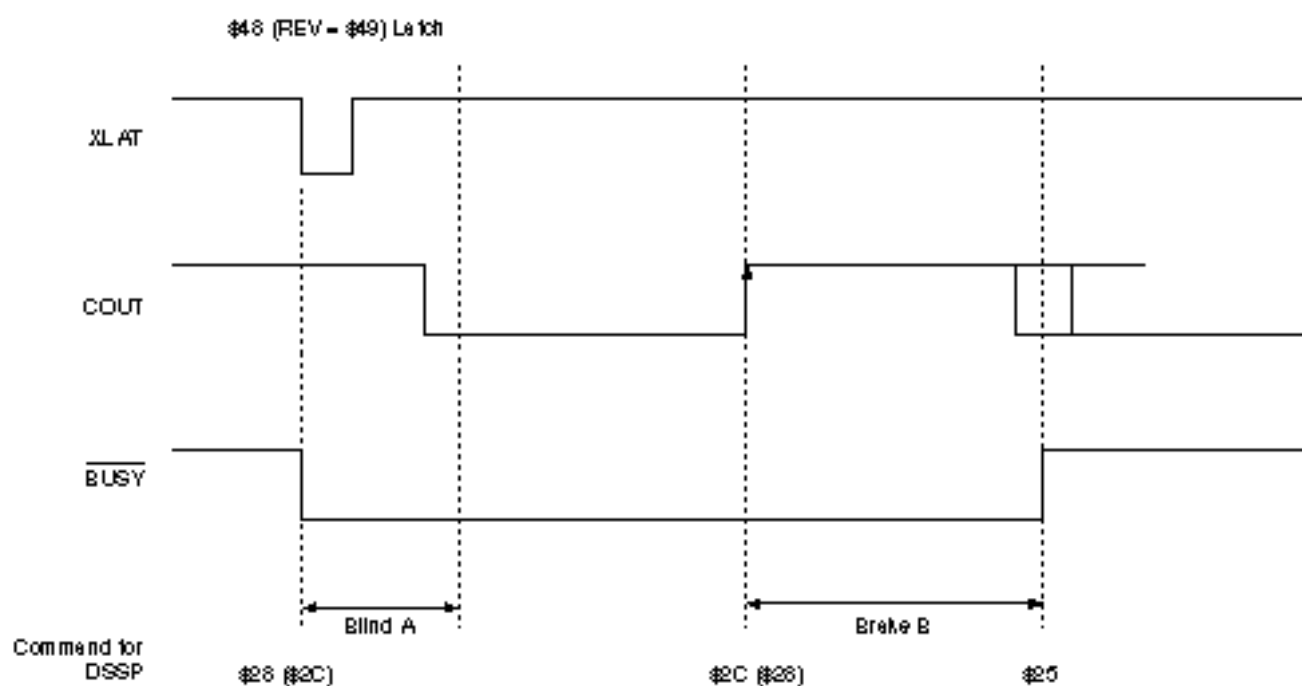**Fig. 4-7-(a). 1-Track Jump Flow Chart**

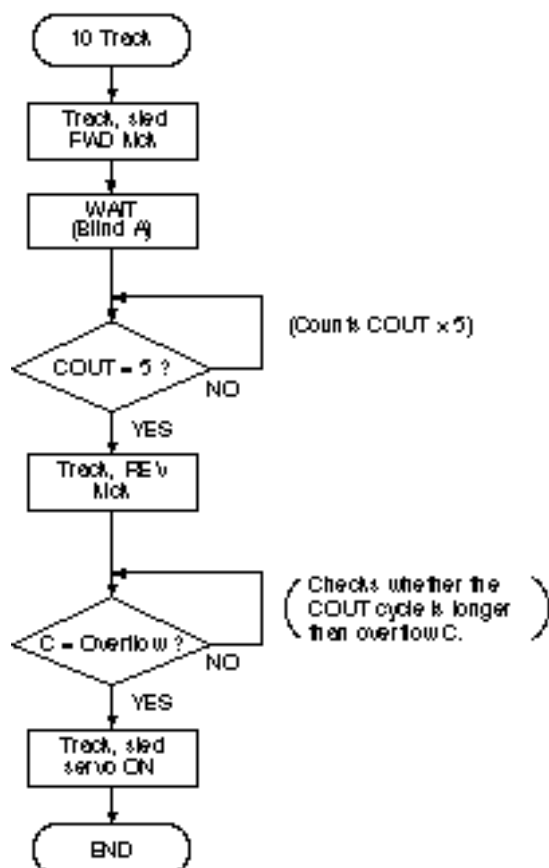

Fig. 4-7-(b). 1-Track Jump Timing Chart

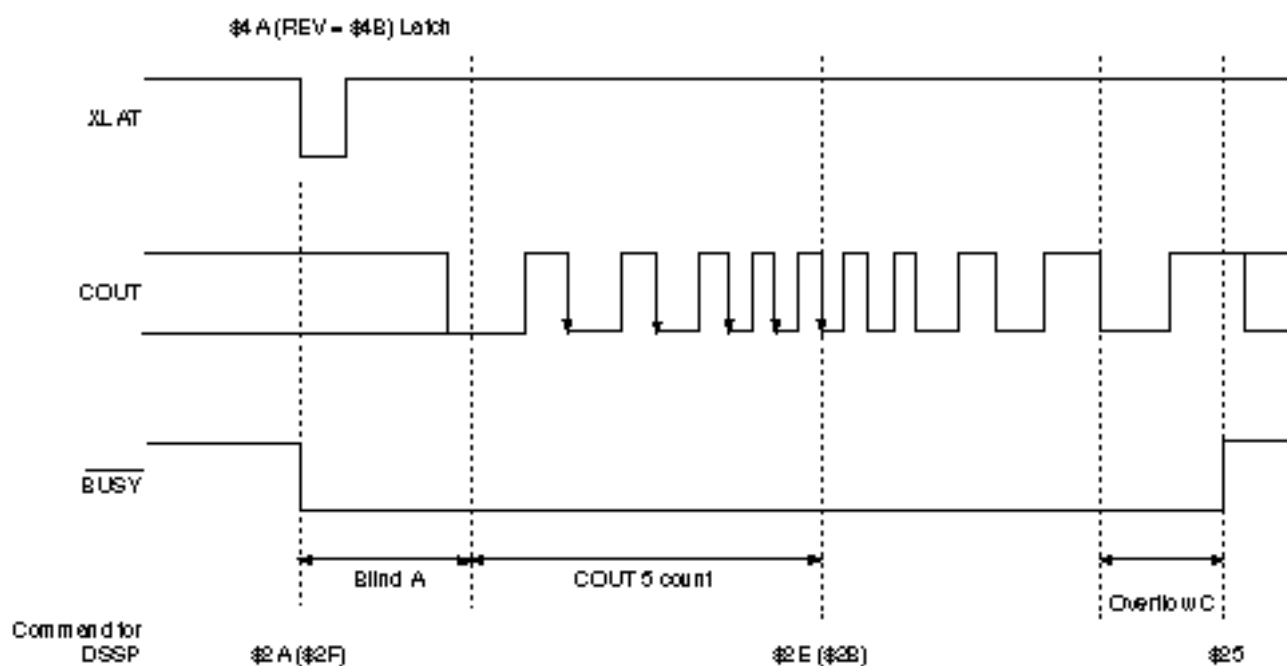**Fig. 4-8-(a). 10-Track Jump Flow Chart**
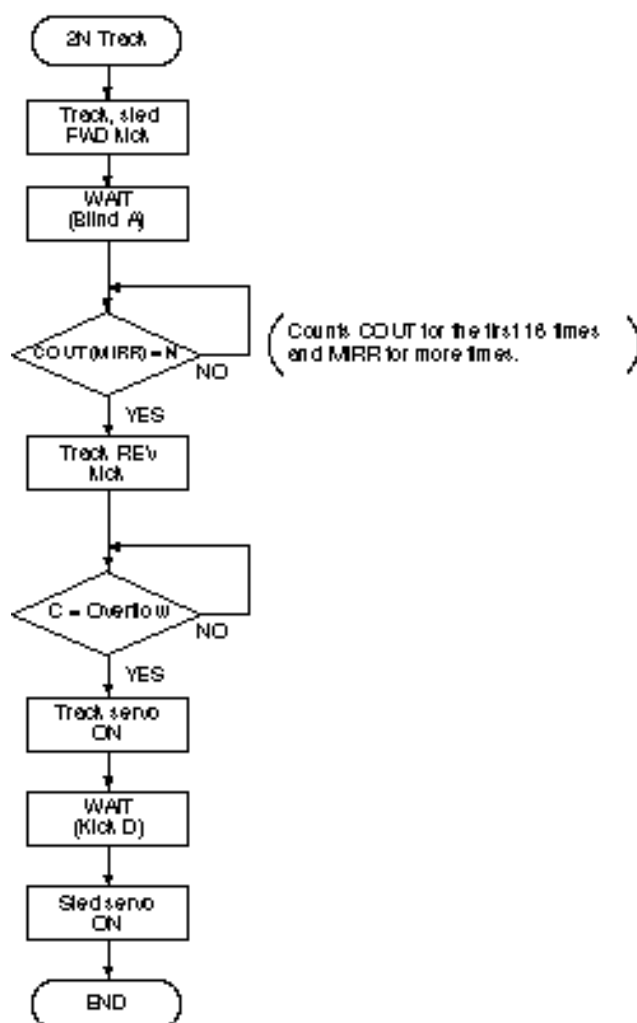

Fig. 4-8-(b). 10-Track Jump Timing Chart

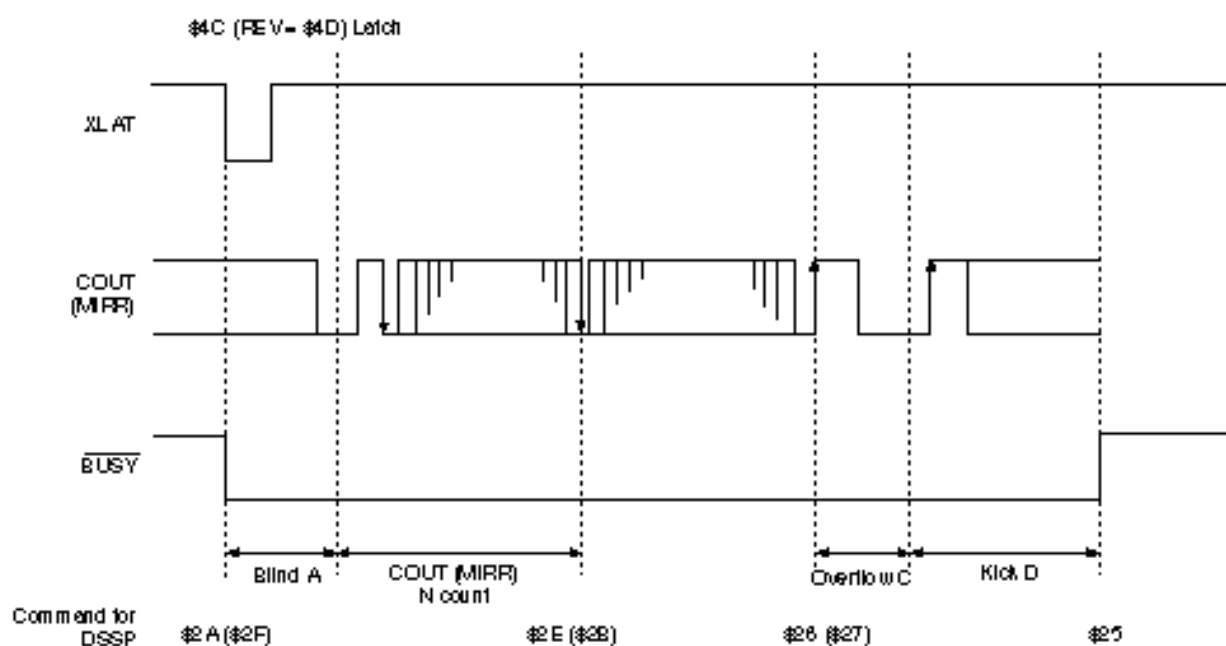**Fig. 4-9-(a). 2N-Track Jump Flow Chart**
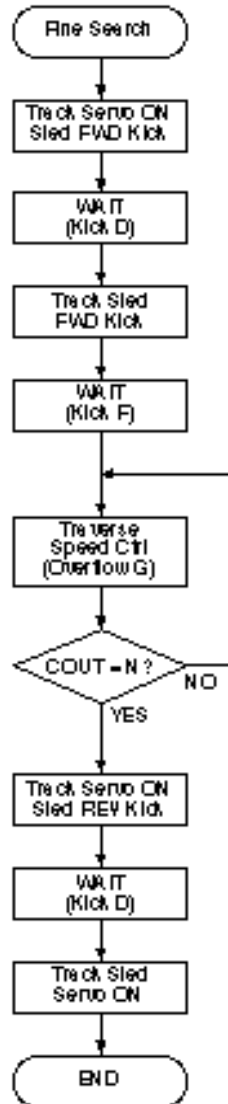

Fig. 4-9-(b). 2N-Track Jump Timing Chart
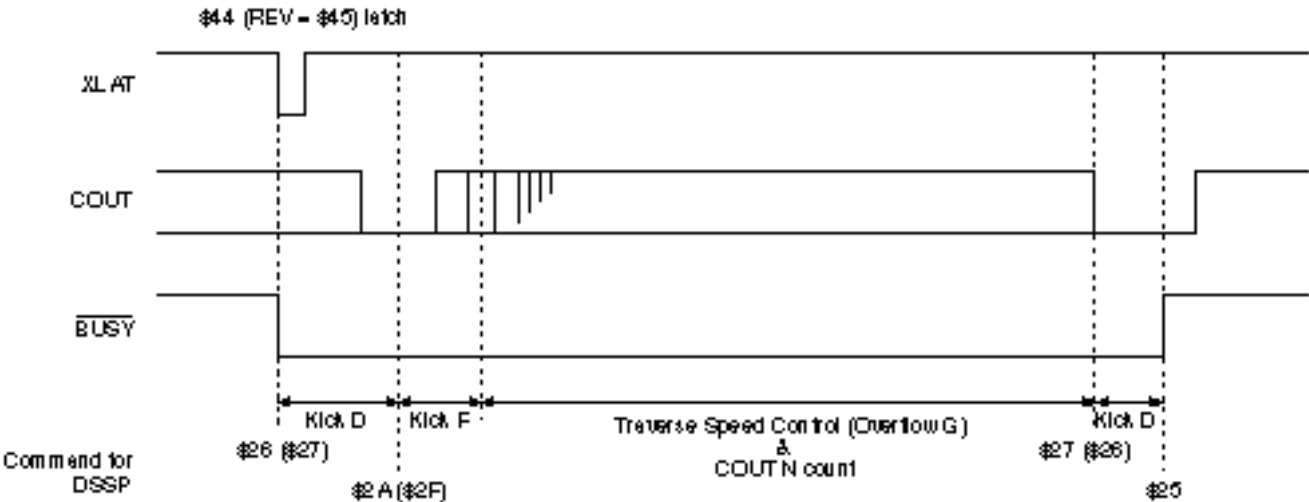
Fig. 4-10-(a). Fine Search Flow Chart
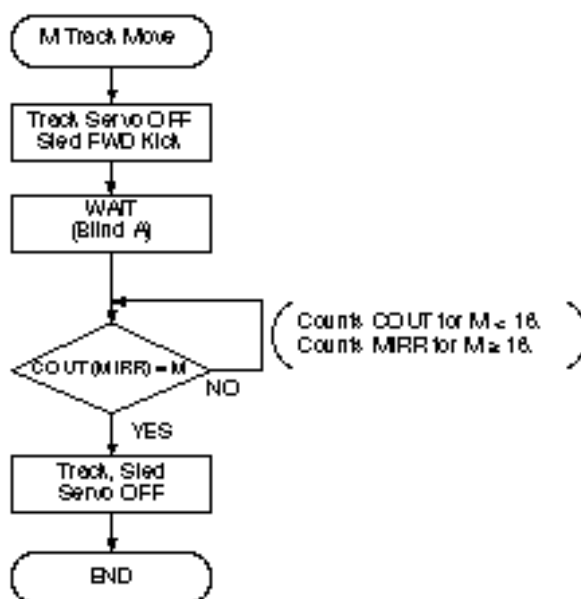

Fig. 4-10-(b). Fine Search Timing Chart

Fig. 4-11-(a). M-Track Move Flow Chart
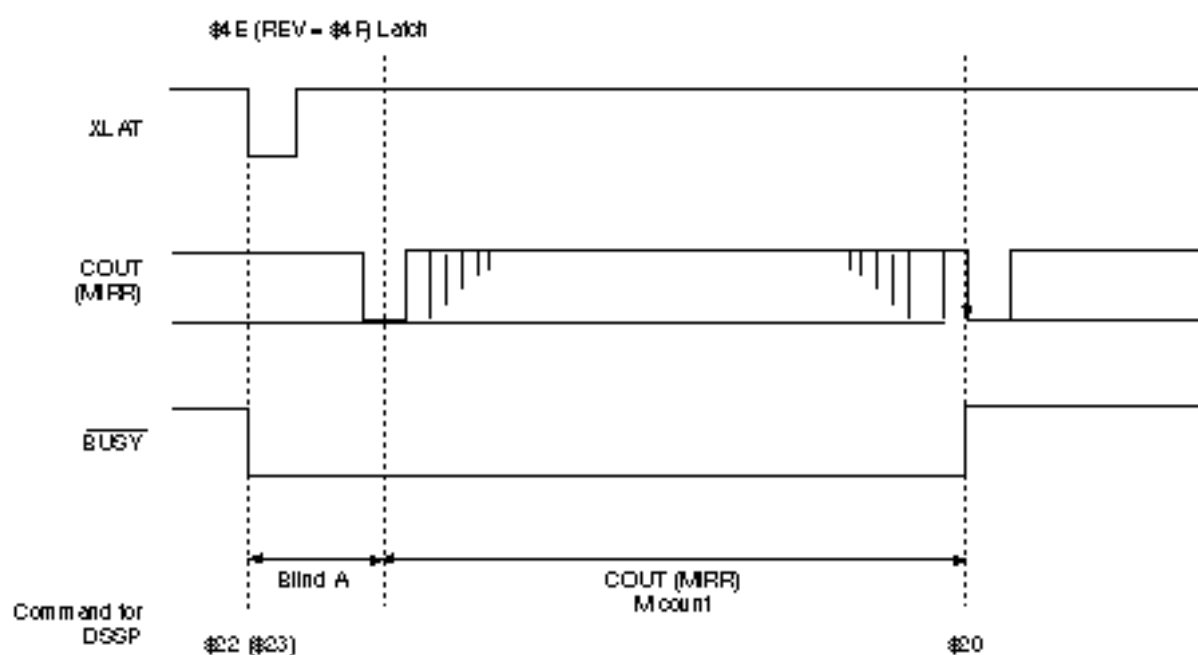
Fig. 4-11-(b). M-Track Move Timing Chart

§ 4-7. Digital CLV

Fig. 4-12 shows the block diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.

Digital CLV
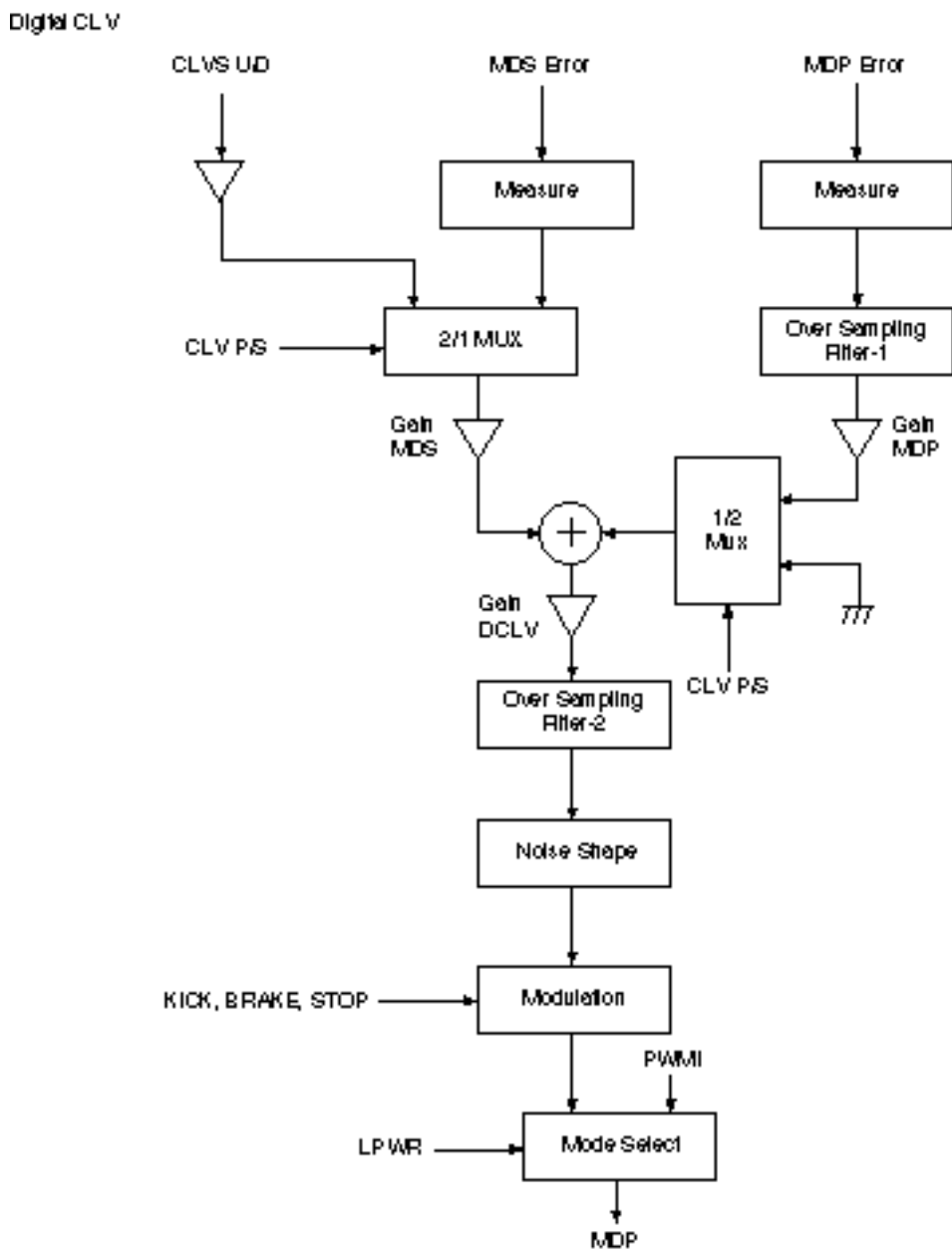
CLVS U/D:	Up/down signal from CLVS servo
MDS error:	Frequency error for CLVP servo
MDP error:	Phase error for CLVP servo
PWMI:	Spindle drive signal from the microcomputer for CAV servo

Fig. 4-12. Block Diagram

§ 4-8. Playback Speed

In the CXD3068Q, the following playback modes can be selected through different combinations of XTAI, XTSL pin, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency division commands (KSL3, KSL2) and command transfer rate selector (ASHS) in CLV-N or CLV-W mode.

Mode	XTAI	XTSL	DSPB	VCOSEL1[*1]	ASHS	Playback speed	Error correction[*2]
1	768Fs	1	0	0/1	0	1×	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	2×	C1: double; C2: double
3	768Fs	0	0	1	1	2×	C1: double; C2: quadruple
4	768Fs	0	1	1	1	4×	C1: double; C2: double
5	384Fs	0	0	0/1	0	1×	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	2×	C1: double; C2: double
7	384Fs	1	1	0/1	0	1×	C1: double; C2: double

[*1] Actually, the optimal value should be used together with KSL3 and KSL2.

[*2] When $8 ERC4 = 1, C2 is for quadruple correction with DSPB = 1.

The playback speed can be varied by setting VP0 to VP7 in CAV-W mode. See "[3] Description of Modes" for details.

§ 4-9. Asymmetry Correction

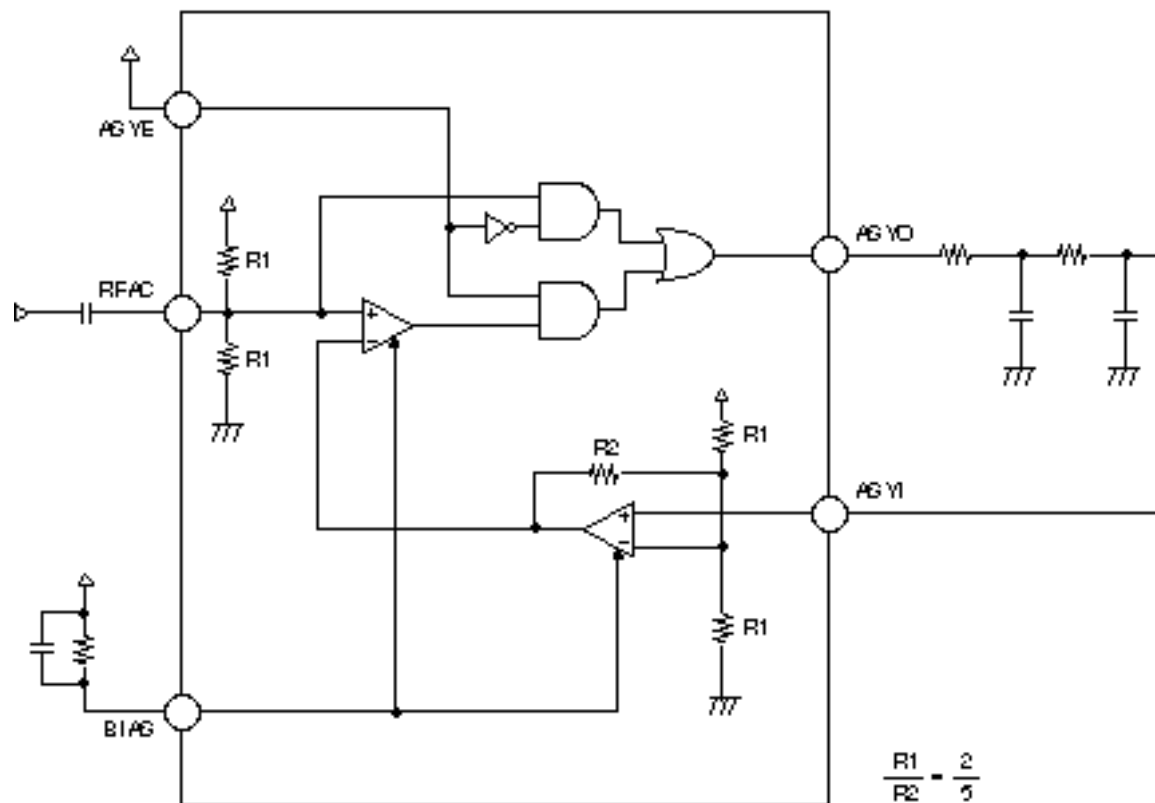Fig. 4-13 shows the block diagram and circuit example.

Fig. 4-15. Asymmetry Correction Application Circuit

§4-10. CD TEXT Data Demodulation

- In order to demodulate the CD TEXT data, set the command $8 Data 6 D3 TXON to 1. During TXON = 1, connect EXCK to low and do not use the data output from SBSO because the CD TEXT demodulation circuit uses EXCK and the SBSO pin exclusively.

  It requires 26.7ms (max.) to demodulate the CD TEXT data correctly after TXON is set to 1.

- The CD TEXT data is output by switching the SQSO pin with the command. The CD TEXT data output is enabled by setting the command $8 Data 6 D2 TXOUT to 1. To read data, the readout clock should be input to SQCK.

- The readable data are the CRC counting results for the each pack and the CD TEXT data (16 bytes) except for CRC data.

- When the CD TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.

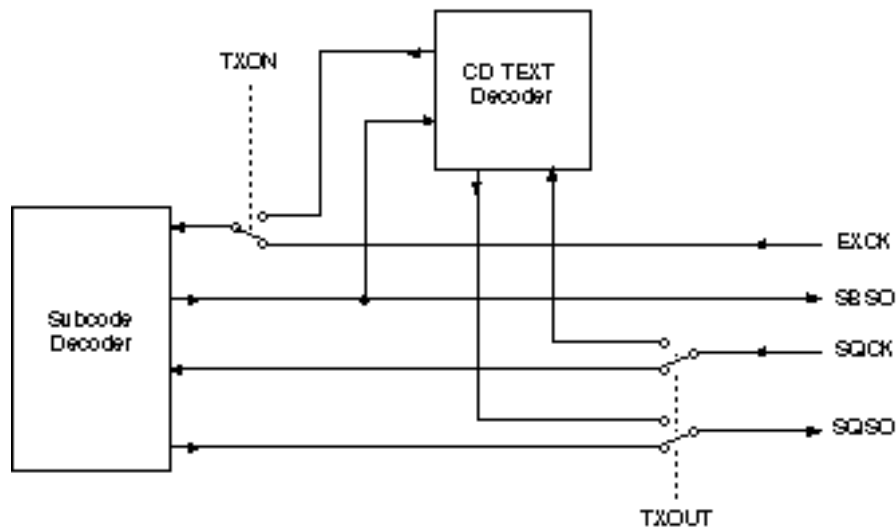- Data which can be stored in the LSI is 1 packet (4 packs).

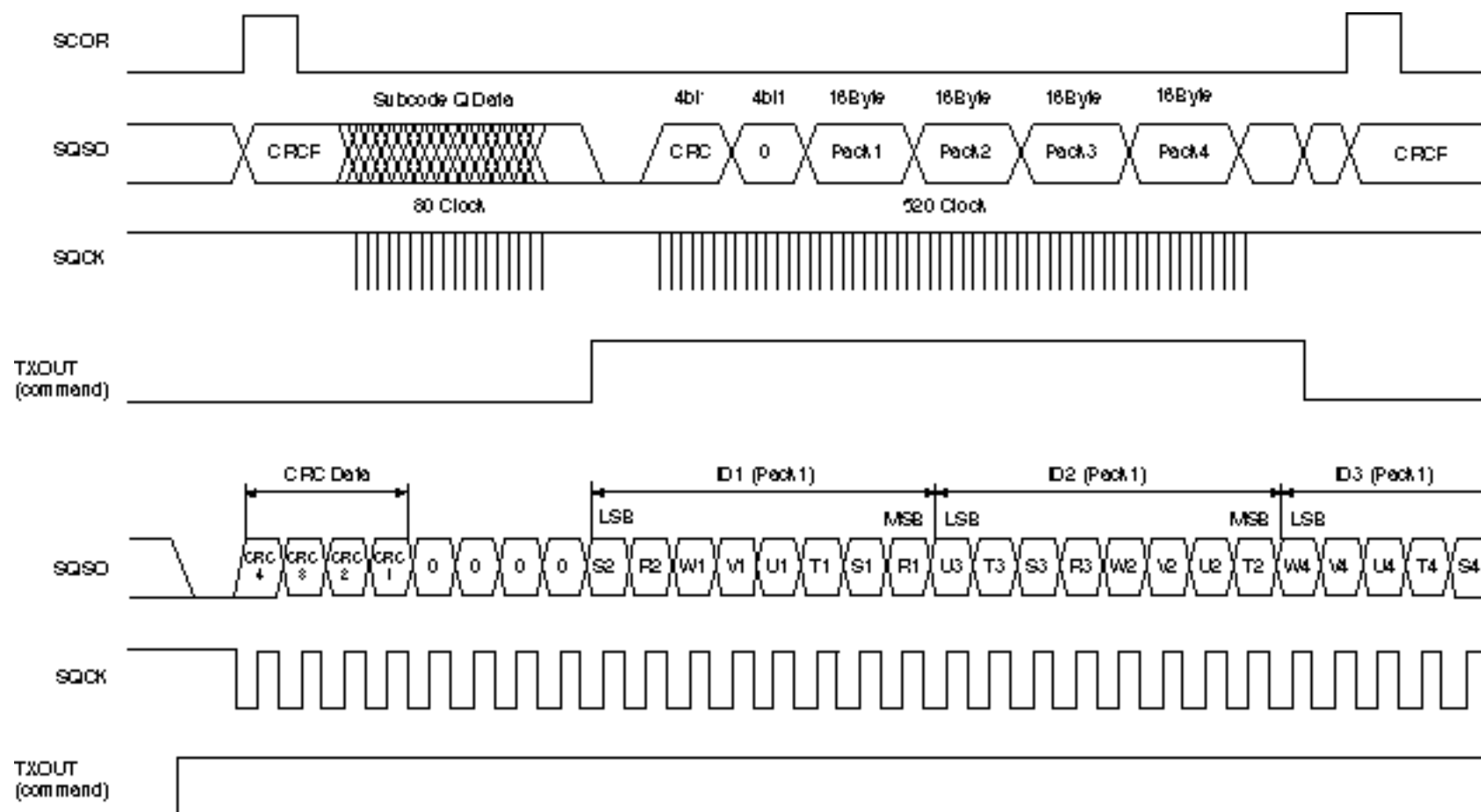**Fig. 4-14. Block Diagram of CD TEXT Demodulation Circuit**

Fig. 4-15. CD TEXT Data Timing Chart

CXD3068Q

[5] Description of Servo Signal Processing System Functions and Commands

§5-1. General Description of Servo Signal Processing System (V$_{DD}$: Supply voltage)

Focus servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1 4V$_{DD}$ to 3 4V$_{DD}$
Output format:	7-bit PWM
Other:	Offset cancel
	Focus bias adjustment
	Focus search
	Gain-down function
	Defect countermeasure
	Auto gain control

Tracking servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1 4V$_{DD}$ to 3 4V$_{DD}$
Output format:	7-bit PWM
Other:	Offset cancel
	E:F balance adjustment
	Track jump
	Gain-up function
	Defect countermeasure
	Drive cancel
	Auto gain control
	Vibration countermeasure

Sled servo

Sampling rate:	345Hz (when MCK = 128Fs)
Input range:	1 4V$_{DD}$ to 3 4V$_{DD}$
Output format:	7-bit PWM
Other:	Sled move

FOK, MIRR, DFCT signal generation

RF signal sampling rate:	1.4MHz (when MCK = 128Fs)
Input range:	1 4V$_{DD}$ to 3 4V$_{DD}$
Other:	RF zero level automatic measurement

§5-2. Digital Servo Block Master Clock (MCK)

The clock with the 2/3 frequency of the crystal is supplied to the digital servo block.

XT4D and XT2D are $3F commands, and XT1D is $3E command. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

Mode	XTAI	FSTO	XTSL	XT4D	XT2D	XT1D	Frequency division ratio	MCK
1	384Fs	256Fs	*	*	*	1	1	256Fs
2	384Fs	256Fs	*	*	1	0	1/2	128Fs
3	384Fs	256Fs	0	0	0	0	1/2	128Fs
4	768Fs	512Fs	*	*	*	1	1	512Fs
5	768Fs	512Fs	*	*	1	0	1/2	256Fs
6	768Fs	512Fs	*	1	0	0	1/4	128Fs
7	768Fs	512Fs	1	0	0	0	1/4	128Fs

Fs = 44.1kHz, *: Don't care

Table 5-1.

§ 5-3. DC Offset Cancel [AVRG (Average) Measurement and Compensation] (See Fig. 5-3.)

The CXD3068Q can measure the average of RFDC, VC, FE and TE and compensate these signals using the measurement results to control the servo effectively. This AVRG measurement and compensation is necessary to initialize the CXD3068Q, and is able to cancel the DC offset.

AVRG measurement takes the levels applied to the VC, FE, RFDC and TE pins as the digital average of 256 samples, and then loads these values into each AVRG register.

The AVRG measurement commands are D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TLM) of $38.

Measurement is on when the respective command is set to 1.

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received. The completion of AVRG measurement operation can be monitored by the SENS pin. (See Timing Chart 5-2.) Monitoring requires that the upper 8 bits of the command register are 38 (Hex).
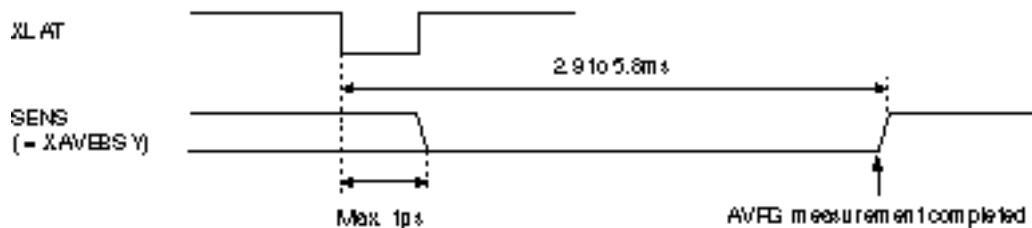
Timing Chart 5-2.

<Measurement>

VC AVRG: The VC DC offset (VC AVRG) which is the center voltage for the system is measured and used to compensate the FE, TE and SE signals.

FE AVRG: The FE DC offset (FE AVRG) is measured and used to compensate the FE and FZC signals.

TE AVRG: The TE DC offset (TE AVRG) is measured and used to compensate the TE and SE signals.

RF AVRG: The RF DC offset (RF AVRG) is measured and used to compensate the RFDC signal.

<Compensation>

RFLC: (RF signal – RF AVRG) is input to the RF In register.
"00" is input when the RF signal is lower than RF AVRG.

TLC0: (TE signal – VC AVRG) is input to the TRK In register.

TLC1: (TE signal – TE AVRG) is input to the TRK In register.

VCLC: (FE signal – VC AVRG) is input to the FCS In register.

FLC1: (FE signal – FE AVRG) is input to the FCS In register.

FLC0: (FE signal – FE AVRG) is input to the FZC register.

Two methods of canceling the DC offset are assumed for the CXD3068Q. These methods are shown in Figs. 5-3a and 5-3b.

An example of AVRG measurement and compensation commands is shown below.

$38 08 00 (RF AVRG measurement)

$38 20 00 (FE AVRG measurement)

$38 00 10 (TE AVRG measurement)

$38 14 0A (Compensation on [RFLC, FLC0, FLC1, TLC1], corresponds to Fig. 5-3a.)

See the description of $38 for these commands.

§ 5-4. E:F Balance Adjustment Function (See Fig. 5-3.)

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.

In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.

The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to "0".

Next, setting D2 (TLC2) of $38 to 1 compensates the values obtained from the TE and SE input pins with the TRVSC register value (subtraction), allowing the E:F balance offset to be adjusted. (See Fig. 5-3.)

§ 5-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 5-3.)

When D11 = 0 and D10 = 1 is set by $34F, the FBIAS register value can be written using the 9-bit value of D9 to D1 (D9: MSB).

In addition, the RF jitter can be monitored by setting the $8 command SOCT to 1. (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of $3A to 1. The FBIAS register functions as an up counter when D12 (FBUP) of $3A = 1, and as a down counter when D12 (FBUP) of $3A = 0.

The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of $3A.

When using the FBIAS register as a counter, the counter stops when the value set beforehand in FBL9 to FBL1 of $34 matches the FCSBIAS value. Also, if the upper 8 bits of the command register are $3A at this time, SENS goes to high and the counter stop can be monitored.

A: Register mode
B: Counter mode
C: Counter mode (when stopped)
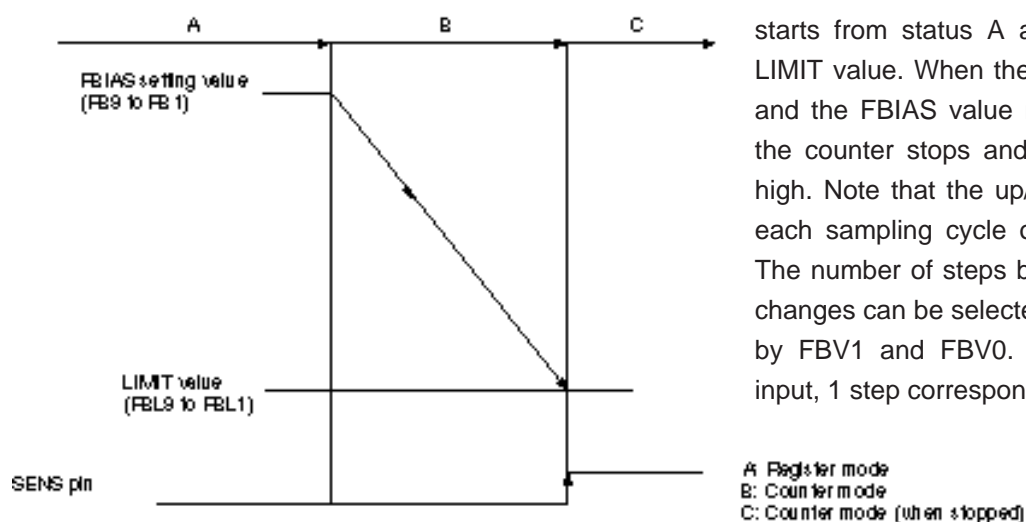
Here, assume the FBIAS setting value FB9 to FB1 and the FBIAS LIMIT value FBL9 to FBL1 are set in status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the LIMIT value is reached and the FBIAS value matches FBL9 to FBL1, the counter stops and the SENS pin goes to high. Note that the up/down counter counts at each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to $1/512 \times V_{DD} \times 0.4$.
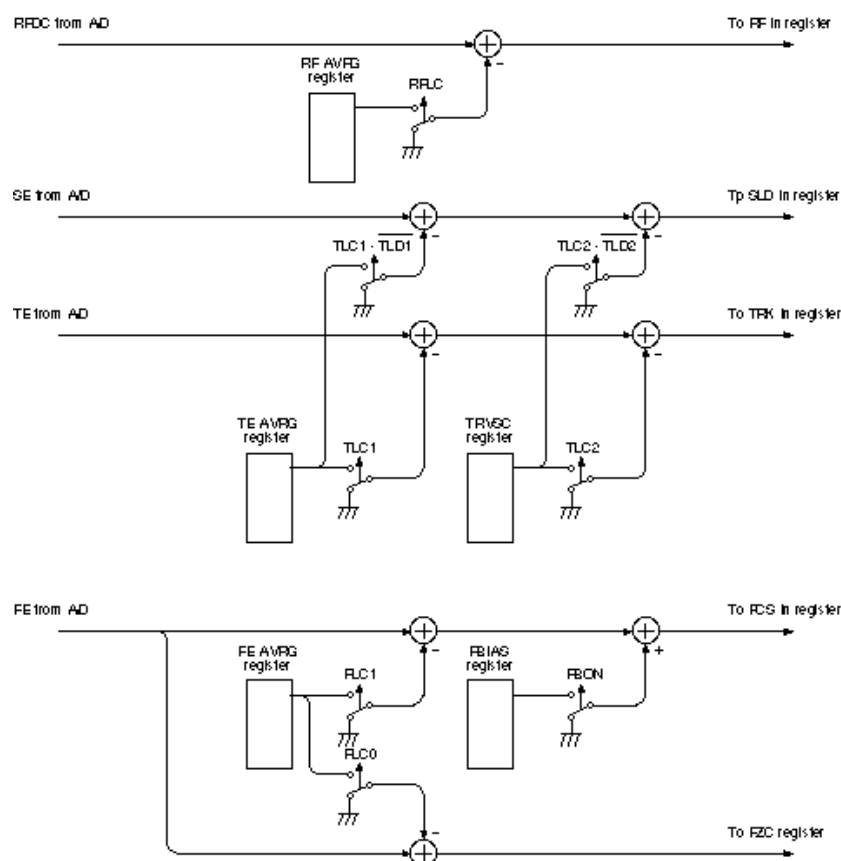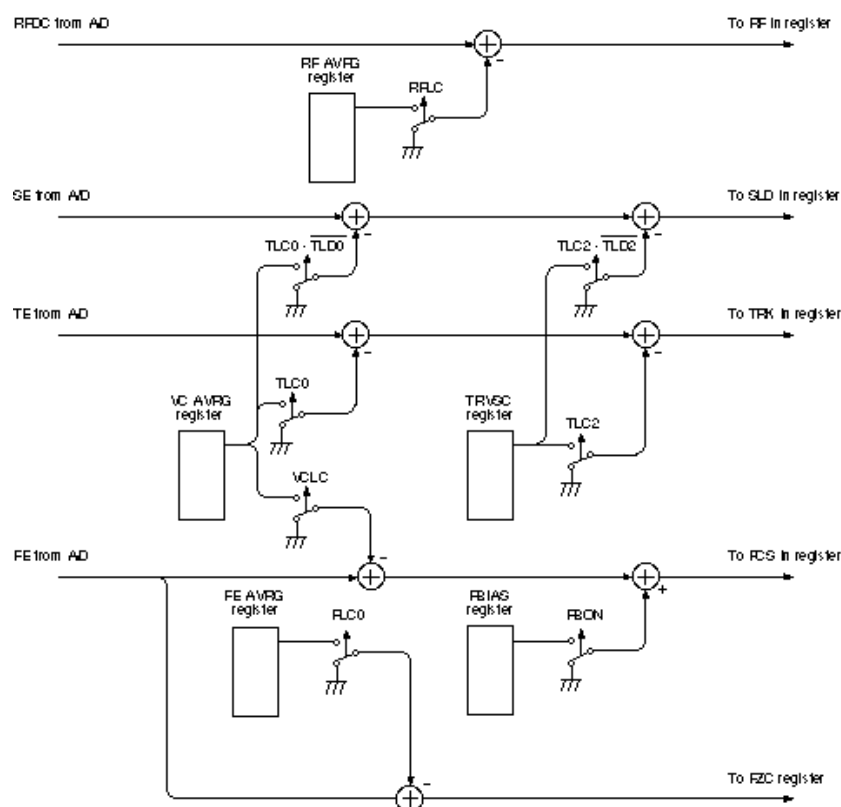
RFDC from A/D ——————————————————→ To RF in register

RF AVRG register

RFLC

SE from A/D ——————————————————→ Tp SLD in register

TLC1 · TLD1

TLC2 · TLD2

TE from A/D ——————————————————→ To TRK in register

TE AVRG register

TLC1

TRVSC register

TLC2

FE from A/D ——————————————————→ To FCS in register

FE AVRG register

FLC1

FBIAS register

FBON

FLC0

To FZC register

Fig. 5-3a.

RFDC from A/D ——————————————————→ To RF in register

RF AVRG register

RFLC

SE from A/D ——————————————————→ To SLD in register

TLC0 · TLD0

TLC2 · TLD2

TE from A/D ——————————————————→ To TRK in register

VC AVRG register

TLC0

VCLC

TRVSC register

TLC2

FE from A/D ——————————————————→ To FCS in register

FE AVRG register

FLC0

FBIAS register

FBON

To FZC register

Fig. 5-3b.

§ 5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate servo loop gain. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (Hex), the completion of AGCNTL operation can be confirmed by monitoring the SENS pin. (See Timing Chart 5-4 and "Description of SENS Signals".)

Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.
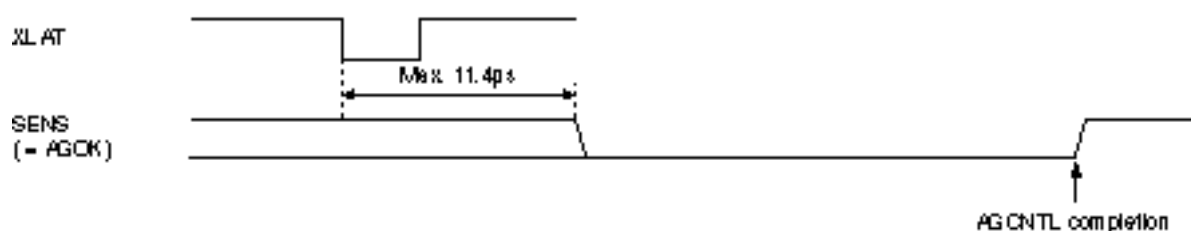
Timing Chart 5-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.

After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings
  The following settings can be changed with $35, $36 and $37.
  FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (Hex)
  TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (Hex)
  AGS;   Self-stop on/off
  AGJ;   Convergence completion judgment time
  AGGF;   Internally generated sine wave amplitude (AGF)
  AGGT;   Internally generated sine wave amplitude (AGT)
  AGV1;   AGCNTL sensitivity 1 (during rough adjustment)
  AGV2;   AGCNTL sensitivity 2 (during fine adjustment)
  AGHS;   Rough adjustment on/off
  AGHT;   Fine adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to FG0 and TG6 to TG0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.

In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.

In the second stage, the AGCNTL coefficient is finely adjusted with relatively low sensitivity to further approach the appropriate value. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD3068Q confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self stop mode) This self-stop mode can be canceled by setting AGS to 0.

In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.

An example of AGCNTL coefficient transitions during AGCNTL operation with various settings is shown in Fig. 5-5.
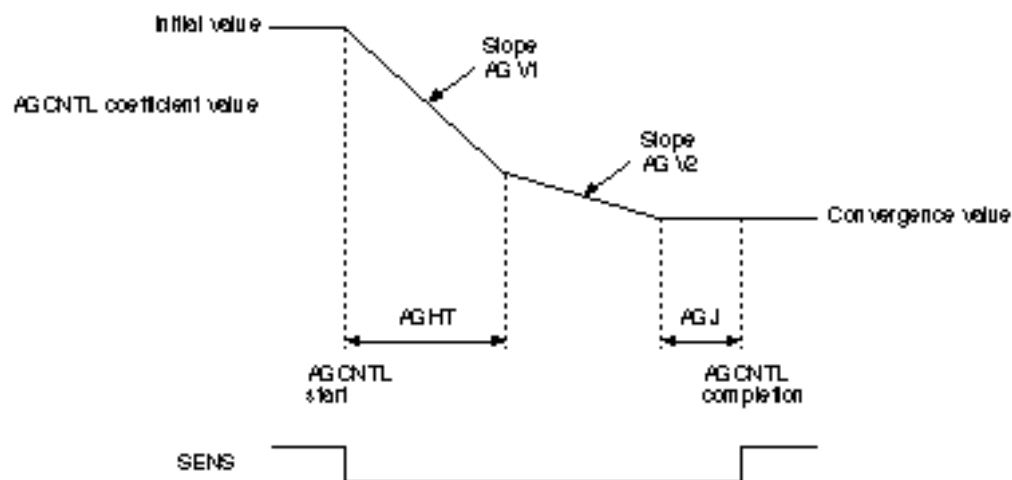

Fig. 5-5.

Note) Fig. 5-5 shows the case where the AGCNTL coefficient converges from the initial value to a smaller value.

§ 5-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 5-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 * *	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 * *	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 * 0 *	FOCUS SERVO OFF, 0V OUT
			0 * 1 *	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 * 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 * 1 1	FOCUS SEARCH VOLTAGE UP

Table 5-6.

*: Don't care

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search operation.
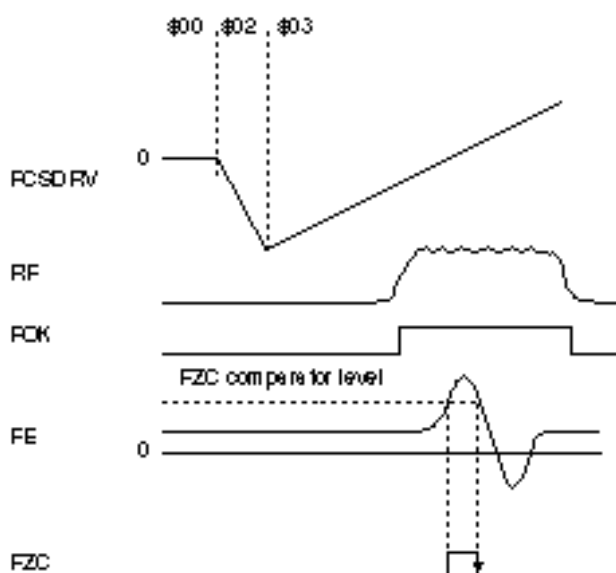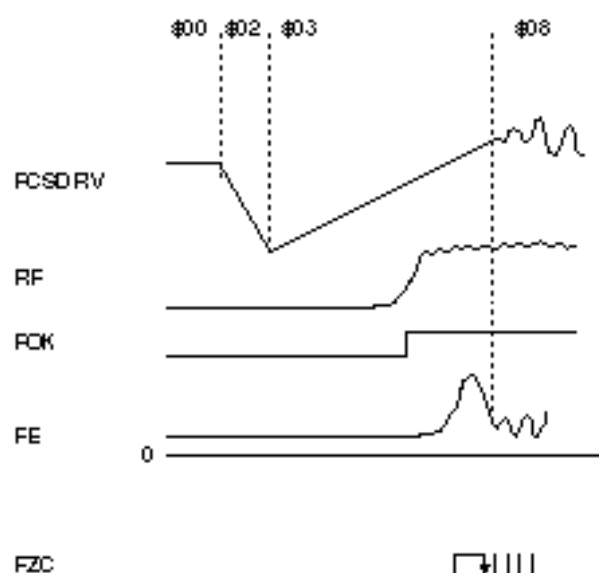Fig. 5-8 shows the signals for sending $08 (FCS on) after that.

Fig. 5-7.

Fig. 5-8.

§ 5-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command $2X. (See Table 5-9.)

When the upper 4 bits of the serial data are 2 (Hex), TZC is output to the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 ∗ ∗	TRACKING SERVO OFF
			0 1 ∗ ∗	TRACKING SERVO ON
			1 0 ∗ ∗	FORWARD TRACK JUMP
			1 1 ∗ ∗	REVERSE TRACK JUMP
			∗ ∗ 0 0	SLED SERVO OFF
			∗ ∗ 0 1	SLED SERVO ON
			∗ ∗ 1 0	FORWARD SLED MOVE
			∗ ∗ 1 1	REVERSE SLED MOVE

Table 5-9.   ∗: Don't care

TRK Servo

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of $36.

In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter switches to gain-up mode. The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.

The CXD3068Q has 2 types of gain-up filter structures in TRK gain-up mode which can be selected by setting D16 of $1. (See Table 5-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of $37, is determined by multiplying this value by 1×, 2×, 3×, or 4× magnification set using D17 and D16 when D18 = D19 = 0 is set with $3. (See Table 5-10.)

SLD MOV must be performed continuously for 50μs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off. These operations are disabled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 5-10.

§ 5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.

An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.

The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 5-11.)

The bottom hold speed and mirror sensitivity can be selected from 4 values using D7 and D6, and D5 and D4, respectively, of $3C.
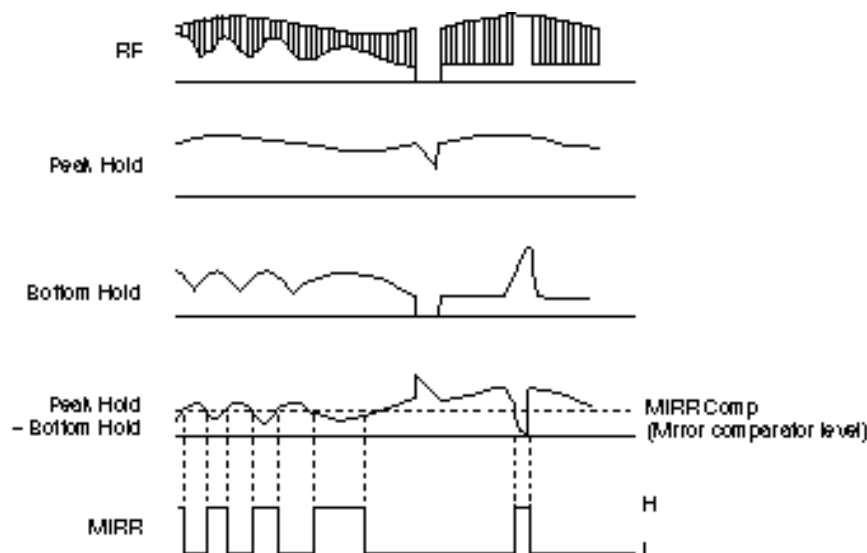
Fig. 5-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)

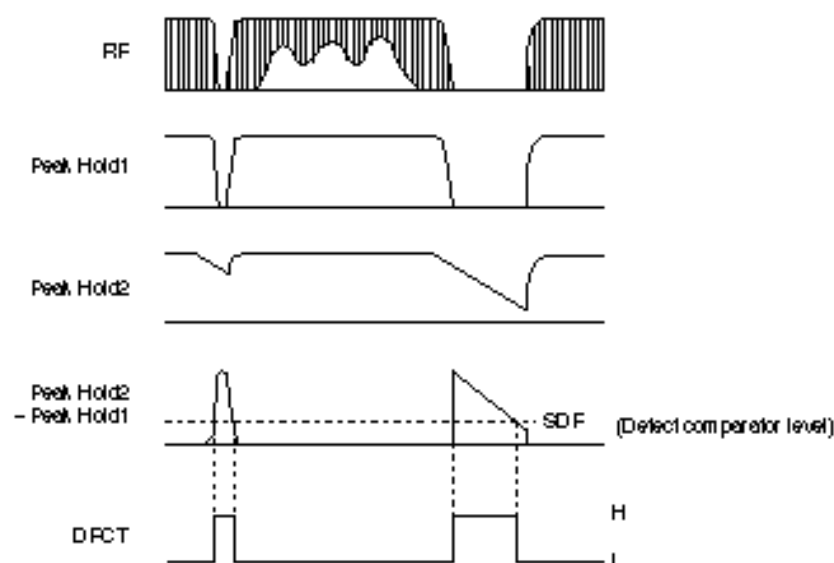The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

Fig. 5-12.

§ 5-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, these operations are achieved by detecting scratches and defects with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)

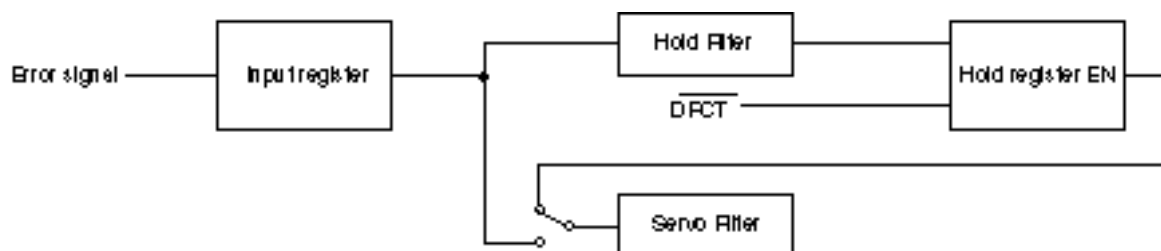In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1.

Fig. 5-13.

§ 5-11. Anti-Shock Circuit

When vibrations occur in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 5-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 4 bits of the command register are 1 (Hex), vibration detection can be monitored from the SENS pin.

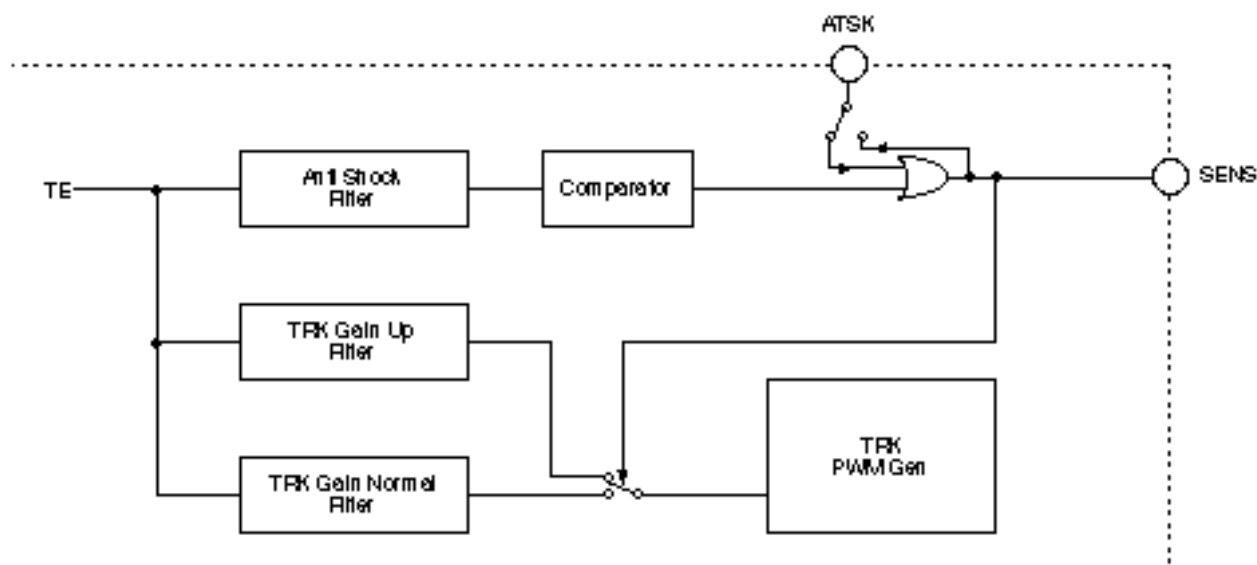It also can be monitored from the ATSK pin by setting the ASOT command of $3F to 0.

Fig. 5-14.

§ 5-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, the brake circuit uses the tracking drive as a brake by cutting the unnecessary portions utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Fig. 5-17.)

In addition, the low frequency for the tracking drive after masking can be boosted. (SFBK1, 2 of $34B)
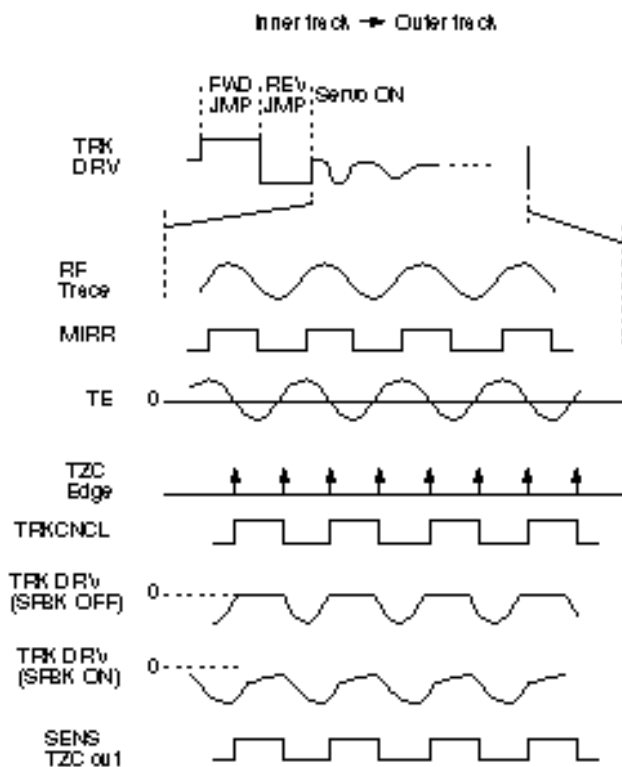
Fig. 5-15.
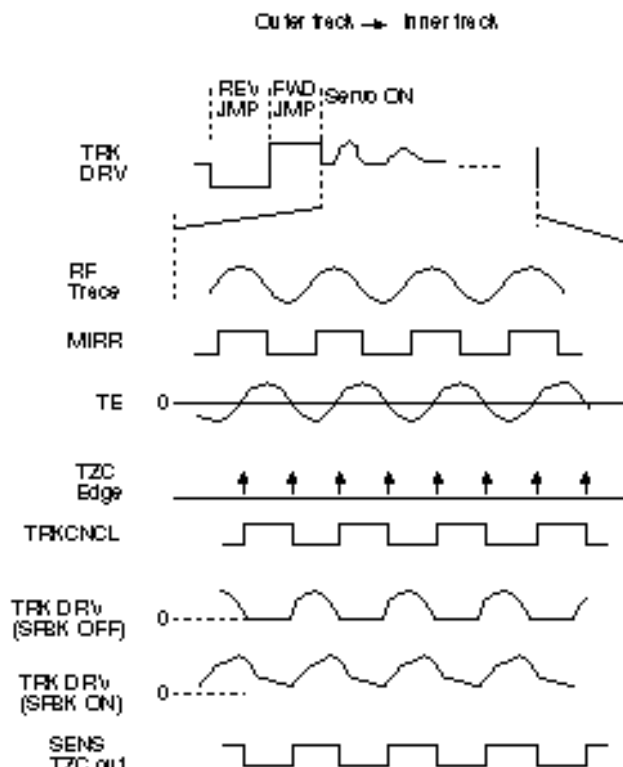
Fig. 5-16.

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 ∗ ∗	ANTI SHOCK ON
			0 ∗ ∗ ∗	ANTI SHOCK OFF
			∗ 1 ∗ ∗	BRAKE ON
			∗ 0 ∗ ∗	BRAKE OFF
			∗ ∗ 0 ∗	TRACKING GAIN NORMAL
			∗ ∗ 1 ∗	TRACKING GAIN UP
			∗ ∗ ∗ 1	TRACKING GAIN UP FILTER SELECT 1
			∗ ∗ ∗ 0	TRACKING GAIN UP FILTER SELECT 2

∗: Don't care

Table 5-17.

§ 5-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. The used TZC signal can be selected from among three different phases according to the COUT signal application.

- HPTZC: For 1-track jumps
  Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cutoff 1kHz digital HPF; when MCK = 128Fs.)
- STZC: For COUT generation when MIRR is externally input and for applications other than COUT generation. This is generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
- DTZC: For high-speed traverse
  Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.

The COUT signal output method is switched with D15 and D14 of $3C.

When D15 = 1: STZC
When D15 = 0 and D14 = 0: HPTZC
When D15 = 0 and D14 = 1: DTZC
When DTZC is selected, the delay can be selected from two values with D14 of $36.

§ 5-14. Serial Readout Circuit

The following measurement and adjustment results can be read out from the SENS pin by inputting the readout clock to the SCLK pin by $39. (See Fig. 5-18, Table 5-19 and "Description of SENS Signals".)

Specified commands

$390C: VC AVRG measurement result $3953: FCS AGCNTL coefficient result
$3908: FE AVRG measurement result $3963: TRK AGCNTL coefficient result
$3904: TE AVRG measurement result $391C: TRVSC adjustment result
$391F: RF AVRG measurement result $391D: FBIAS register value
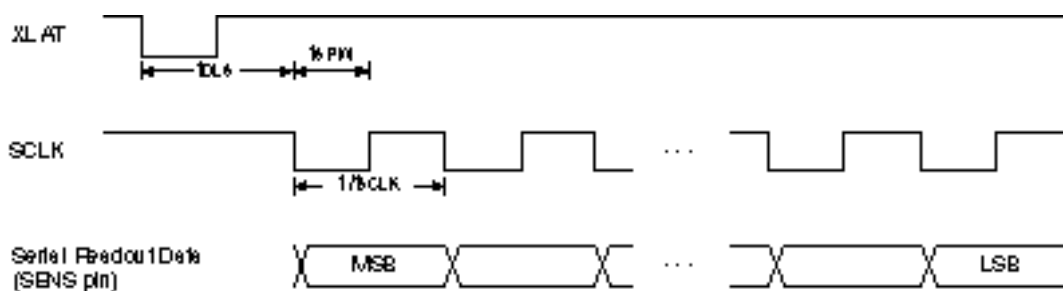
Fig. 5-18.

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

Table 5-19.

During readout, the upper 8 bits of the command register must be 39 (Hex).

§ 5-15. Writing to Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data. Coefficient rewriting is completed 11.3µs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients, be sure to wait 11.3µs (when MCK = 128Fs) before sending the next rewrite command.

§ 5-16. PWM Output

FCS, TRK and SLD PWM format outputs are described below.

In particular, FCS and TRK use a double oversampling noise shaper.

Timing Chart 5-20 and Fig. 5-21 show examples of output waveforms and drive circuits.

$$t_{MCK} = \frac{1}{5.6448MHz} \approx 180ns$$
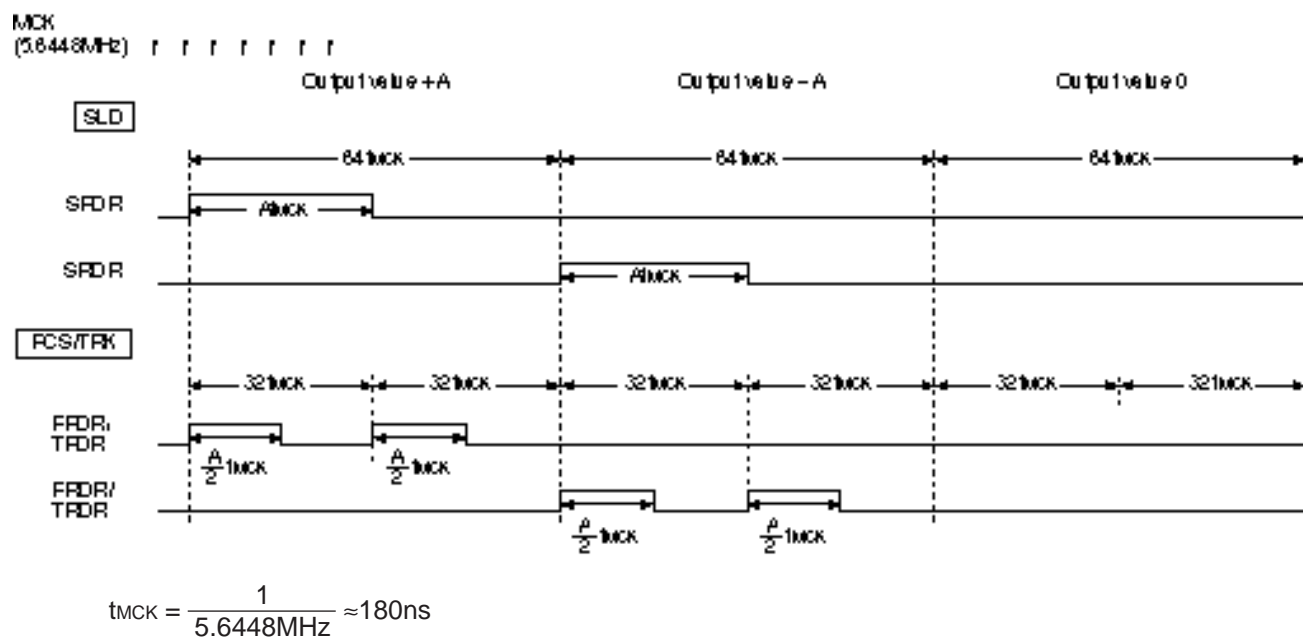
Timing Chart 5-20.
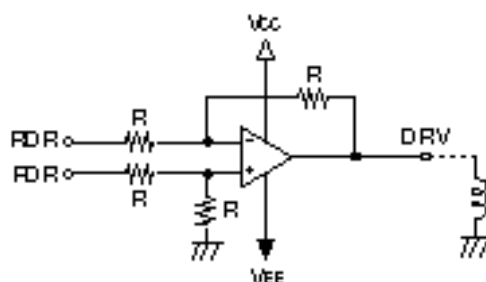
Fig. 5-21. Drive Circuit

§ 5-17. Servo Status Changes Produced by LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.

Setting D6 (LKSW) of $38 to 1 deactivates this function.

In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.

This enables microcomputer control.

§ 5-18. Description of Commands and Data Sets

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0.
  KA6 to KA0: Coefficient address
  KD7 to KD0: Coefficient data

$348 (preset: $348000)

| D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PGFS1	PGFS0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0

These commands set the GFS pin hold time. The hold time is inversely proportional to the playback speed.

PGFS1	PGFS0	Processing
0	0	High when the frame sync is of the correct timing, low when not the correct timing.
0	1	High when the frame sync is of the correct timing, low when continuously not the correct timing for 2ms or longer.
1	0	High when the frame sync is of the correct timing, low when continuously not the correct timing for 4ms or longer.
1	1	High when the frame sync is the correct timing, low when continuously not the correct timing for 8ms or longer.

These commands set the FOK hold time. See $3B for the FOK slice level.

These are the values when MCK = 128Fs, and the hold time is inversely proportional to the MCK setting.

PFOK1	PFOK0	Processing
0	0	High when the RFDC value is higher than the FOK slice level, low when lower than the FOK slice level.
0	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 4.35ms or more.
1	0	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 10.16ms or more.
1	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 21.77ms or more.

MRS: Switches the time constant for the MIRR comparator level generation of the MIRR generation circuit.
When MRS = 0, the time constant is set to normal. (default)
When MRS = 1, the time constant is delayed compared to the normal state.
The duration of MIRR = high, which is caused by the affection of the RFDC signal pulse-formed noise and the like, is suppressed by setting MRS to 1.

MRT1, 0:   These commands limit the time while MIRR = high.

	MRT1	MRT0	MIRR maximum time [ms]
*	0	0	No time limit
	0	1	1.10
	1	0	2.20
	1	1	4.00

∗: preset

$34B (preset: $34B000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0

The low frequency can be boosted for brake operation.
See "§ 5-12 for brake operation".

SFBK1: When 1, brake operation is performed by setting the LowBooster-1 input to 0.
      This is valid only when TLB1ON = 1. The preset is 0.
SFBK2: When 1, brake operation is performed by setting the LowBooster-2 input to 0.
      This is valid only when TLB2ON = 1. The preset is 0.

$34C (preset: $34C000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	THB ON	FHB ON	TLB1 ON	FLB1 ON	TLB2 ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0

These commands turn on the boost function. (See "§ 5-20. Filter Composition".)
There are five boosters (three for the TRK filter and two for the FCS filter) which can be turned on and off independently.

THBON: When 1, the high frequency is boosted for the TRK filter. Preset when 0.
FHBON: When 1, the high frequency is boosted for the FCS filter. Preset when 0.
TLB1ON: When 1, the low frequency is boosted for the TRK filter. Preset when 0.
FLB1ON: When 1, the low frequency is boosted for the FCS filter. Preset when 0.
TLB2ON: When 1, the low frequency is boosted for the TRK filter. Preset when 0.

The difference between TLB1ON and TLB2ON is the position where the low frequency is boosted.
For TLB1ON, the low frequency is boosted before the TRK jump, and for TLB2ON, after the TRK jump.

The following commands set the boosters. (See "§ 5-20. Filter Composition".)

HBST1, HBST0: TRK and FCS HighBooster setting.
              HighBooster has the configuration shown in Fig. 5-24a, and can select three different combinations of coefficients BK1, BK2 and BK3. (See Table 5-25a.)
              An example of characteristics is shown in Fig. 5-26a.
              These characteristics are the same for both the TRK and FCS filters.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB1S1, LB1S0: TRK and FCS LowBooster-1 setting.
              LowBooster-1 has the configuration shown in Fig. 5-24b, and can select three different combinations of coefficients BK4, BK5 and BK6. (See Table 5-25b.)
              An example of characteristics is shown in Fig. 5-26b.
              These characteristics are the same for both the TRK and FCS filters.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB2S1, LB2S0: TRK LowBooster-2 setting.
              LowBooster-2 has the configuration shown in Fig. 5-24c, and can select three different combinations of coefficients BK7, BK8 and BK9. (See Table 5-25c.)
              An example of characteristics is shown in Fig. 5-26c.
              This booster is used exclusively for the TRK filter.
              The sampling frequency is 88.2kHz (when MCK = 128Fs).

              Note) Fs = 44.1kHz
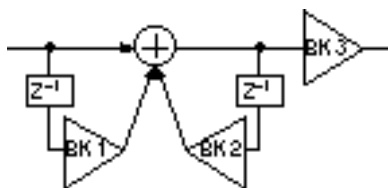
Fig. 5-24a.

HBST1	HBST0	HighBooster setting		
		BK1	BK2	BK3
0	—	−120/128	96/128	2
1	0	−124/128	112/128	2
1	1	−126/128	120/128	2

Table 5-25a.
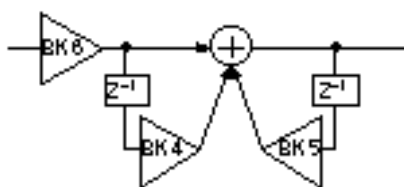
Fig. 5-24b.

LB1S1	LB1S0	LowBooster-1 setting		
		BK4	BK5	BK6
0	—	−255/256	1023/1024	1/4
1	0	−511/512	2047/2048	1/4
1	1	−1023/1024	4095/4096	1/4

Table 5-25b.
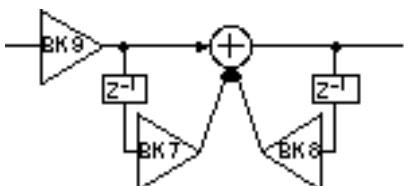
Fig. 5-24c.

LB2S1	LB2S0	LowBooster-2 setting		
		BK7	BK8	BK9
0	—	−255/256	1023/1024	1/4
1	0	−511/512	2047/2048	1/4
1	1	−1023/1024	4095/4096	1/4

Table 5-25c.
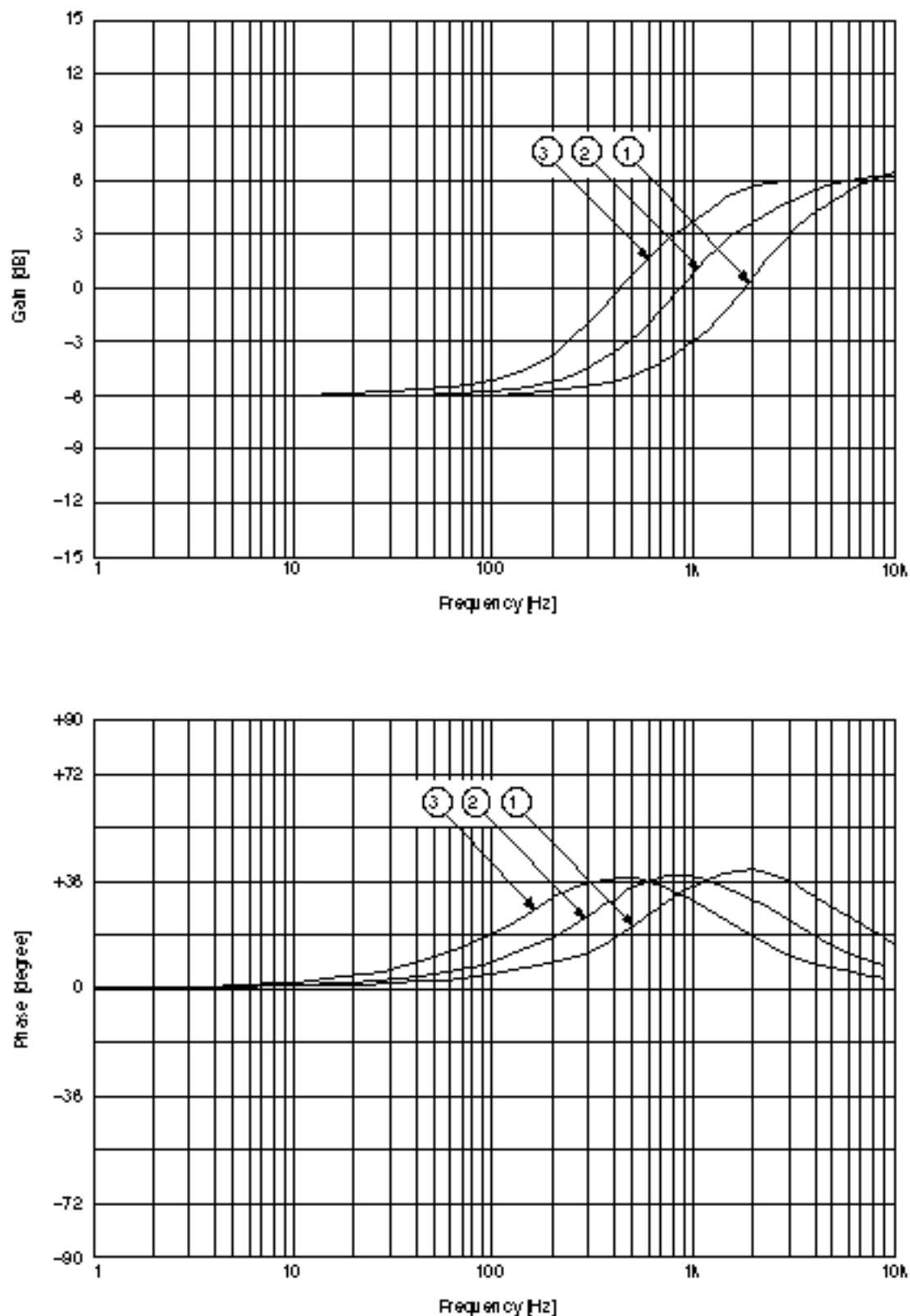
Fig. 5-26a. Servo HighBooster Characteristics [FCS, TRK] (MCK = 128Fs)

① HBST1 = 0   ② HBST1 = 1, HBST0 = 0   ③ HBST1 = 1, HBST0 = 1
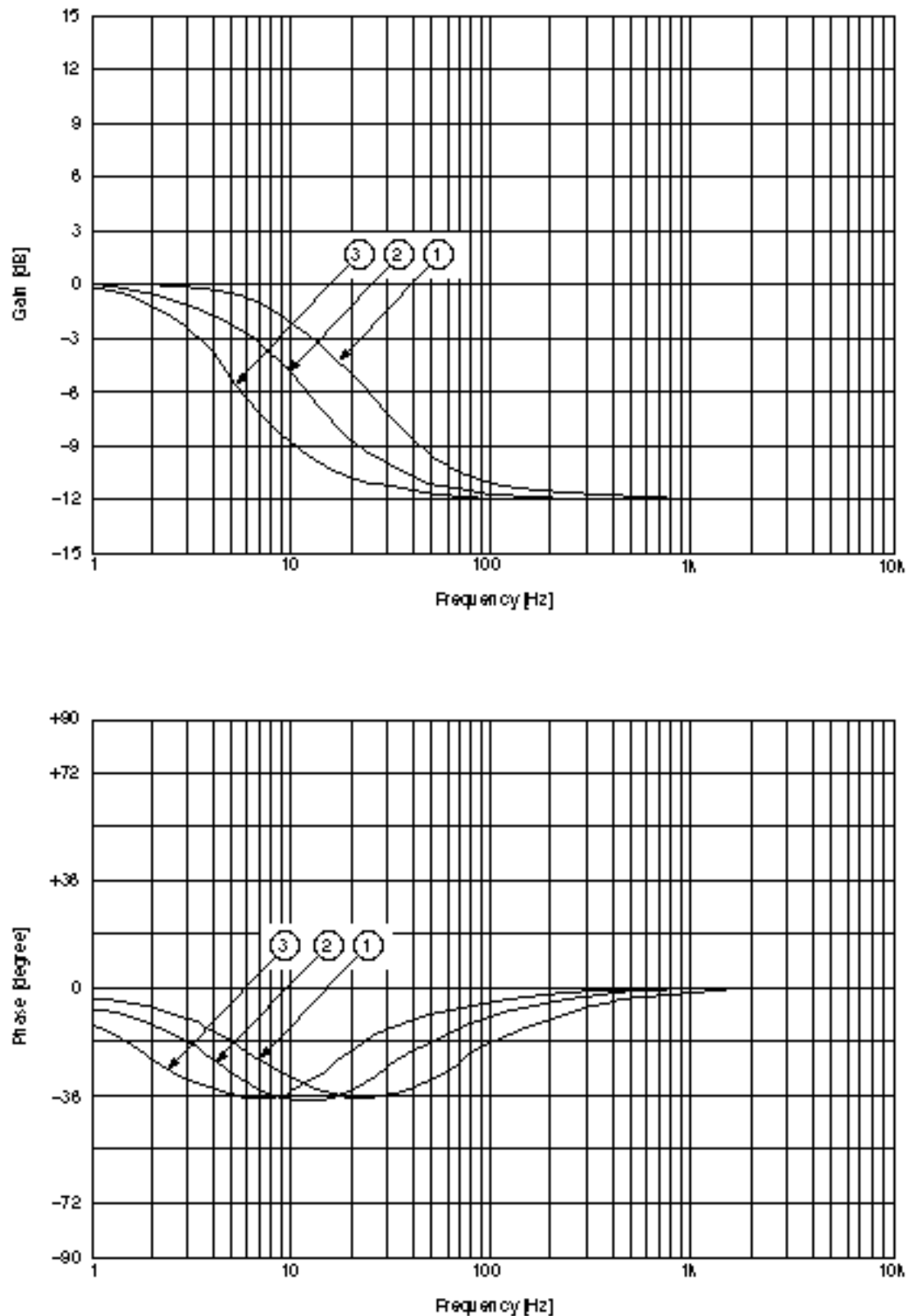
Fig. 5-26b. Servo LowBooster1 Characteristics [FCS, TRK] (MCK = 128Fs)

① LB1S1 = 0   ② LB1S1 = 1, LB1S0 = 0   ③ LB1S1 = 1, LB1S0 = 1
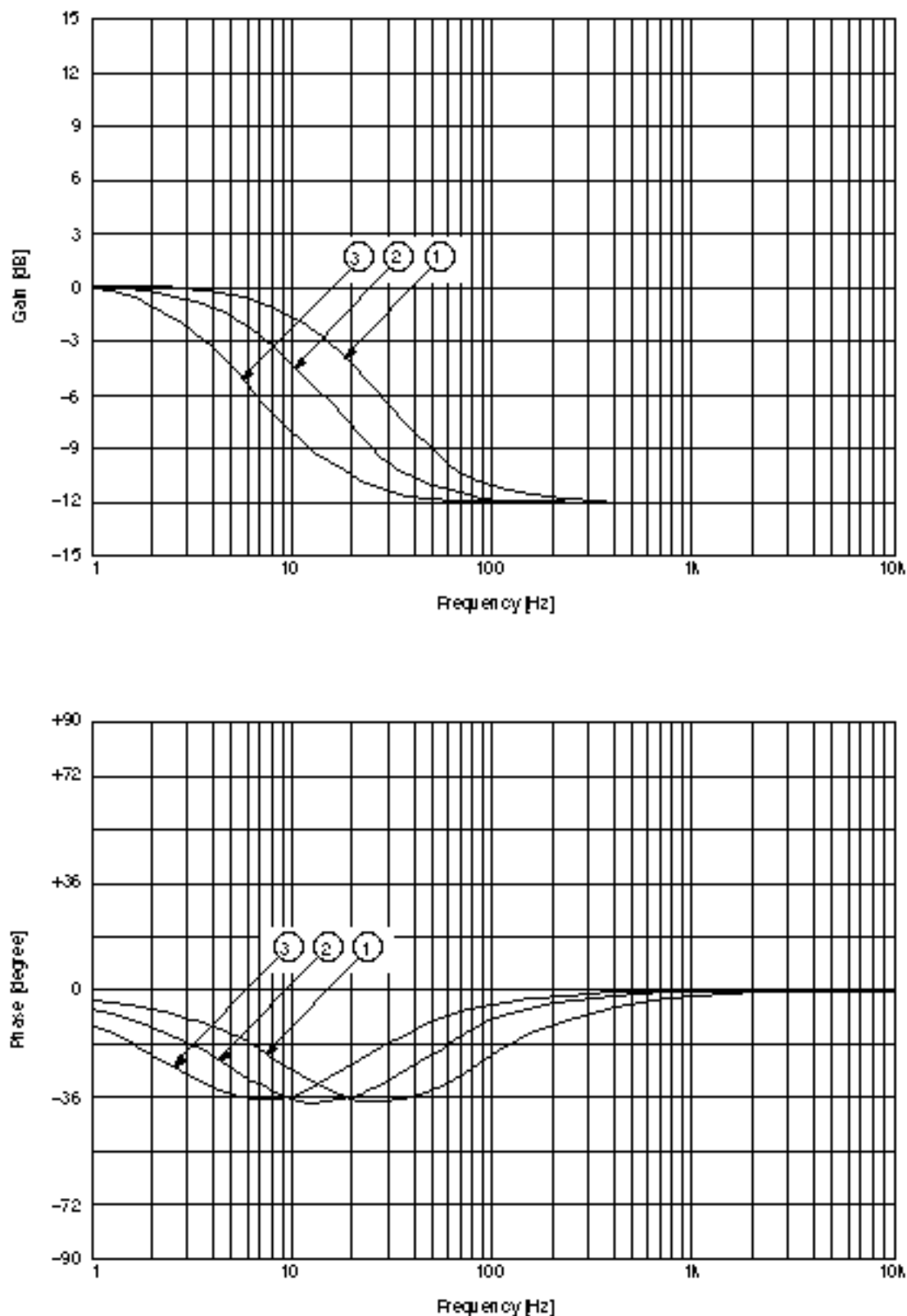
Fig. 5-26c. Servo LowBooster2 Characteristics [FCS, TRK] (MCK = 128Fs)

① LB2S1 = 0   ② LB2S1 = 1, LB2S0 = 0   ③ LB2S1 = 1, LB2S0 = 1

$34E (preset: $34E000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	IDFSL3	IDFSL2	IDFSL1	IDFSL0	0	0	IDFT1	IDFT0	0	0	0	0

IDFSL3: The new DFCT detection is output.

When IDFSL3 = 0, only DFCT in §5-9 is detected and the signal is output from the DFCT pin. (default)

When IDFSL3 = 1, DFCT in §5-9 and new DFCT are switched and the resulting signal is output from the DFCT pin.

The timing for switching is as follows;

When DFCT in §5-9 = low, the new DFCT signal is output from the DFCT pin.

When DFCT in §5-9 = high, DFCT in $5-9 is output from the DFCT pin.

After DFCT in §5-9 is switched to low, the time when the new DFCT output is enabled can be set. (See IDFT1 and IDFT0 of $34E.)

IDFSL3	DFCT in $5-9	DFCT pin
0	L	DFCT in §5-9
0	H	DFCT in §5-9
1	L	New DFCT
1	H	DFCT in §5-9

IDFSL2: The new DFCT detection time is set.

After the new DFCT is detected, DFCT=high is held for a specific time. This time is set.

When IDFSL2 = 0, long hold time. (default)

When IDFSL2 = 1, short hold time.

IDFSL1: The new DFCT detection sensitivity is set.

When IDFSL1 = 0, high detection sensitivity. (default)

When IDFSL1 = 1, low detection sensitivity.

IDFSL0: The new DFCT cancel sensitivity is set.

When IDFSL0 = 0, high cancel sensitivity is set. (default)

When IDFSL0 = 1, low cancel sensitivity is set.

IDFT1, 0: After DFCT in §5-9 is switched to low, the time when the new DFCT output is enabled (output prohibit time) is set.

	IDFT1	IDFT0	New DFCT signal output prohibit time
∗	0	0	204.08μs
	0	1	294.78μs
	1	0	408.16μs
	1	1	612.24μs

∗: preset

$34F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)

    D10 = 0

    FBIAS LIMIT register write

    FBL9 to FBL1: Data;   data compared with FB9 to FB1, FBL9 = MSB.

                   When using the FBIAS register in counter mode, counter operation stops when the

                   value of FB9 to FB1 matches with FBL9 to FBL1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1 ($34F)

    D11 = 0, D10 = 1

    FBIAS register write

    FB9 to FB1: Data; two's complement data, FB9 = MSB.

                   For FE input conversion, FB9 to FB1 = 011111111 corresponds to $255/256 \times V_{DD}/4$ and

                   FB9 to FB1 = 100000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD}: supply voltage)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1 ($34F)

    D11 = 0, D10 = 0

    TRVSC register write

    TV9 to TV0: Data; two's complement data, TV9 = MSB.

                   For TE input conversion, TV9 to TV0 = 0011111111 corresponds to $255/256 \times V_{DD}/4$ and

                   TV9 to TV0 = 1100000000 to $-256/256 \times V_{DD}/4$ respectively. (V_{DD}: supply voltage)

Note) • When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to

      each bit TV8 to TV0 during external write are read out.

    • When reading out internally measured values and then writing these values externally, set TV9 the

      same as TV8.

$35 (preset: $35 58 2D)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed

Default value: 010 ($0.673 \times V_{DD}$ V/s)

Focus drive output conversion

	FT1	FT0	FTZ	Focus search speed [V/s]
	0	0	0	$1.35 \times V_{DD}$
*	0	1	0	$0.673 \times V_{DD}$
	1	0	0	$0.449 \times V_{DD}$
	1	1	0	$0.336 \times V_{DD}$
	0	0	1	$1.79 \times V_{DD}$
	0	1	1	$1.08 \times V_{DD}$
	1	0	1	$0.897 \times V_{DD}$
	1	1	1	$0.769 \times V_{DD}$

$*$: preset, V_{DD}: PWM driver supply voltage

FS5 to FS0:   Focus search limit voltage

Default value: 011000 ($(1\pm24/64) \times V_{DD}/2$, V_{DD}: PWM driver supply voltage)

Focus drive output conversion

FG6 to FG0:   AGF convergence gain setting value

Default value: 0101101

$36 (preset: $36 0E 2E)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0

TDZC: Selects the TZC signal for generating the TRKCNCL signal during brake circuit operation.

TDZC = 0: The edge of the HPTZC or STZC signal, whichever has the faster phase, is used.

TDZC = 1: The edge of the HPTZC or STZC signal or the tracking drive signal zero-cross, whichever has the fastest phase, is used. (See § 5-12.)

DTZC: DTZC delay (8.5/4.25μs, when MCK = 128Fs)

Default value: 0 (4.25μs)

TJ5 to TJ0:   Track jump voltage

Default value: 001110 ($(1\pm14/64) \times V_{DD}/2$, V_{DD}: PWM driver supply voltage)

Tracking drive output conversion

SFJP: Surf jump mode on/off

The tracking PWM output is generated by adding the tracking filter output and TJReg (TJ5 to 0), by setting D7 to 1 (on)

TG6 to TG0:   AGT convergence gain setting value

Default value: 0101110

$37 (preset: $37 50 BA)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level

Default value: 01 ($1/8 \times V_{DD}/2$, V_{DD}: supply voltage); FE input conversion

	FZSH	FZSL	Slice level
	0	0	$1/4 \times V_{DD}/2$
*	0	1	$1/8 \times V_{DD}/2$
	1	0	$1/16 \times V_{DD}/2$
	1	1	$1/32 \times V_{DD}/2$

∗: preset

SM5 to SM0: Sled move voltage

Default value: 010000 (($1\pm16/64) \times V_{DD}/2$, V_{DD}: PWM driver supply voltage)

Sled drive output conversion

AGS: AGCNTL self-stop on/off

Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms, when MCK = 128Fs)

Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small)	$1/32 \times V_{DD}/2$
	1 (large)∗	$1/16 \times V_{DD}/2$
AGGT	0 (small)	$1/16 \times V_{DD}/2$
	1 (large)∗	$1/8 \times V_{DD}/2$

∗: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low

Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low

Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off

Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)

Default value: 0 (256ms)

$38 (preset: $38 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

DC offset cancel. See §5-3.

*VCLM: VC level measurement (on/off)

 VCLC: VC level compensation for FCS In register (on/off)

*FLM: Focus zero level measurement (on/off)

 FLC0: Focus zero level compensation for FZC register (on/off)

*RFLM: RF zero level measurement (on/off)

 RFLC: RF zero level compensation (on/off)

Automatic gain control. See §5-6.

 AGF: Focus auto gain adjustment (on/off)

 AGT: Tracking auto gain adjustment (on/off)

Misoperation prevention circuit

 DFSW: Defect disable switch (on/off)

   Setting this switch to 1 (on) disables the defect countermeasure circuit.

 LKSW: Lock switch (on/off)

   Setting this switch to 1 (on) disables the sled free-running prevention circuit.

DC offset cancel. See §5-3.

 TBLM: Traverse center measurement (on/off)

*TCLM: Tracking zero level measurement (on/off)

 FLC1: Focus zero level compensation for FCS In register (on/off)

 TLC2: Traverse center compensation (on/off)

 TLC1: Tracking zero level compensation (on/off)

 TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with * are accepted every 2.9ms. (when MCK = 128Fs)

   All commands are on when 1.

$39 (preset: $39 0000)

D15	D14	D13	D12	D11	D10	D9	D8
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0

DAC: Serial data readout DAC mode (on/off)

SD6 to SD0:   Serial readout data select

SD6	SD5	Readout data			Readout data length	
1	Coefficient RAM data for address = SD5 to SD0				8 bits	
0	1	Data RAM data for address = SD4 to SD0			16 bits	
		SD4	SD3 to SD0			
			1 1 1 1	RF AVRG register	8 bits	$399F
			1 1 1 0	RFDC input signal	8 bits	$399E
			1 1 0 1	FBIAS register	9 bits	$399D
		1	1 1 0 0	TRVSC register	9 bits	$399C
			0 0 1 1	RFDC envelope (bottom)	8 bits	$3993
			0 0 1 0	RFDC envelope (peak)	8 bits	$3992
0	0		0 0 0 1	RFDC envelope (peak) – (bottom)	8 bits	$3991
			1 1 ∗ ∗	VC AVRG register	9 bits	$398C
			1 0 ∗ ∗	FE AVRG register	9 bits	$3988
			0 1 ∗ ∗	TE AVRG register	9 bits	$3984
		0	0 0 1 1	FE input signal	8 bits	$3983
			0 0 1 0	TE input signal	8 bits	$3982
			0 0 0 1	SE input signal	8 bits	$3981
			0 0 0 0	VC input signal	8 bits	$3980

∗: Don't care

Note) Coefficients K40 to K4F cannot be read out.

See the Description for "Data Readout" concerning readout methods for the above data.

$3A (preset: $3A 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	FBON	FBSS	FBUP	FBV1	FBV0	FIFZC	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0

FBON: FBIAS (focus bias) register addition (on/off)

The FBIAS register value is added to the signal loaded into the FCS In register by setting FBON = 1 (on).

FBSS: FBIAS (focus bias) register/counter switching

FBSS = 0: register, FBSS = 1: counter.

FBUP: FBIAS (focus bias) counter up/down operation switching

This performs counter up/down control when FBSS = 1. FBUP = 0: down counter, FBUP = 1: up counter.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching

The number of FCS BIAS count-up/-down steps per cycle is decided by these bits.

FBV1	FBV0	Number of steps per cycle
0	0	1
0	1	2
1	0	4
1	1	8

∗ (row: FBV1=0, FBV0=0)

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately $1/2^9 \times V_{DD} \times 0.4$, V_{DD} = supply voltage.

∗: preset

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.

These are effective for increasing the overall gain in order to widen the servo band.

Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

FPS1	FPS0	Relative gain
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

∗ (row: FPS1=0, FPS0=0)

TPS1	TPS0	Relative gain
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

∗ (row: TPS1=0, TPS0=0)

∗: preset

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When INBK = 0 (off), the brake circuit masks the tracking drive signal with TRKCNCL which is generated by fetching the MIRR signal at the TZC edge. When INBK = 1 (on), the tracking filter input is masked instead of the drive output.

MTI0: The tracking filter input is masked when the MIRR signal is high by setting MTI0 = 1 (on).

FIFZC: This selects the FZC slice level setting command.
          When 0, the FZC slice level is determined by the $37 FZSH and FZSL setting values. (default)
          When 1, the FZC slice level is determined by the $3F8 FIFZB3 to FIFZB0 and FIFZA3 to
          FIFZA0 setting values.
          This allows more detailed setting and the addition of hysteresis compared to the $37 FZSH and
          FZSL setting.

$3B (preset: $3B E0 50)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 ($28/256 \times V_{DD}/2$, V_{DD} = supply voltage)

RFDC input conversion

	SFOX	SFO2	SFO1	Slice level
	0	0	0	$16/256 \times V_{DD}/2$
	0	0	1	$20/256 \times V_{DD}/2$
	0	1	0	$24/256 \times V_{DD}/2$
*	0	1	1	$28/256 \times V_{DD}/2$
	1	0	0	$32/256 \times V_{DD}/2$
	1	0	1	$40/256 \times V_{DD}/2$
	1	1	0	$48/256 \times V_{DD}/2$
	1	1	1	$56/256 \times V_{DD}/2$

∗: preset

SDF2, SDF1: DFCT slice level

Default value: 10 ($0.0313 \times V_{DD}$)

RFDC input conversion

	SDF2	SDF1	Slice level
	0	0	$0.0156 \times V_{DD}$
	0	1	$0.0234 \times V_{DD}$
*	1	0	$0.0313 \times V_{DD}$
	1	1	$0.0391 \times V_{DD}$

∗: preset, V_{DD}: supply voltage

MAX2, MAX1: DFCT maximum time (MCK = 128Fs)

Default value: 00 (no timer limit)

	MAX2	MAX1	DFCT maximum time
*	0	0	No timer limit
	0	1	2.00ms
	1	0	2.36
	1	1	2.72

∗: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation

On/off (default: off)

On when set to 1.

D2V2, D2V1:   Peak hold 2 for DFCT signal generation
              Count-down speed setting
              Default value: 01 (0.086 × V$_{DD}$/ms, 44.1kHz)

              [V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D2V2	D2V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.0431 × V$_{DD}$	22.05
0	1	0.0861 × V$_{DD}$	44.1
1	0	0.172 × V$_{DD}$	88.2
1	1	0.344 × V$_{DD}$	176.4

∗: preset, V$_{DD}$: supply voltage

D1V2, D1V1:   Peak hold 1 for DFCT signal generation
              Count-down speed setting
              Default value: 01 (0.688 × V$_{DD}$/ms, 352.8kHz)

              [V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D1V2	D2V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.344 × V$_{DD}$	176.4
0	1	0.688 × V$_{DD}$	352.8
1	0	1.38 × V$_{DD}$	705.6
1	1	2.75 × V$_{DD}$	1411.2

∗: preset, V$_{DD}$: supply voltage

RINT: This initializes the initial-state registers of the circuits which generate MIRR, DFCT and FOK.

$3C (preset: $3C 00 80)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0

COSS, COTS: This selects the TZC signal used when generating the COUT signal.
Preset = HPTZC.

	COSS	COTS	TZC
	1	—	STZC
∗	0	0	HPTZC
	0	1	DTZC

∗: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
DTZC is the delayed phase STZC. (The delay time can be selected by D14 of $36.)
HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
See § 5-13.

CETZ: The input from the TE pin normally enters the TRK filter and is used to generate the TZC signal. However, the input from the CE pin can also be used. This function is for the center error servo.
When 0, the TZC signal is generated by using the signal input to the TE pin.
When 1, the TZC signal is generated by using the signal input to the CE pin.

CETF: When 0, the signal input to the TE pin is input to the TRK servo filter.
When 1, the signal input to the CE pin is input to the TRK servo filter.

These commands output the TZC signal.
COT2, COT1: This outputs the TZC signal from the COUT pin.

	COT2	COT1	COUT pin output
	1	—	STZC
	0	1	HPTZC
∗	0	0	COUT

∗: preset, —: don't care

MOT2: The STZC signal is output from the MIRR pin by setting MOT2 to 1.

These commands set the MIRR signal generation circuit.
BTS1, BTS0: This sets the count-up speed for the bottom hold value of the MIRR generation circuit.
The time per step is approximately 708ns (when MCK = 128Fs). The preset value is BTS1 = 1, BTS0 = 0 like the CXD2586R. This is valid only when BTF of $3B is 0.

MRC1, MRC0: This sets the minimum pulse width for masking the MIRR signal of the MIRR generation circuit. As noted in § 5-9, the MIRR signal is generated by comparing the waveform obtained by subtracting the bottom hold value from the peak hold value with the MIRR comparator level. Strictly speaking, however, for MIRR to become high, these levels must be compared continuously for a certain time. This sets that time.
The preset value is MRC1 = 0, MRC0 = 0 like the CXD2586R.

	BTS1	BTS0	Number of count-up steps per cycle
	0	0	1
	0	1	2
∗	1	0	4
	1	1	8

MRC1	MRC0	Setting time [μs]
0	0	5.669∗
0	1	11.338
1	0	22.675
1	1	45.351

∗: preset (when MCK = 128Fs)

$3D (preset: $3D 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0

SFID: SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
               When the low frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.

SFSK: Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, creating a difference in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.

THID: TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
               When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as the TRK hold filter input.

THSK: Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, creating a difference in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.

∗ See "§ 5-20. Filter Composition" regarding the SFID, SFSK, THID and THSK commands.

TLD0 to 2:   This turns on and off SLD filter correction independently of the TRK filter.
               See $38 (TLC0 to 2) and Fig. 5-3.

	TLC2	TLD2	Traverse center correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

	TLC1	TLD1	Tracking zero level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

|	TLC0	TLD0	VC level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

∗: preset, —: don't care

• Input coefficient sign inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the CXD3068Q outputs the servo drives which have the reversed phase to the error inputs..
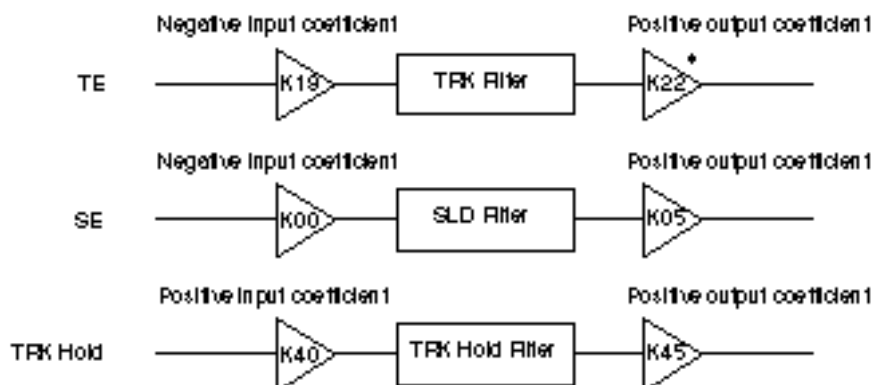
When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so invert the SLD input coefficient (K00) sign. (For example, inverting the sign for coefficient K00: E0Hex results in 20Hex.)
For the same reason, when THID = 1, invert the TRK hold input coefficient (K40) sign.
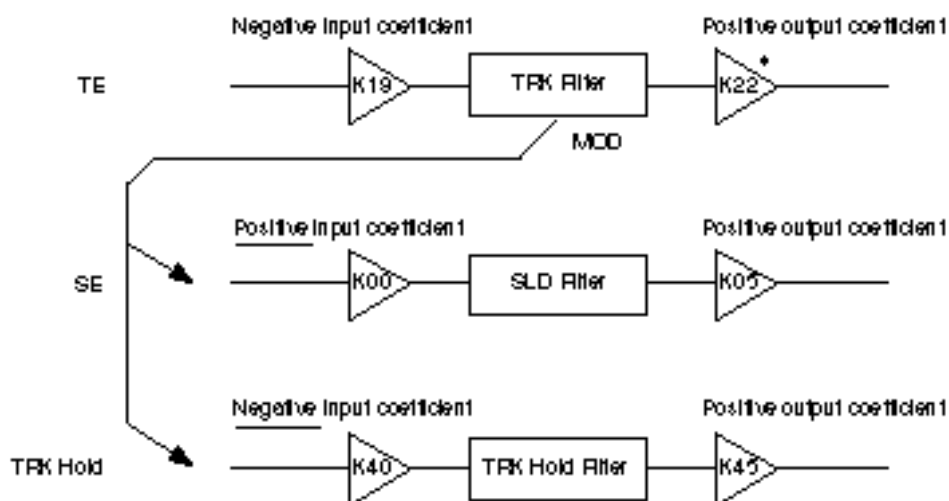
* for TRK servo gain normal
See "§ 5-20. Filter Composition".

$3E (preset: $3E 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when 1; default when 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when 1; default when 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when 1; default when 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when 1; default when 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See "§ 5-20 Filter Composition" at the end of this specification concerning quasi double accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when 1; default when 0

LKIN: When 0, the internally generated LOCK signal is output to the LOCK pin. (default)
When 1, the LOCK signal can be input from an external source to the LOCK pin.

COIN: When 0, the internally generated COUT signal is output to the COUT pin. (default)
When 1, the COUT signal can be input from an external source to the COUT pin.

The MIRR, DFCT and FOK signals can also be input from an external source.

MDFI: When 0, the MIRR, DFCT and FOK signals are generated internally. (default)
When 1, the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.

MIRI: When 0, the MIRR signal is generated internally. (default)
When 1, the MIRR signal can be input from an external source through the MIRR pin.

	MDFI	MIRI	
∗	0	0	MIRR, DFCT and FOK are all generated internally.
	0	1	MIRR only is input from an external source.
	1	—	MIRR, DFCT and FOK are all input from an external source.

∗: preset, —: don't care

XT1D: When XT1D = 1, the input to the servo master clock can be used without dividing its frequency. This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of $3F for XT2D and XT4D.

$3F (preset: $3F 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	0	0	AGHF	0

Note) Be sure to set D4 of $3F to 1 for CXD3068Q.

AGG4:   This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC. When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

AGG4	AGGF	AGGT	Sine wave amplitude	
			FE input conversion	TE input conversion
0	0	—	$1/32 \times V_{DD}/2$	—
	1	—	$1/16 \times V_{DD}/2$	—
	—	0	—	$1/16 \times V_{DD}/2$
	—	1	—	$1/8 \times V_{DD}/2*$
1	0	0	$1/64 \times V_{DD}/2$	
	0	1	$1/32 \times V_{DD}/2$	
	1	0	$1/16 \times V_{DD}/2$	
	1	1	$1/8 \times V_{DD}/2$	

See $37 for AGGF and AGGT.

The presets are AGG4 = 0,

AGGF = 1 and AGGT = 1.

∗: preset, —: don't care

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated. See the description of $3E for XT1D. Also, see the decription of "§5-2. Digital Servo Block Master Clock (MCK)".

	XT1D	XT2D	XT4D	Frequency division ratio
∗	0	0	0	According to XTSL
	1	—	—	1/1
	0	1	—	1/2
	0	0	1	1/4

∗: preset, —: don't care

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
Note) Set DRR1 and DRR0 on for 50μs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, the FCS servo filter is forcibly set to gain normal status.
On when 1; default when 0

AGHF: This halves the frequency of the internally generated sine wave during AGC.

FTQ: The slope of the output during focus search is 1/4 of the conventional output slope.
On when 1; default when 0 .

ASOT: The anti-shock signal, which is internally detected, is output from the ATSK pin.
Output when set to 1; default = 0
Vibration detection when a high signal is output for the anti-shock signal output.

$3F8 (preset: $3F8800)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SYG3	SYG2	SYG1	SYG0	FIFZB3	FIFZB2	FIFZB1	FIFZB0	FIFZA3	FIFZA2	FIFZA1	FIFZA0

SYG3 to SYG0: These simultaneously set the focus drive, tracking drive and sled drive output gains. See the $CX command for the spindle drive output gain setting.

	SYG3	SYG2	SYG1	SYG0	GAIN
	0	0	0	0	0 (−∞dB)
	0	0	0	1	0.125 (−18.1dB)
	0	0	1	0	0.250 (−12.0dB)
	0	0	1	1	0.375 (−8.5dB)
	0	1	0	0	0.500 (−6.0dB)
	0	1	0	1	0.625 (−4.1dB)
	0	1	1	0	0.750 (−2.5dB)
	0	1	1	1	0.875 (−1.2dB)
∗	1	0	0	0	1.000 (0.0dB)
	1	0	0	1	1.125 (+1.0dB)
	1	0	1	0	1.250 (+1.9dB)
	1	0	1	1	1.375 (+2.8dB)
	1	1	0	0	1.500 (+3.5dB)
	1	1	0	1	1.625 (+4.2dB)
	1	1	1	0	1.750 (+4.9dB)
	1	1	1	1	1.875 (+5.5dB)

∗: preset

FIFZB3 to FIFZB0:

This sets the slice level at which FZC changes from high to low.

FIFZA3 to FIFZA0:

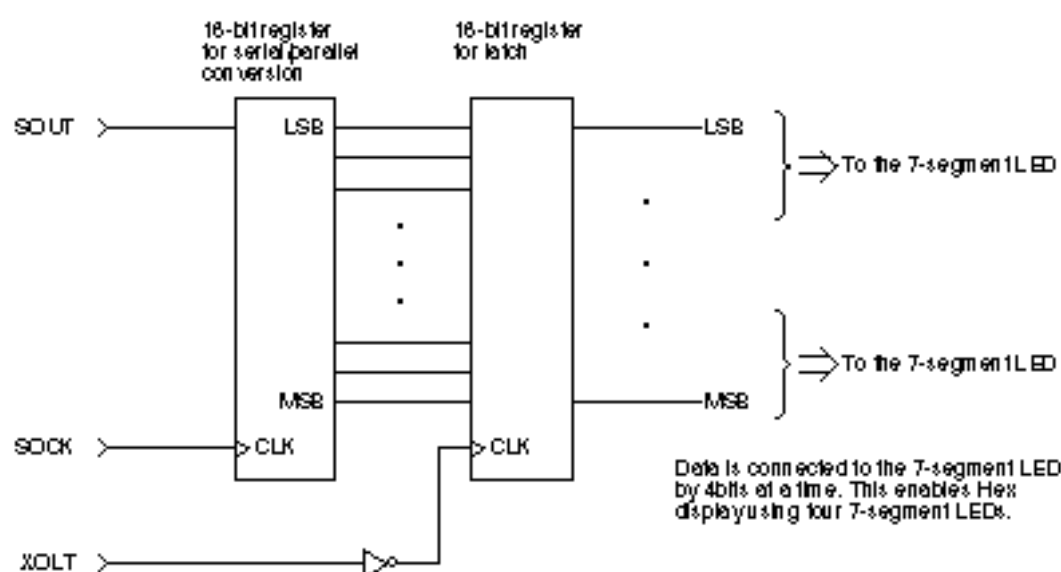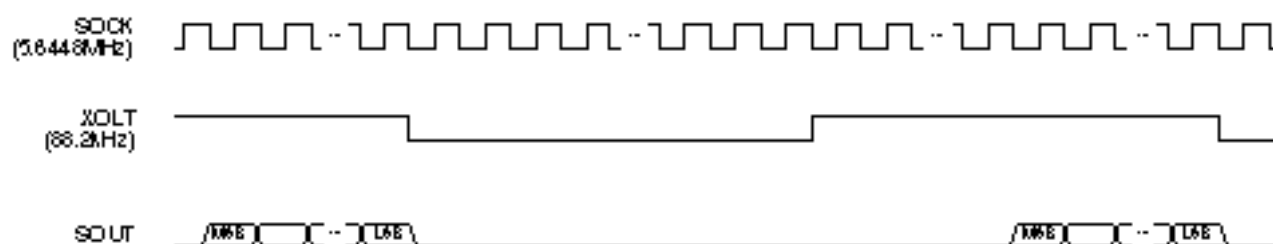This sets the slice level at which FZC changes from low to high.

The FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values are valid only when $3A FIFZC is 1.

Set so that the FIFZB3 to FIFZB0 ≤ FIFZA3 to FIFZA0.

Hysteresis can be added to the slice level by setting FIFZB3 to FIFZB0 < FIFZA3 to FIFZA0.

$$\text{FZC slice level} = \frac{\text{FIFZB3 to FIFZB0 or FIFZA3 to FIFZA0 setting value}}{32} \times 0.5 \times V_{DD} \text{ [V]}$$

Description of Data Readout

Data is connected to the 7-segment1 LED by 4bits at a time. This enables Hex display using four 7-segment1 LEDs.

Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.
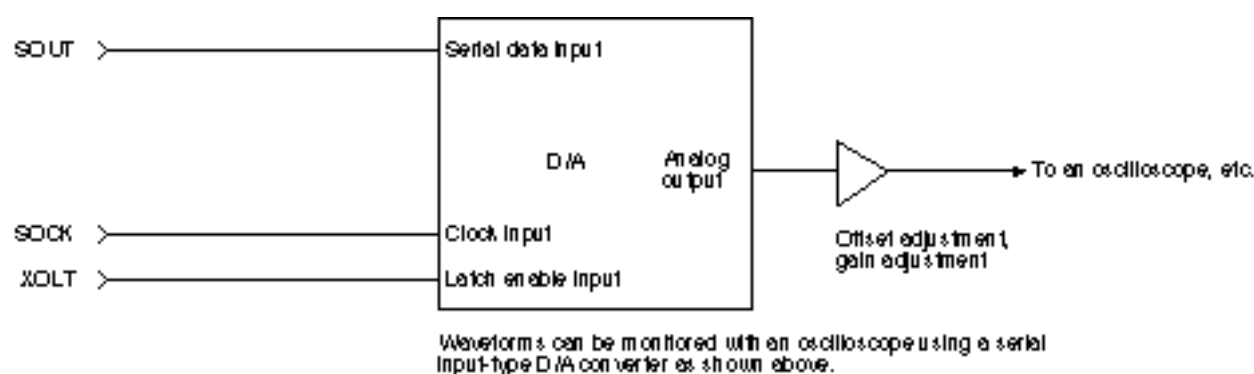
§ 5-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

* Fix indicates that normal preset values should be used.

<Coefficient Preset Value Table (2)>
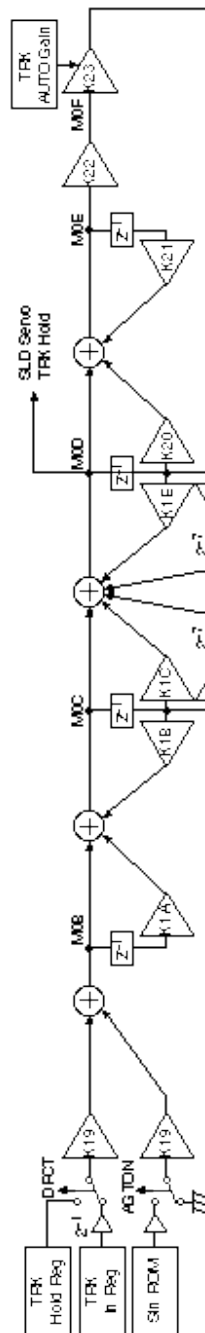
ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

§ 5-20. Filter Composition
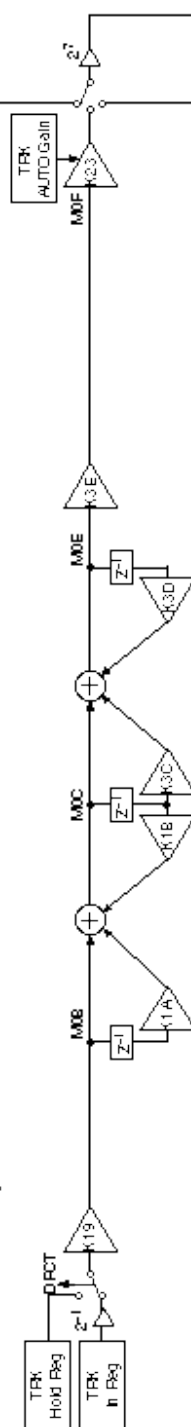The internal filter composition is shown below.
K** and M** indicate coefficient RAM and Data RAM address values respectively.
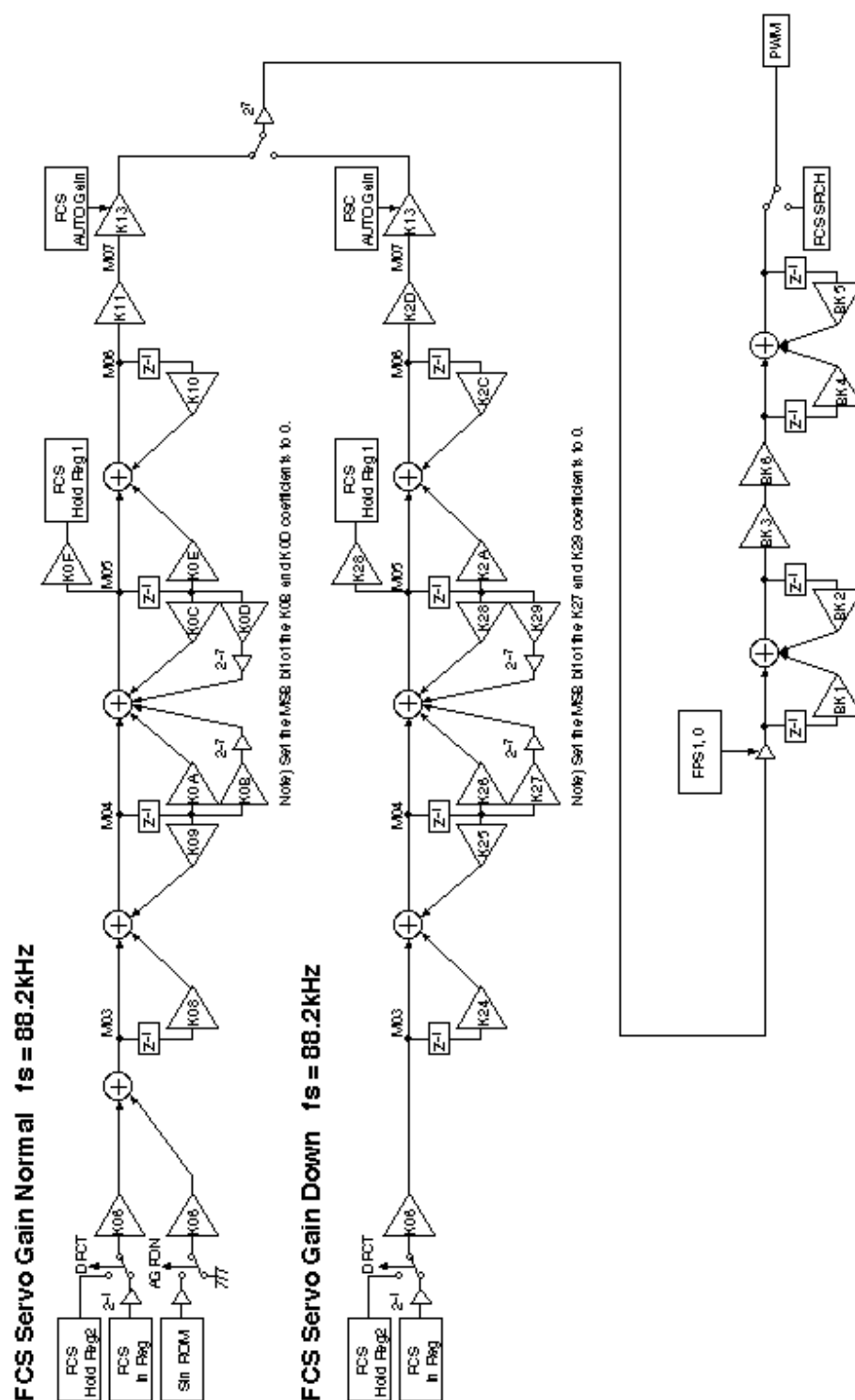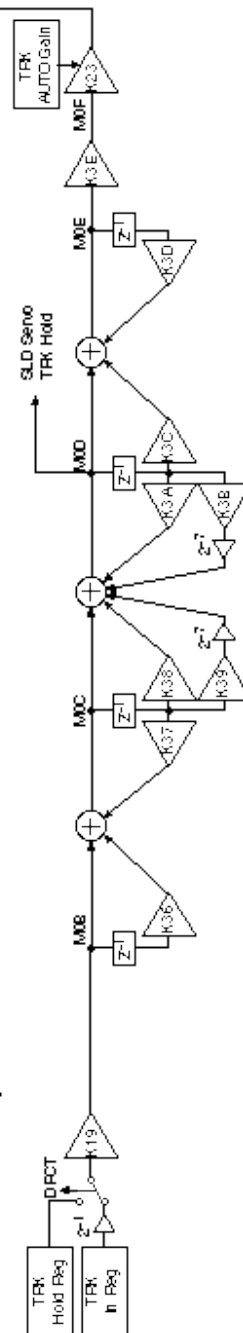
FCS Servo Gain Normal fs = 88.2kHz

FCS Servo Gain Down fs = 88.2kHz

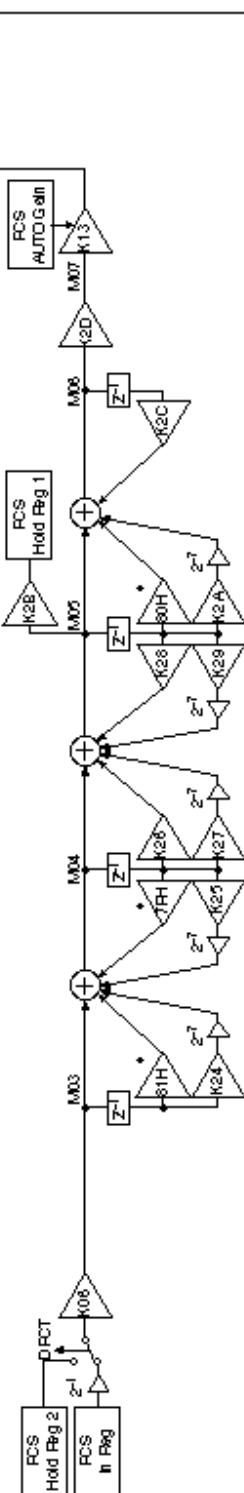FCS Servo Gain Normal 1s = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)

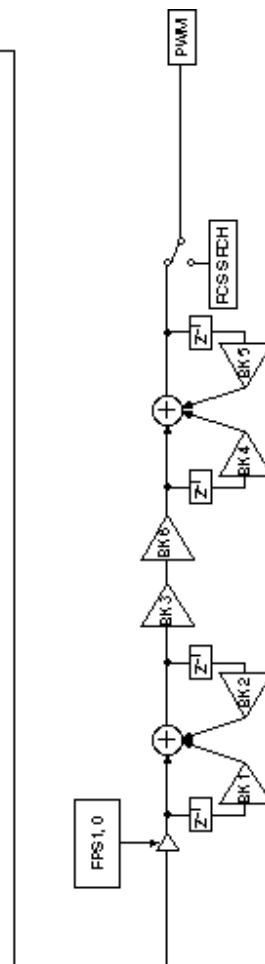FCS Servo Gain Normal 1s = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)
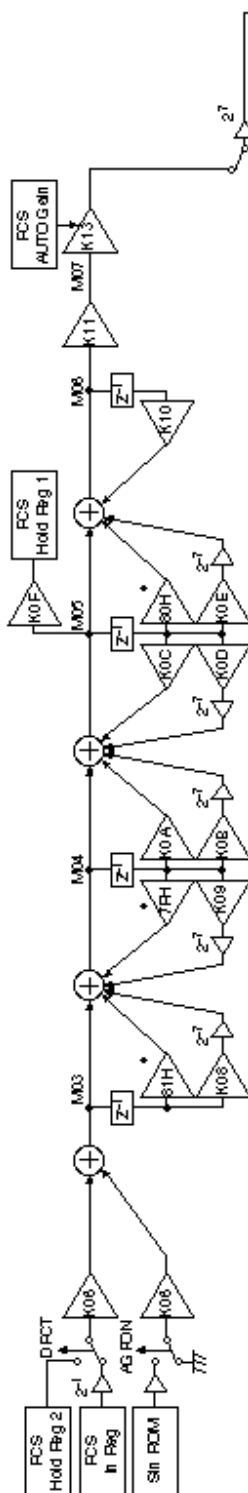
Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K0B, K09 and K0E coefficient s during quasi double accuracy to 0.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficient s during quasi double accuracy to 0.

*81H, 7FH and 80H are each Hex displays bit.
Fixed values when set to quasi double accuracy.

TRK Servo Gain Normal 1s = 88.2kHz, during quasi double accuracy (Ex.: $3EXAX0)

TRK Servo Gain up1 1s = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)

TRK Servo Gain up2 1s = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)
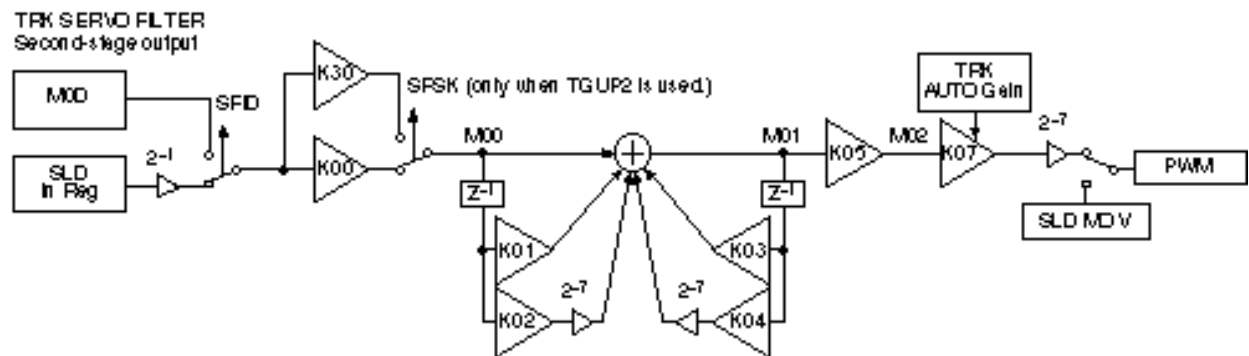
Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K38, K37 and K3C coefficients during quasi double accuracy to 0.

* 81H, 7FH and 80H are each Hex display 8-bit
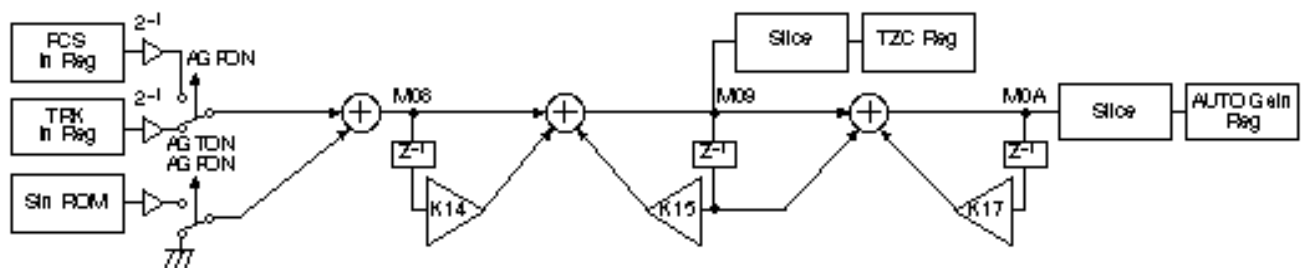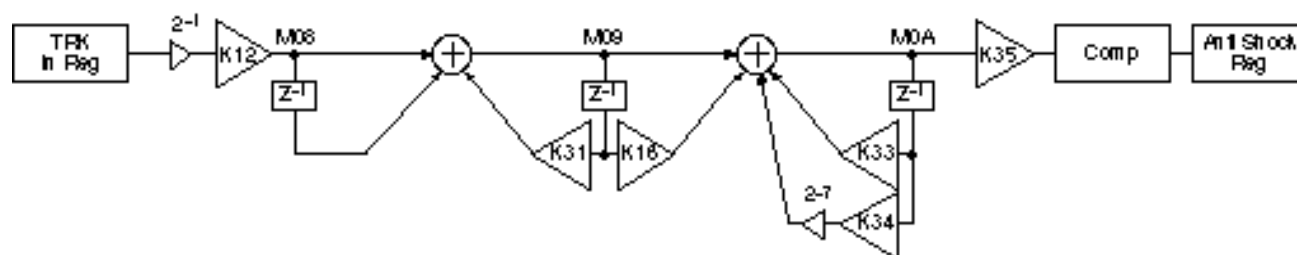fixed values when set to quasi double accuracy.

SLD Servo   fs = 345Hz

Note) Set the MSB bit of the K02 and K04 coefficients to 0.
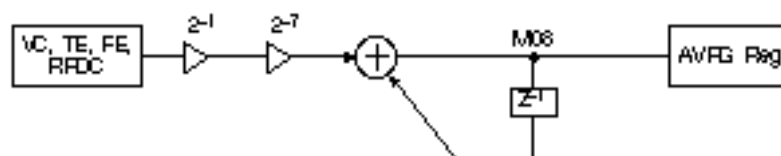
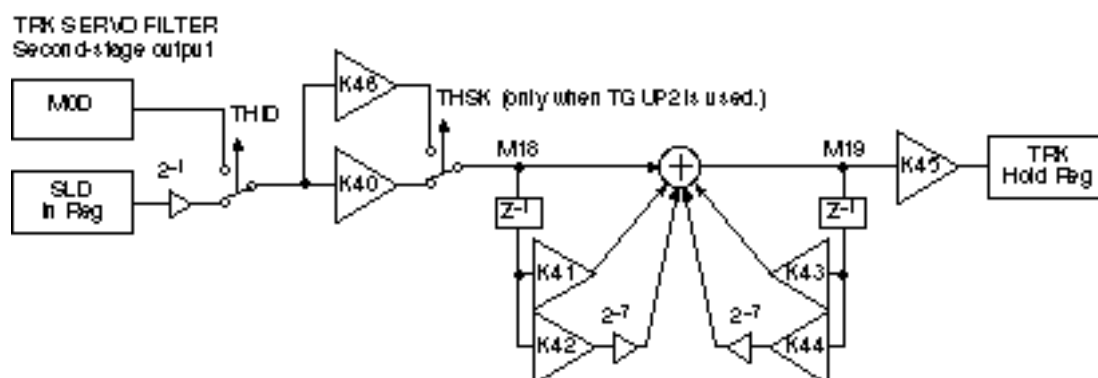## HPTZC/Auto Gain   fs = 88.2kHz

Anti Shock   fs = 88.2kHz

> **Note)** Set the MSB bit of the K34 coefficient to 0.
> The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG   fs = 88.2kHz

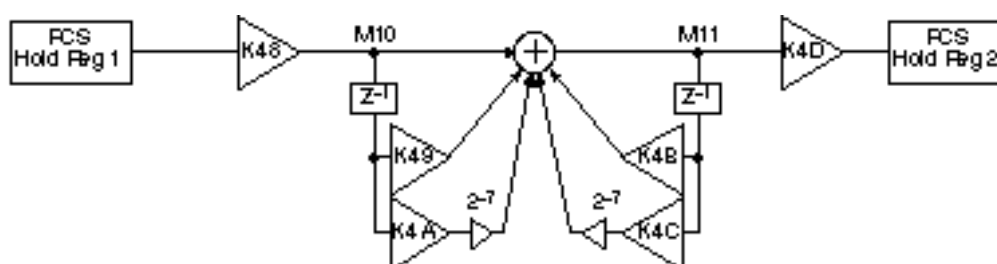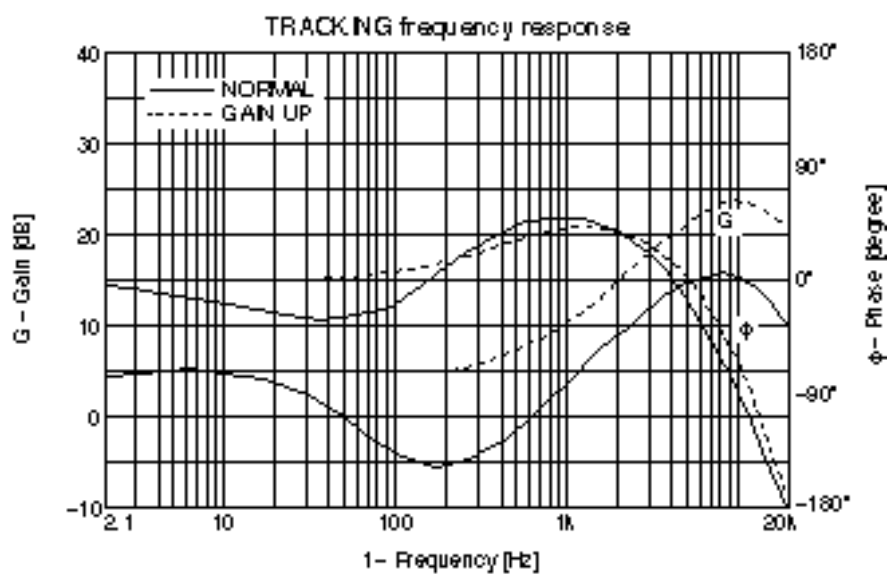**TRK Hold   fs = 345Hz**

> **Note)** Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold   fs = 345Hz

> **Note)** Set the MSB bit of the K4A and K4C coefficients to 0.

§ 5-21. TRACKING and FOCUS Frequency Response

When using the preset coefficients with the boost function off.
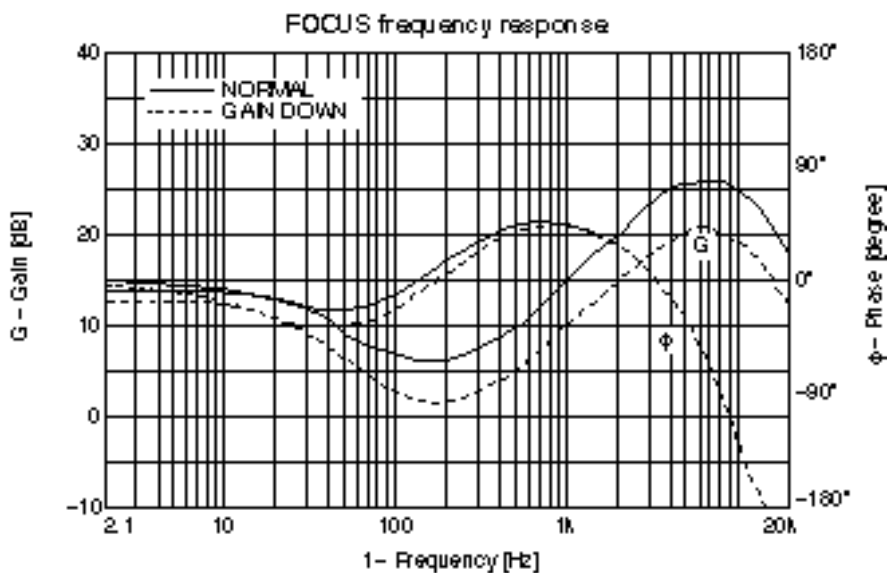
When using the preset coefficients with the boost function off.

[6] Application Circuit

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline   Unit: mm

80PIN QFP (PLASTIC)

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g
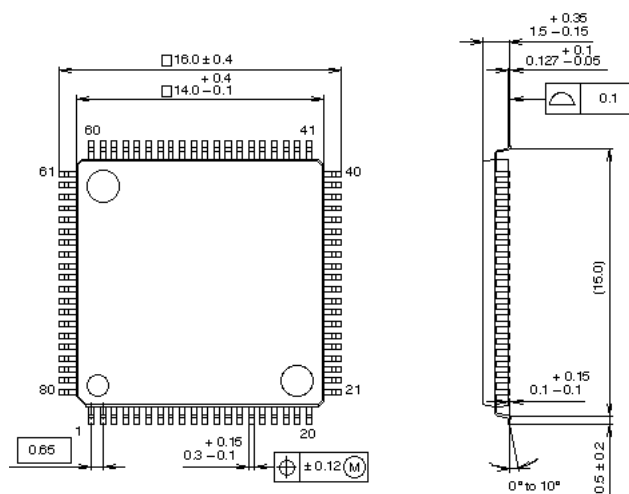
SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

80PIN QFP (PLASTIC)

DETAIL A

DETAIL B

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.6g
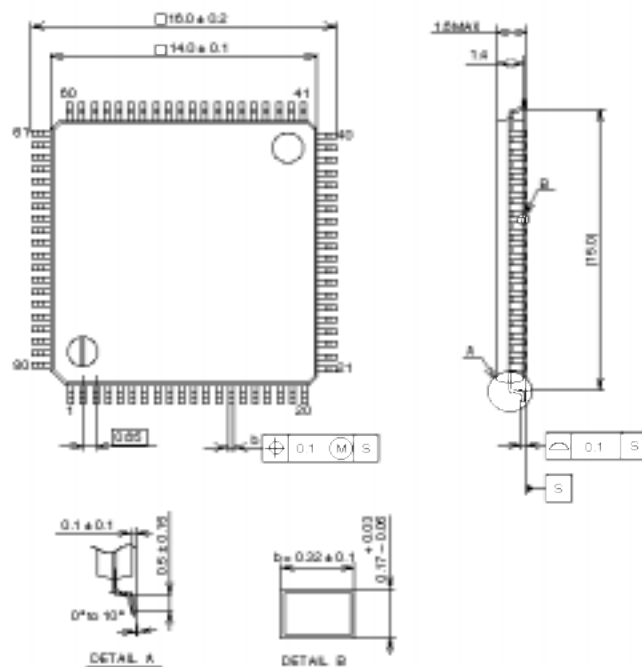
SONY CODE	QFP-80P-L02
EIAJ CODE	P-QFP80-16X14-0.65
JEDEC CODE	————

2 Megabit (256K x 8) Multi-Purpose Flash
SST39VF020

FEATURES:

- **Organized as 256K X 8**

- **Single 2.7-3.6V Read and Write Operations**

- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention

- **Low Power Consumption:**
  - Active Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)

- **Sector Erase Capability**
  - Uniform 4 KByte sectors

- **Fast Read Access Time:**
  - 70 and 90 ns

- **Latched Address and Data**

- **Fast Sector Erase and Byte Program:**
  - Sector Erase Time: 18 ms typical
  - Chip Erase Time: 70 ms typical
  - Byte Program time: 14 µs typical
  - Chip Rewrite Time: 4 seconds typical

- **Automatic Write Timing**
  - Internal V_{pp} Generation

- **End of Write Detection**
  - Toggle Bit
  - Data# Polling

- **CMOS I/O Compatibility**

- **JEDEC Standard**
  - EEPROM Pinouts and command set

- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8x14mm)

PRODUCT DESCRIPTION

The SST39VF020 is a 256K x 8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF020 device writes (Program or Erase) with a 2.7-3.6V power supply. The SST39VF020 device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance byte program, the SST39VF020 device provides a maximum byte-program time of 20 µsec. The entire memory can be erased and programmed byte by byte typically in 4 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, the SST39VF020 device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST39VF020 device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF020 device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST39VF020 device significantly improves performance and reliability, while lowering power con-

sumption. The SST39VF020 inherently uses less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST39VF020 device also improves flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of endurance cycles that have occurred. Therefore the system software or hardware does not have to be modified or derated as is necessary with alternative flash technologies, whose erase and program times increase with accumulated endurance cycles.

To meet high density, surface mount requirements, the SST39VF020 device is offered in 32-pin TSOP and 32-pin PLCC packages. A 600 mil, 32-pin PDIP is also available. See Figures 1 and 2 for pinouts.

Device Operation
Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while

keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39VF020 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Byte Program Operation

The SST39VF020 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 μs. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 14 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector by sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector Erase operation is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A17 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse , while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 8 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

Chip Erase Operation

The SST39VF020 device provides a Chip Erase operation, which allows the user to erase the entire memory array to the "1's" state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte software data protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 17 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

Write Operation Status Detection

The SST39VF020 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ₇)

When the SST39VF020 device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For sector or chip erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 15 for a flowchart.

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Preliminary Specifications

Toggle Bit (DQ$_6$)
During the internal Program or Erase operation, any consecutive attempts to read DQ$_6$ will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 15 for a flowchart.

Data Protection
The SST39VF020 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection
Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V$_{DD}$ Power Up/Down Detection: The Write operation is inhibited when V$_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)
The SST39VF020 provides the JEDEC approved software data protection scheme for all data alteration operation, i.e., program and erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires

the inclusion of six byte load sequence. The SST39VF020 device is shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T$_{RC}$.

Product Identification
The product identification mode identifies the device as the SST39VF020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39VF020 device. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the software ID entry and read timing diagram and Figure 16 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	0000H	BF H
Device Code	0001H	D6 H

336 PGM T1.0

Product Identification Mode Exit/Reset
In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 11 for timing waveform and Figure 16 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM OF **SST39VF020**
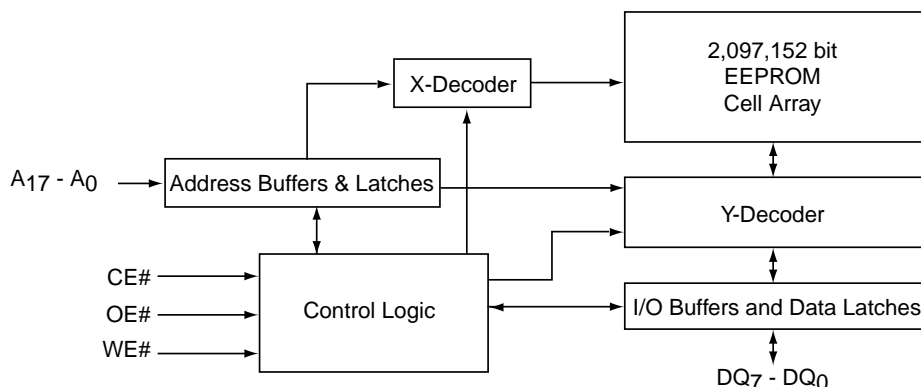
336 ILL B1.0

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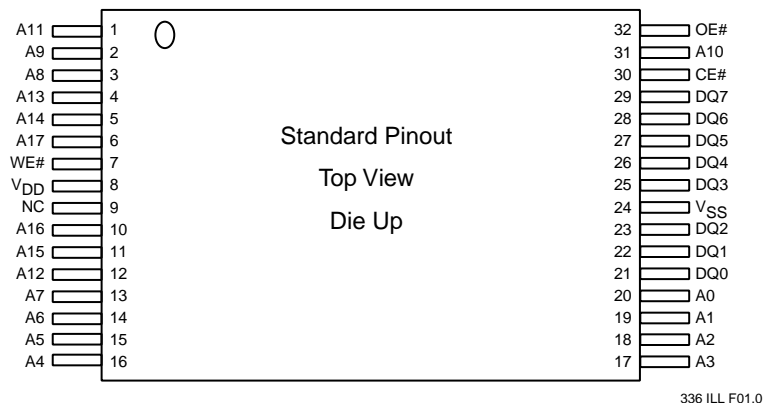
FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGE (8mm x 14mm)
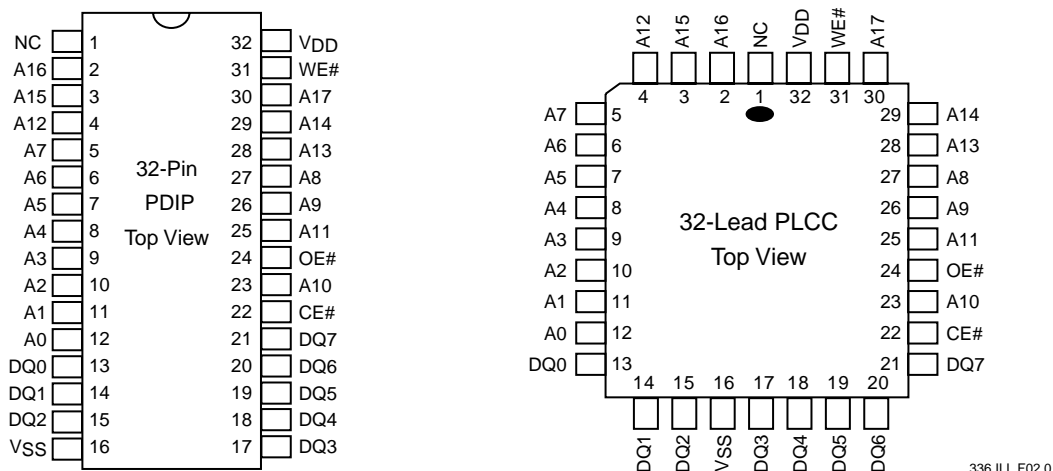
FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLASTIC DIPS AND 32-LEAD PLCCS

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2 Megabit Multi-Purpose Flash
SST39VF020

Preliminary Specifications

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{17}-A_0	Address Inputs	To provide memory addresses. During sector erase A_{17}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations.
V_{DD}	Power Supply	To provide 2.7-3.6V supply
Vss	Ground	
NC	No Connection	Unconnected pins

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A9	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXh for chip erase
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}	X
	X	X	V_{IH}	X	High Z/D_{OUT}	X
Product Identification Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer Code (BF) Device Code (D6)	A_{17} - A_1 = V_{IL}, A_0 = V_{IL} A_{17} - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

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TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA$_x$[2]	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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Notes:

[1] Address format A_{14}-A_0 (Hex), Addresses A_{15}, A_{16} and A_{17} are a "Don't Care" for the Command sequence.

[2] SA$_x$ for sector erase; uses A_{17}-A_{12} address lines

[3] BA = Program Byte address

[4] Both Software ID Exit operations are equivalent

Notes for Software ID Entry Command Sequence

1. With A_{17} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0, SST39VF020 Device Code = D6H, is read with A_0 = 1.

2. The device does not remain in Software Product ID Mode if powered down.

2 Megabit Multi-Purpose Flash
SST39VF020

Preliminary Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

D. C. Voltage on Any Pin to Ground Potential .... -0.5V to V_{DD}+ 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential .... -1.0V to V_{DD}+ 1.0V

Voltage on A_9 Pin to Ground Potential .... -0.5V to 13.2V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Through Hole Lead Soldering Temperature (10 Seconds) .... 300°C

Surface Mount Lead Soldering Temperature (3 Seconds) .... 240°C

Output Short Circuit Current[1] .... 50 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0 °C to +70 °C	2.7 - 3.6V
Industrial	-40 °C to +85 °C	2.7 - 3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time .... 10 ns

Output Load .... C_L = 100 pF

See Figures 12 and 13

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	

I_{DD}	Power Supply Current
	  Read
			12	mA	CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open,
					Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min.,
					  V_{DD}=V_{DD} Max

	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{DD} =V_{DD} Max.
I_{SB}	Standby V_{DD} Current		15	µA	CE#=V_{IHC}, V_{DD} = V_{DD} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min.
V_{IH}	Input High Voltage	2.0		V	V_{DD} = V_{DD} Max.
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100µA, V_{DD} = V_{DD} Min.
V_{H}	Supervoltage for A_9 pin	11.4	12.6	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_{H}	Supervoltage Current for A_9 pin		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

336 PGM T7.0

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Preliminary Specifications

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V$_{DD}$ = 2.7-3.6V

| Symbol | Parameter | SST39VF020-70 | | SST39VF020-90 | | |
		Min	Max	Min	Max	Units
T$_{RC}$	Read Cycle time	70		90		ns
T$_{CE}$	Chip Enable Access Time		70		90	ns
T$_{AA}$	Address Access Time		70		90	ns
T$_{OE}$	Output Enable Access Time		35		45	ns
T$_{CLZ}$[1]	CE# Low to Active Output	0		0		ns
T$_{OLZ}$[1]	OE# Low to Active Output	0		0		ns
T$_{CHZ}$[1]	CE# High to High-Z Output		15		20	ns
T$_{OHZ}$[1]	OE# High to High-Z Output		15		20	ns
T$_{OH}$[1]	Output Hold from Address Change	0		0		ns

336 PGM T9.1

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T$_{BP}$	Byte Program time		20	μs
T$_{AS}$	Address Setup Time	0		ns
T$_{AH}$	Address Hold Time	30		ns
T$_{CS}$	WE# and CE# Setup Time	0		ns
T$_{CH}$	WE# and CE# Hold Time	0		ns
T$_{OES}$	OE# High Setup Time	0		ns
T$_{OEH}$	OE# High Hold Time	10		ns
T$_{CP}$	CE# Pulse Width	40		ns
T$_{WP}$	WE# Pulse Width	40		ns
T$_{WPH}$	WE# Pulse Width High	30		ns
T$_{CPH}$	CE# Pulse Width High	30		ns
T$_{DS}$	Data Setup Time	40		ns
T$_{DH}$	Data Hold Time	0		ns
T$_{IDA}$	Software ID Access and Exit Time		150	ns
T$_{SE}$	Sector Erase		25	ms
T$_{SCE}$	Chip Erase		100	ms

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Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
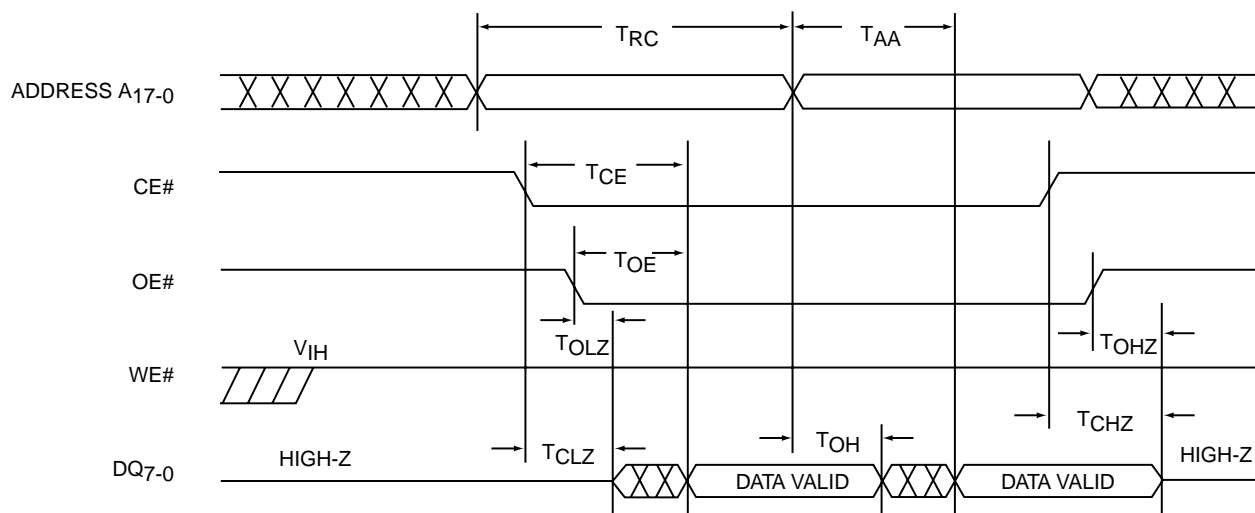
336 ILL F03.0

FIGURE 3: READ CYCLE TIMING DIAGRAM
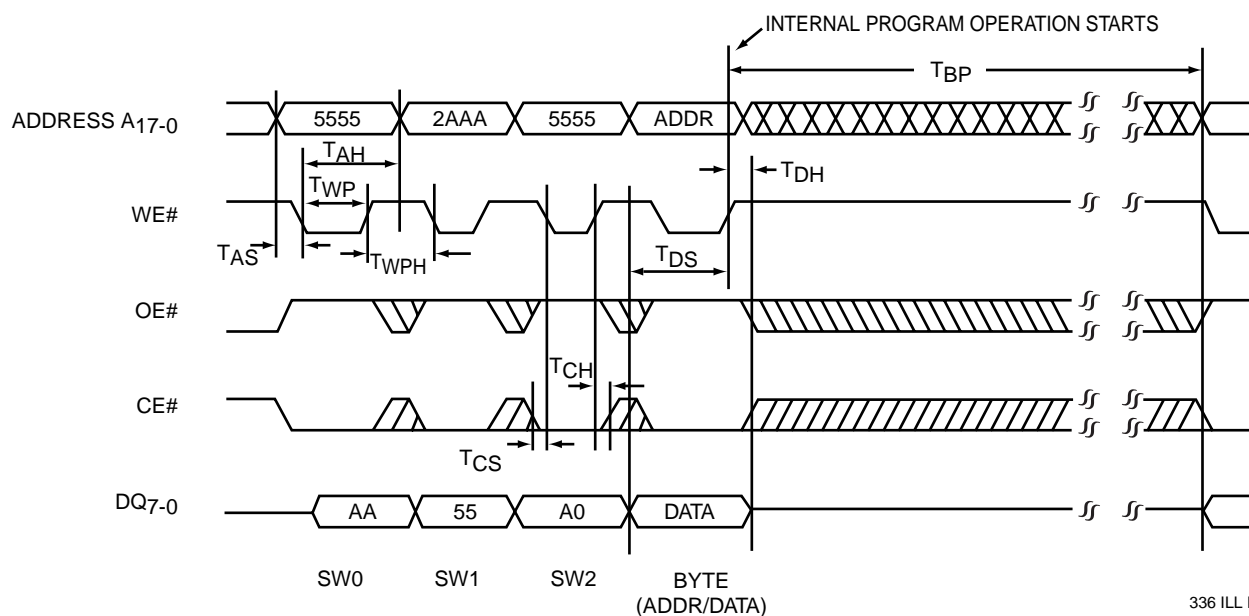
336 ILL F04.0

FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM
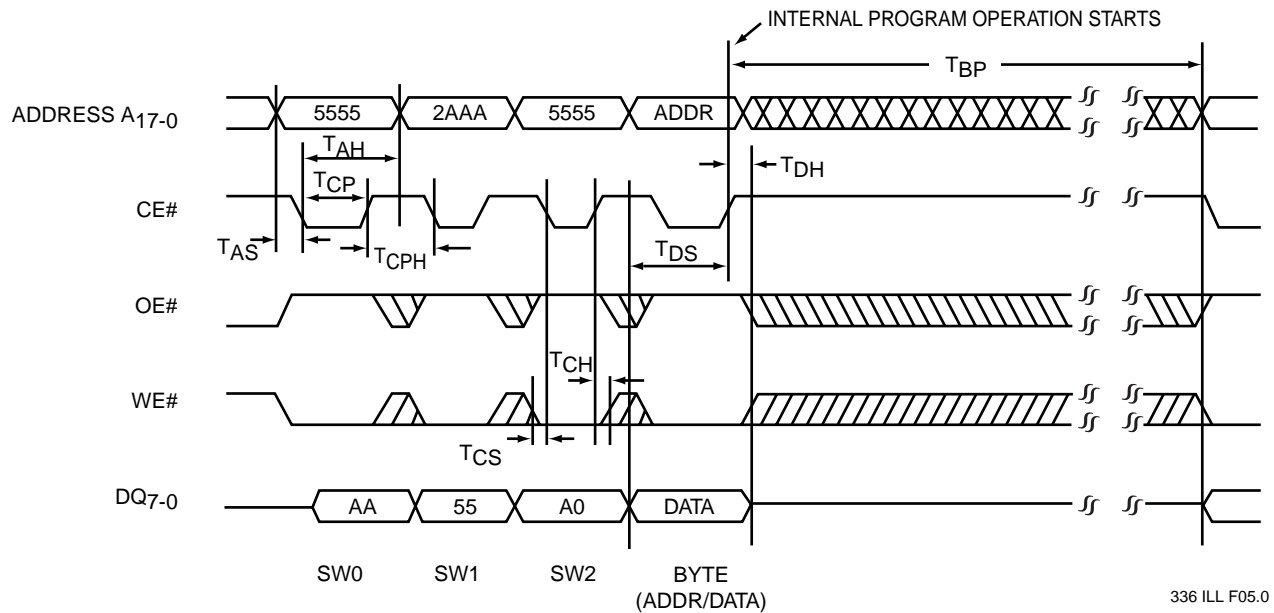
FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM
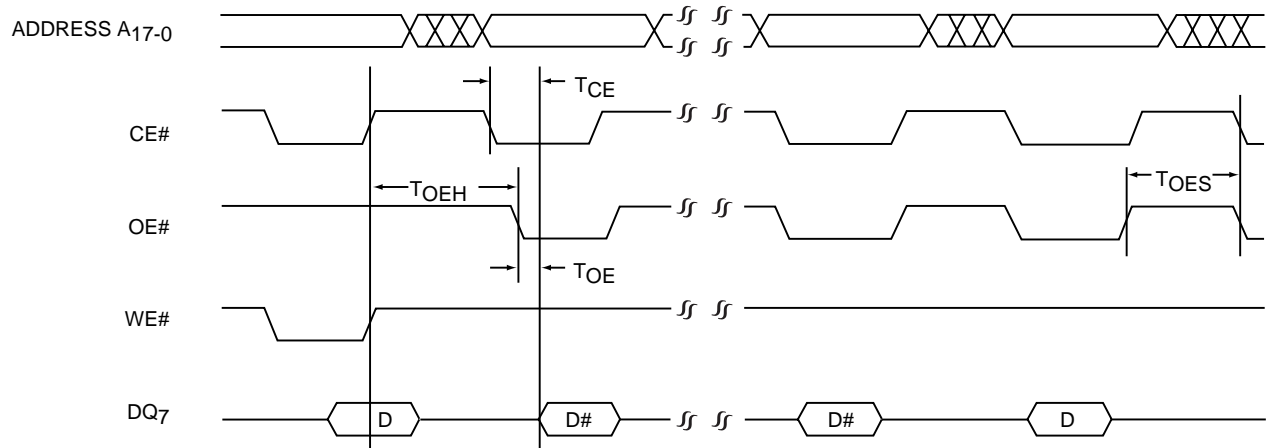
336 ILL F05.0

FIGURE 6: DATA# POLLING TIMING DIAGRAM

336 ILL F06.0

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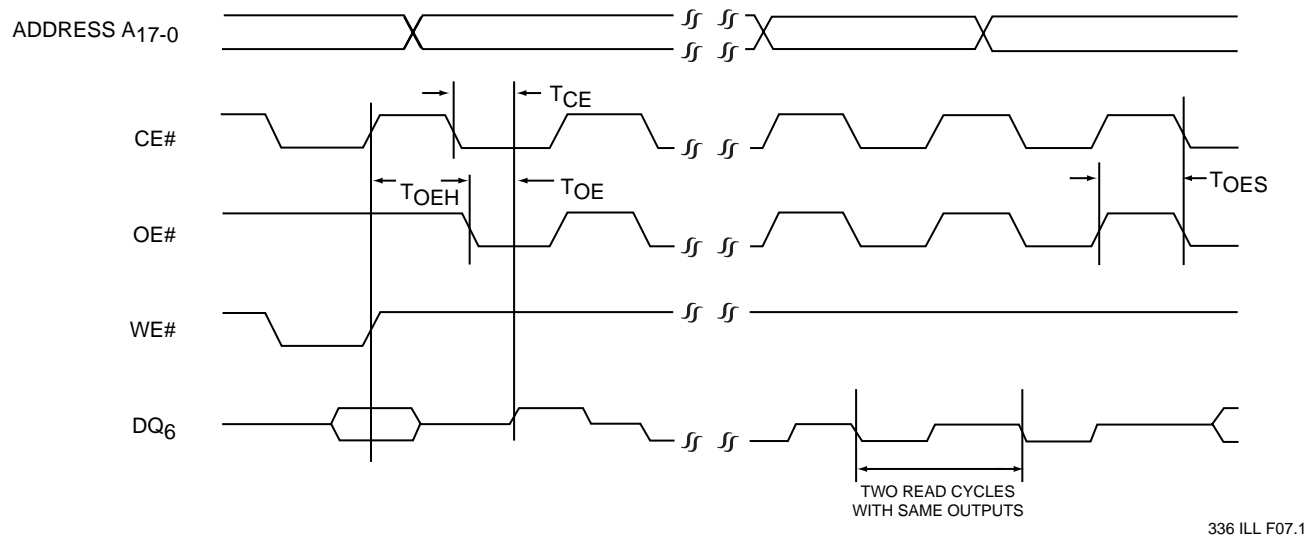
FIGURE 7: TOGGLE BIT TIMING DIAGRAM
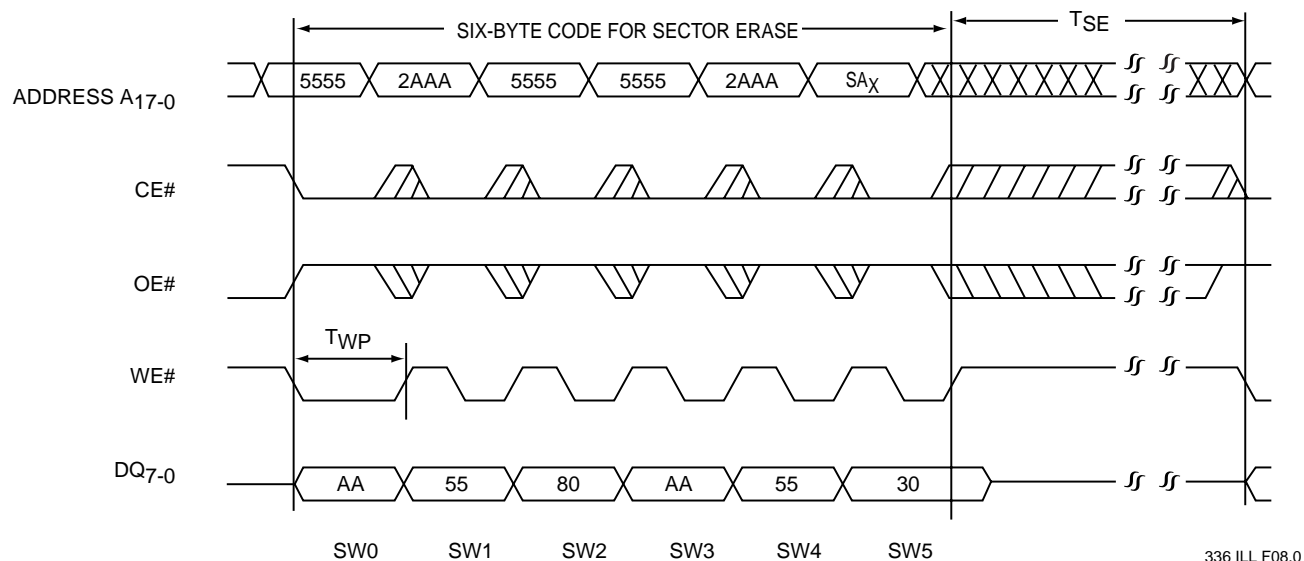
Note: The device also supports CE# controlled sector erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address

FIGURE 8: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM

SIX-BYTE CODE FOR CHIP ERASE

T_{SCE}

ADDRESS A_{17-0}

| 5555 | 2AAA | 5555 | 5555 | 2AAA | 5555 |

CE#

OE#

T_{WP}

WE#

DQ$_{7-0}$

| AA | 55 | 80 | AA | 55 | 10 |

SW0   SW1   SW2   SW3   SW4   SW5

336 ILL F17.0
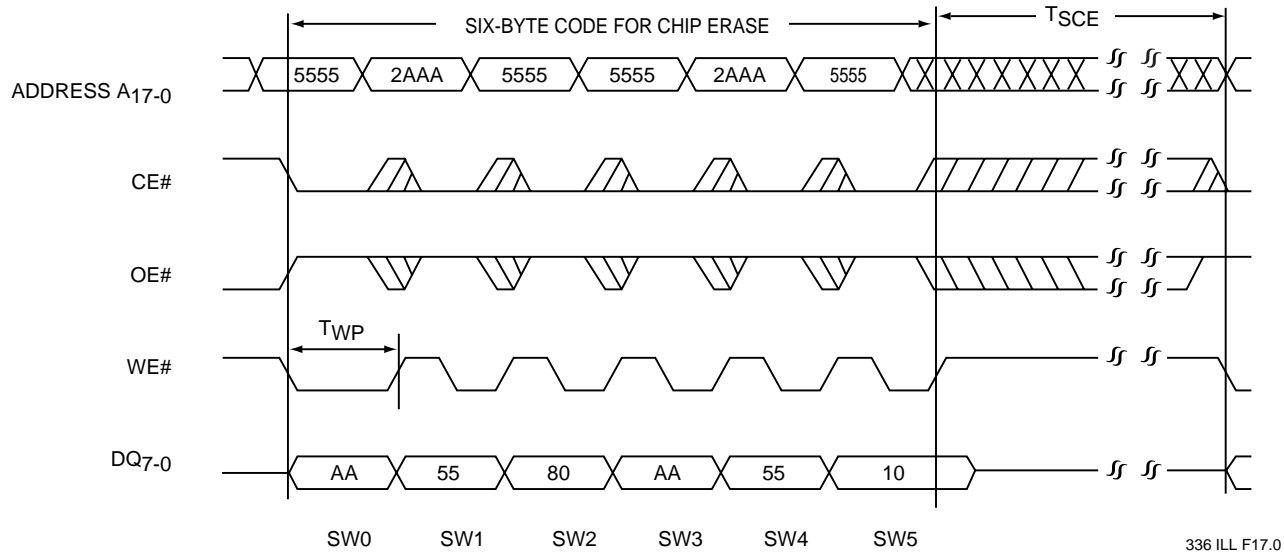
Note: The device also supports CE# controlled chip erase operation. The WE# and CE# signals are
interchangeable as long as minimum timings are met. (See Table 10)

FIGURE 9: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM

Three-byte sequence for
Software ID Entry

ADDRESS A_{14-0}

| 5555 | 2AAA | 5555 | | 0000 | 0001 |

CE#

OE#

T_{WP}

T_{IDA}

WE#

T_{WPH}

T_{AA}

DQ$_{7-0}$

| AA | 55 | 90 | | BF | D6 |

SW0   SW1   SW2

336 ILL F09.1
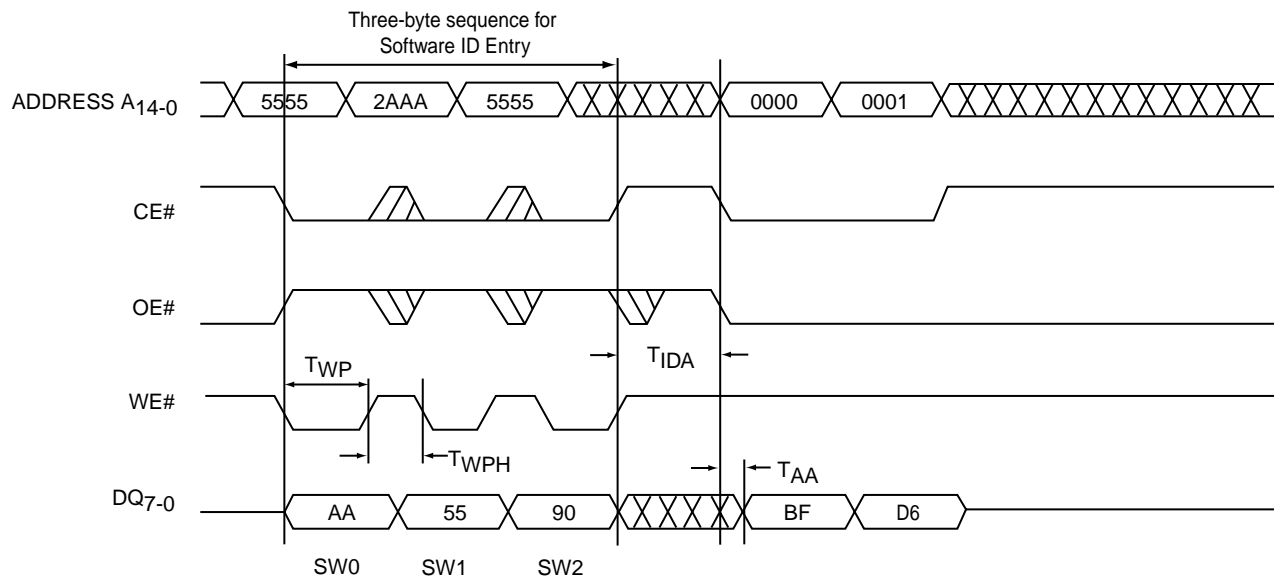
FIGURE 10: SOFTWARE ID ENTRY AND READ

THREE-BYTE SEQUENCE FOR
SOFTWARE ID EXIT AND RESET

ADDRESS A_{14-0}

5555   2AAA   5555

DQ_{7-0}

AA   55   F0

CE#

T_{IDA}

OE#

T_{WP}

WE#

T_{WHP}

SW0   SW1   SW2
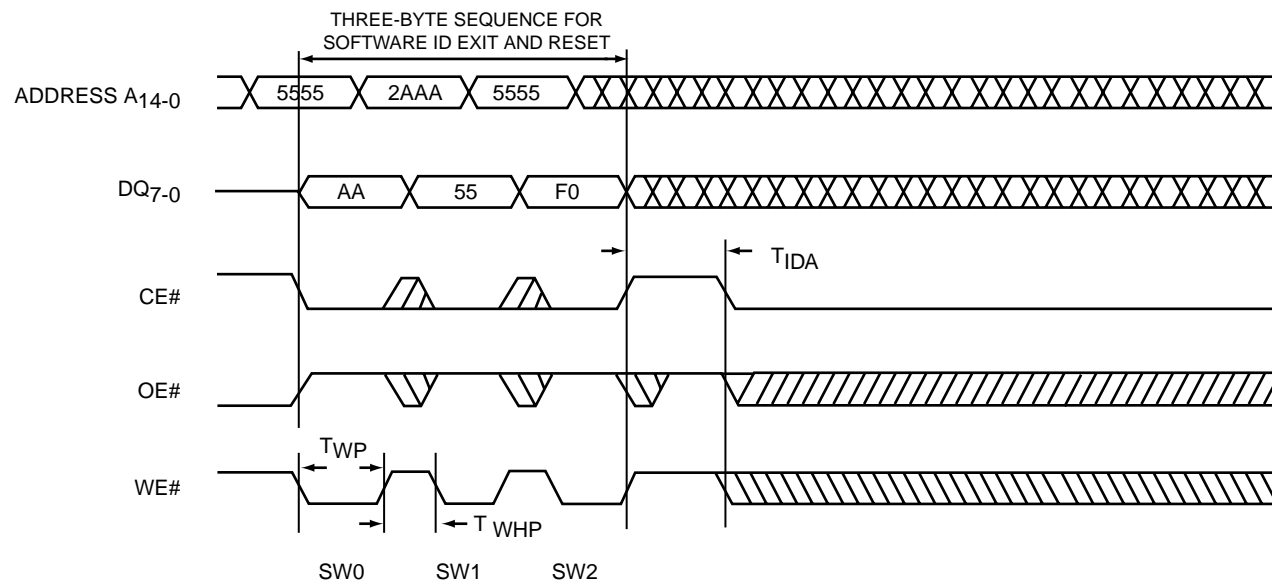
336 ILL F10.0

FIGURE 11: SOFTWARE ID EXIT AND RESET

Preliminary Specifications
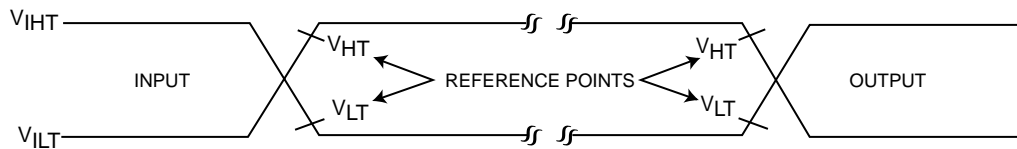
336 ILL F11.1

AC test inputs are driven at V_{IHT} (2.4 V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0".
Measurement reference points for inputs and outputs are at V_{HT} (2.0 V) and V_{LT} (0.8 V)
Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT}–V_{HIGH} Test
V_{LT}–V_{LOW} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 12: AC INPUT/OUTPUT REFERENCE WAVEFORMS

TEST LOAD EXAMPLE
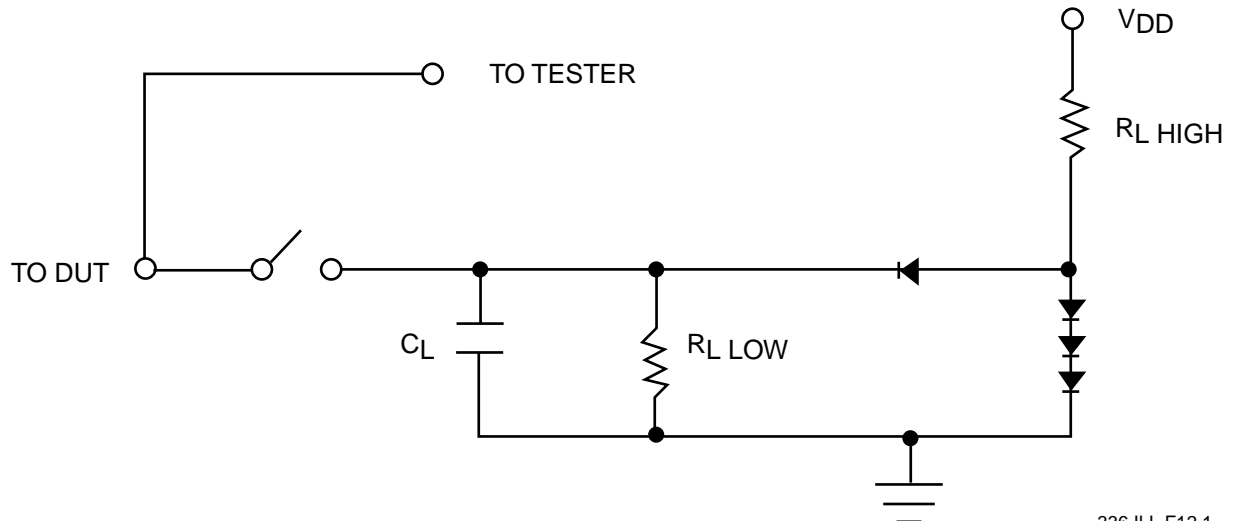
336 ILL F12.1

FIGURE 13: A TEST LOAD EXAMPLE

```
                           ╭──────────╮
                           │  Start   │
                           ╰──────────╯
                                │
                                ▼
                    ┌───────────────────────┐
                    │   Write data: AA      │
                    │   Address: 5555       │
                    └───────────────────────┘
                                │
                                ▼
                    ┌───────────────────────┐
                    │   Write data: 55      │
                    │   Address: 2AAA       │
                    └───────────────────────┘
                                │
                                ▼
                    ┌───────────────────────┐
                    │   Write data: A0      │
                    │   Address: 5555       │
                    └───────────────────────┘
                                │
                                ▼
                    ┌───────────────────────┐
                    │   Load Byte           │
                    │   Address/Byte        │
                    │   Data                │
                    └───────────────────────┘
                                │
                                ▼
                    ┌───────────────────────┐
                    │   Wait for end of     │
                    │   Program (TBP,       │
                    │   Data# Polling       │
                    │   bit, or Toggle bit  │
                    │   operation)          │
                    └───────────────────────┘
                                │
                                ▼
                           ╭──────────╮
                           │ Program  │
                           │Completed │
                           ╰──────────╯
```
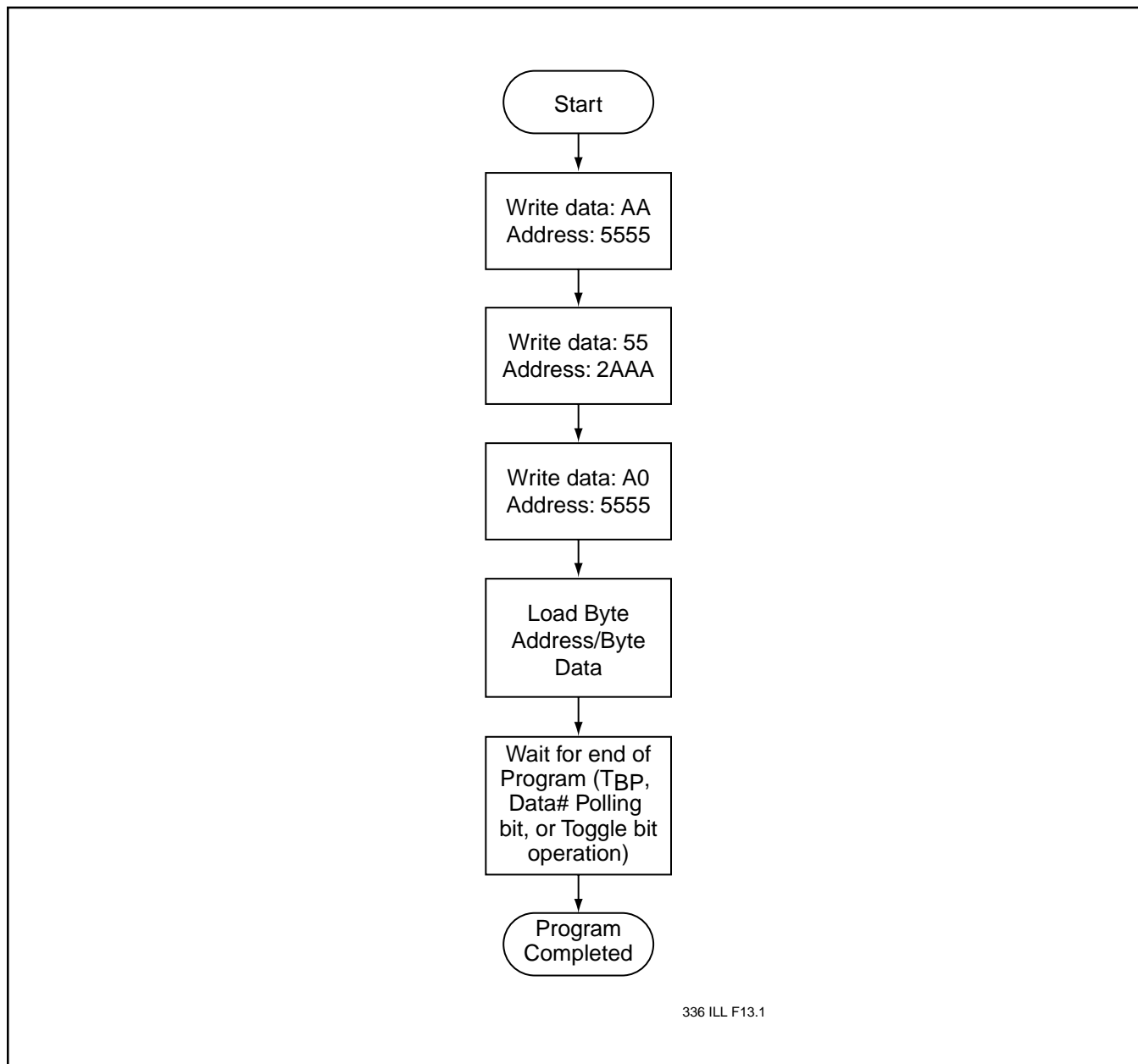
336 ILL F13.1

FIGURE 14: BYTE PROGRAM ALGORITHM

Internal Timer

```
┌──────────────┐
│    Byte      │
│Program/Erase │
│  Initiated   │
└──────────────┘
       │
       ▼
┌──────────────┐
│ Wait T_BP,   │
│ T_SCE, or T_SE│
└──────────────┘
       │
       ▼
╭──────────────╮
│Program/Erase │
│  Completed   │
╰──────────────╯
```

Toggle Bit

```
┌──────────────┐
│    Byte      │
│Program/Erase │
│  Initiated   │
└──────────────┘
       │
       ▼
┌──────────────┐
│  Read byte   │
└──────────────┘
       │
       ▼
┌──────────────┐
│  Read same   │
│    byte      │
└──────────────┘
       │
       ▼
    ╱─────╲
   ╱ Does  ╲   No
  ╱  DQ6    ╲──────
  ╲  match? ╱
   ╲───────╱
       │ Yes
       ▼
╭──────────────╮
│Program/Erase │
│  Completed   │
╰──────────────╯
```

Data# Polling

```
┌──────────────┐
│    Byte      │
│Program/Erase │
│  Initiated   │
└──────────────┘
       │
       ▼
┌──────────────┐
│  Read DQ7    │
└──────────────┘
       │
       ▼
    ╱─────╲
No ╱ Is DQ7 ╲
──╱ = true   ╲
  ╲  data?   ╱
   ╲───────╱
       │ Yes
       ▼
╭──────────────╮
│Program/Erase │
│  Completed   │
╰──────────────╯
```
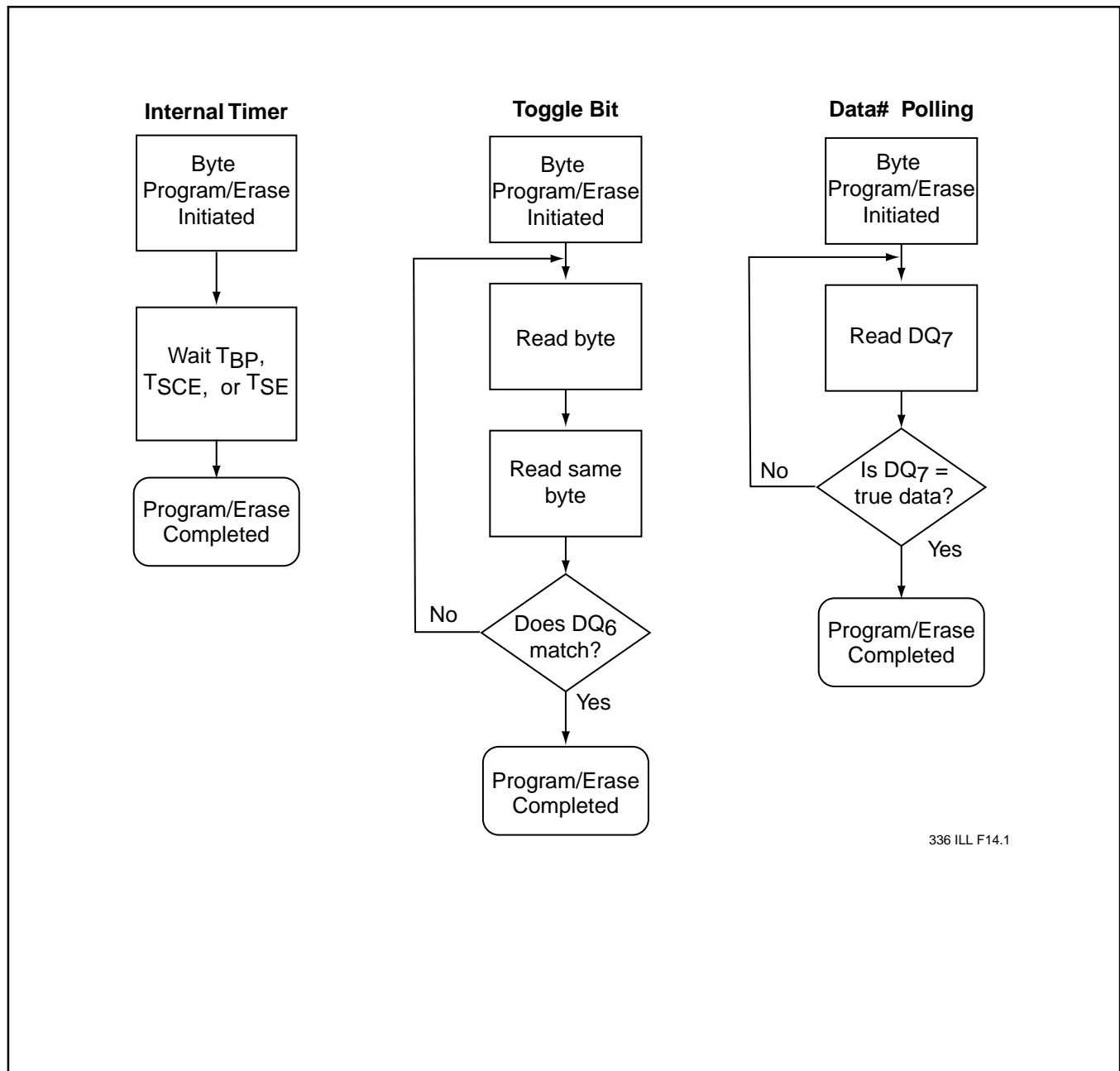
336 ILL F14.1

FIGURE 15: WAIT OPTIONS

Software Product ID Entry Command Sequence

```
┌─────────────────┐
│ Write data: AA  │
│ Address: 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│ Write data: 55  │
│ Address: 2AAA   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│ Write data: 90  │
│ Address: 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│                 │
│   Wait T_IDA    │
│                 │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│ Read Software ID│
└─────────────────┘
```
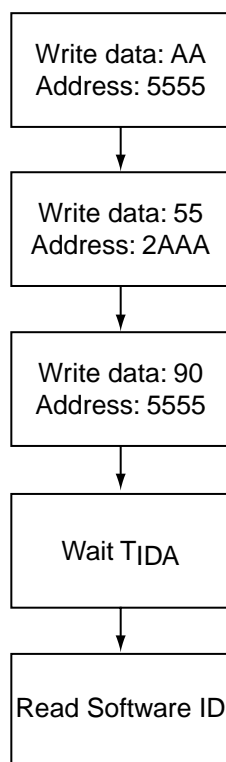
Software Product ID Exit & Reset Command Sequence

```
┌─────────────────┐       ┌─────────────────┐
│ Write data: AA  │       │ Write data: F0  │
│ Address: 5555   │       │ Address: XX     │
└─────────────────┘       └─────────────────┘
         │                         │
         ▼                         ▼
┌─────────────────┐       ┌─────────────────┐
│ Write data: 55  │       │                 │
│ Address: 2AAA   │       │   Wait T_IDA    │
└─────────────────┘       │                 │
         │                └─────────────────┘
         ▼                         │
┌─────────────────┐                ▼
│ Write data: F0  │       ┌─────────────────┐
│ Address: 5555   │       │ Return to normal│
└─────────────────┘       │   operation     │
         │                └─────────────────┘
         ▼
┌─────────────────┐
│                 │
│   Wait T_IDA    │
│                 │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│ Return to normal│
│   operation     │
└─────────────────┘
```
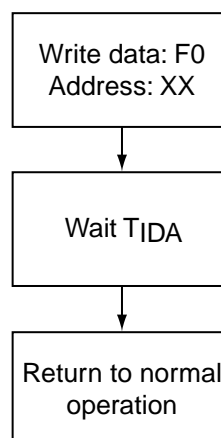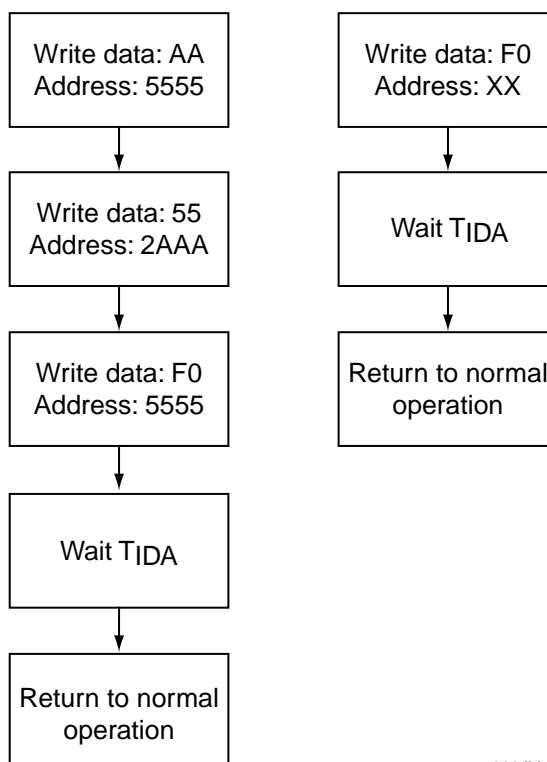
336 ILL F15.0

FIGURE 16: SOFTWARE PRODUCT COMMAND FLOWCHARTS

Preliminary Specifications

**Chip Erase
Command Sequence**

**Sector Erase
Command Sequence**

Write data: AA Address: 5555	Write data: AA Address: 5555
Write data: 55 Address: 2AAA	Write data: 55 Address: 2AAA
Write data: 80 Address: 5555	Write data: 80 Address: 5555
Write data: AA Address: 5555	Write data: AA Address: 5555
Write data: 55 Address: 2AAA	Write data: 55 Address: 2AAA
Write data: 10 Address: 5555	Write data: 30 Address: SA_X
Wait T_{SCE}	Wait T_{SE}
Chip erased to FFH	Sector erased to FFH

336 ILL F16.1

FIGURE 17: ERASE COMMAND SEQUENCE

Device	Speed	Suffix1	Suffix2
SST39VF020	- XXX	- XX	- XX

Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
W = TSOP (die up) (8mm x 14mm)
U = Unencapsulated die

Temperature Range
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
4 = 10,000 cycles

Read Access Speed
70 = 70 ns, 90 = 90 ns
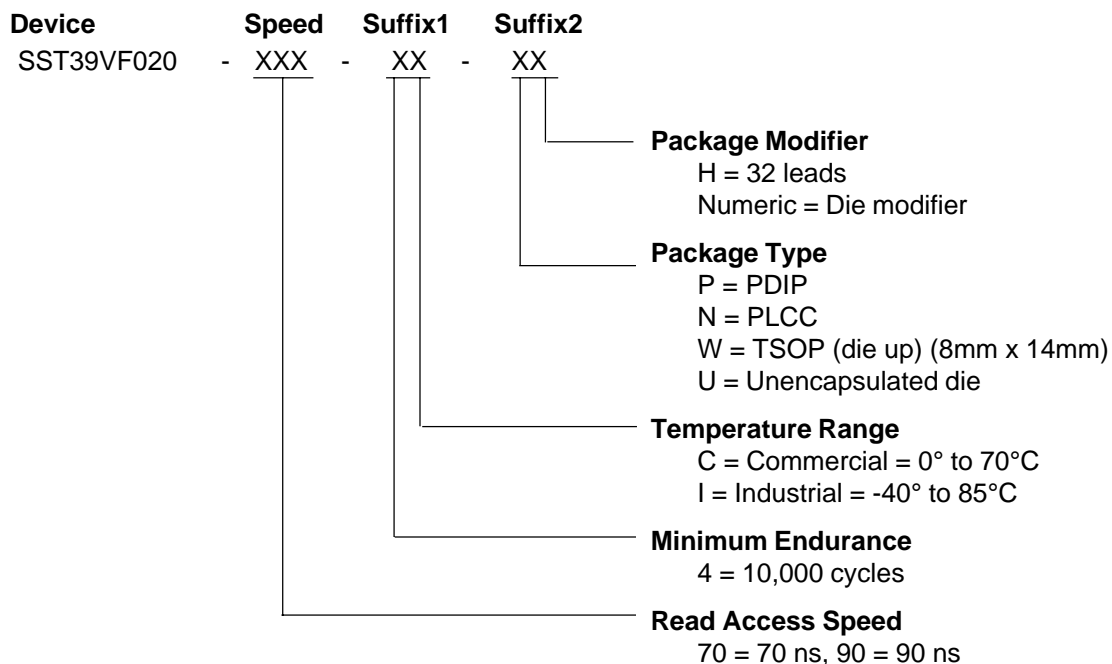
SST39VF020 Valid combinations

SST39VF020-70-4C-WH	SST39VF020-70-4C-NH	SST39VF020-70-4C-PH
SST39VF020-90-4C-WH	SST39VF020-90-4C-NH	SST39VF020-90-4C-PH
SST39VF020-90-4C-U1		

SST39VF020-70-4I-WH	SST39VF020-70-4I-NH
SST39VF020-90-4I-WH	SST39VF020-90-4I-NH

Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

PACKAGING DIAGRAMS

pin 1 index

1

32

Optional Ejector Pin
Indentation Shown for
Conventional Mold Only

C̲L̲

.065
.075

1.645
1.655

Base Plane
Seating Plane

.170
.200

.015
.050

.070
.080

.045
.065

.016
.022

.100 BSC

.120
.150

.600
.625

.530
.550

7°
4 PLCS.

.008
.012

0°
15°

.600 BSC

Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
         2. All linear dimensions are in inches (min/max).
         3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32.pdipPH-ILL.0

32-Lᴇᴀᴅ Pʟᴀsᴛɪᴄ Dᴜᴀʟ-ɪɴ-Lɪɴᴇ Pᴀᴄᴋᴀɢᴇ (PDIP)

SST Pᴀᴄᴋᴀɢᴇ Cᴏᴅᴇ: PH

TOP VIEW   SIDE VIEW   BOTTOM VIEW

.485
.495

.447
.453

.045 Dia. x .000/.010
Deep Polished
(Optional)

.042
.048

.020 R.
MAX.

2 1 32

.042
.048

.585
.595

.547
.553

.026
.032

.050
BSC.

.050
BSC.

.106
.112

.023
.029 x 30°

.030
.040 R.

.013
.021

.400
BSC

.490
.530

.015 Min.

.075
.095

.125
.140

.076/.125 Dia.
Ejector Pin

.020 High x .002
Deep Characters

.026
.032

Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
         2. All linear dimensions are in inches (min/max).
         3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32.PLCC.NH-ILL.0

32-Lᴇᴀᴅ Pʟᴀsᴛɪᴄ Lᴇᴀᴅ Cʜɪᴘ Cᴀʀʀɪᴇʀ (PLCC)

SST Pᴀᴄᴋᴀɢᴇ Cᴏᴅᴇ: NH

1.10 / 0.90

PIN # 1 IDENT. DIA. 1.00

8.10 / 7.90

12.50 / 12.30

1.05 / 0.95

.50 BSC

.270 / .170

0.15 / 0.05

0.70 / 0.50

14.20 / 13.80

Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
         2. All linear dimensions are in metric (min/max).
         3. Coplanarity: 0.1 (±.05) mm.

32.TSOP-WH-ILL.0

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: WH

(Waslin Group . since 1992)
Website: http://www.waslin.cn, http://www.metatech.com.tw

HongKong
Tel: 852-24212379   Fax: 852-24212479
Address: Unit 3503, Metroplaza Tower II, 223 Hing Fong Rd., Kwai
                    Fong, Hong Kong.
Email: service@meta.com.hk

Beijing
Tel: 86-10-68582188   Fax: 86-10-68583188
Address: Rm. 210, China Hall of Science & Technology, No. 3 FuXing
                    Road, Beijing, China 100038

Shanghai
Tel: 86-21-64857530   Fax:86-21-64852237
Address: No. 507, New Cao He Jing Tower, No. 509 Cao Bao Road,
                    Shanghai, China 200233

Chengdu
Tel: 86-28-5577415   Fax:86-28-5577415
Address: Rm. 1405, 14/F Dong Fu Da Xia, Yu Lin Bei Jie, Chengdu,
                    Sichuan, China 610041

Fuzhou
Tel: 86-591-3781033   Fax: 86-591-3781033
Address: Room 1512, Block 2, Xi Hong Xiao Qiu, Gu Lou Qiu, FuZhou,
                    China

Shenzhen
Tel: 86-755-3219726   Fax: 86-755-3219736
Address: Room 1105, 11/F, Bei Fang Da Xia, Shen Nan Zhong Lu,
                    Shenzhen, China.

Customer Service Center
Tel:86-756-8117078   Fax:86-756-8117078
Address: 20 Qiao Guang Rd., Kuns Bei , Zhuhai, China 519020

凌陽科技
SUNPLUS

SPCA717A

Digital Video Encoder for Video CD

Preliminary

NOV. 11, 2002

Version 0.1

Table of Contents

NOV. 11, 2002
Preliminary Version: 0.1

DIGITAL VIDEO ENCODER FOR VIDEO CD

1.GENERAL DESCRIPTION

The SPCA717A is designed specifically for VideoCD, video games and other digital video systems, which require the conversion of digital YCrCb (MPEG) data to analog NTSC/PAL video. The device supports a glue-less interface to most popular MPEG decoders. The SPCA717A supports worldwide video standards, including NTSC (N America, Japan) PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay), and PAL-Nc (Argentina). Furthermore, the SPCA717A operates with a single 2x clock and can be powered with a single 3.3V supply. The composite analog video signal is output simultaneously onto two outputs. Therefore, it allows one output to provide base-band composite video while the other drives a RF modulator. As a slave, the SPCA717A automatically detects the input data formats (PAL/NTSC, CCIR601) and switches internally to provide the proper format on the outputs. This feature, along with the on-board voltage reference and single clock interface, makes the SPCA717A extremely simple to use. In addition, use of 2x over-sampling on-chip simplifies external filter design resulting in reduced overall system cost.
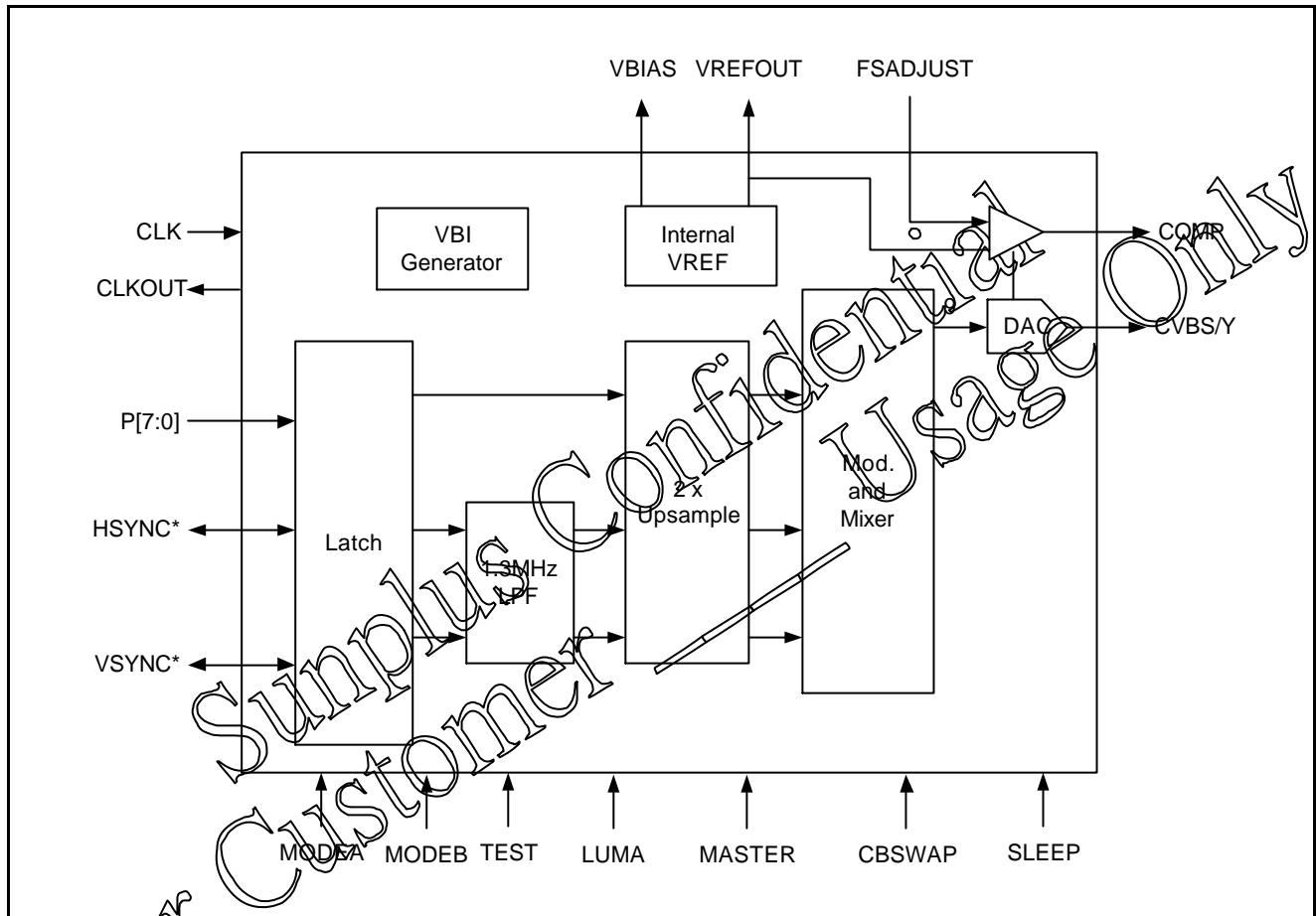
2.FEATURES

- 8-bit 4:2:2 YCrCb inputs for glue-less interface to MPEG decoders
- NTSC/PAL/PAL-M/PAL-Nc composite video outputs
- 3.3 V supply voltage
- ITU-R BT601/656 operation
- 2x over-sampling simplifies external filtering
- One 9-bit DAC
- Master or slave video timing
- Interlaced or non-interlaced operation
- Automatic mode detection/switching in slave mode
- 27MHz crystal oscillator input
- Power-down mode of chip
- On-board voltage reference
- 32-pin LQFP package

3.APPLICATIONS

- VideoCD
- Karaoke/video games
- Digital Video Disk (DVD)
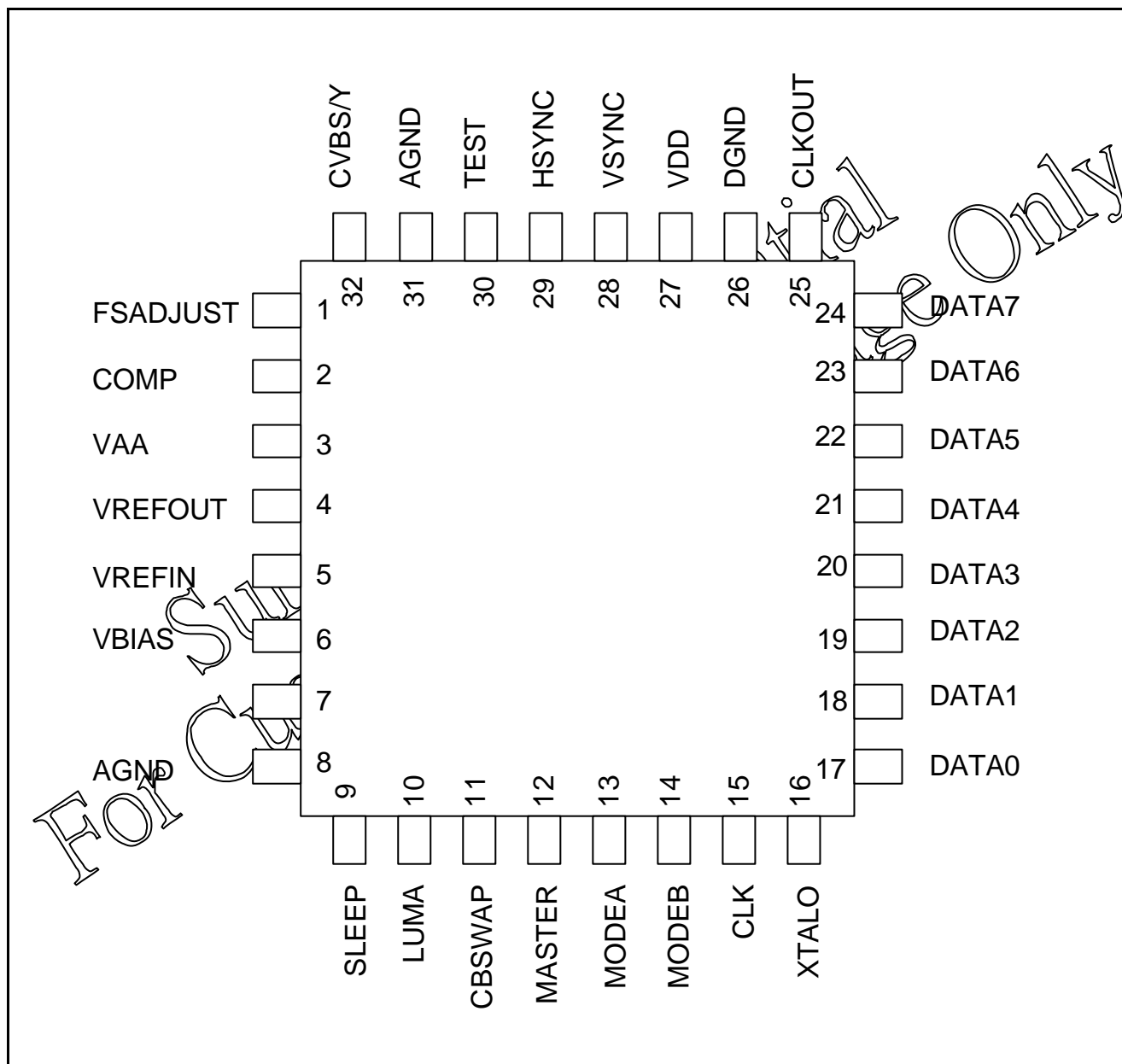- Digital VCR
- Digital set top box

4.BLOCK DIAGRAM

5. SIGNAL DESCRIPTIONS

5.1. PIN Description

Mnemonic	PIN No.	Type	Description
DATA[7:0]	17 - 24	I	YCrCb pixel inputs. They are latched on the rising edge of CLK. YCrCb input data conform to CCIR 601.
CLKOUT	25	O	Pixel clock output
VSYNC	28	I/O	Vertical sync input/output. VSYNC is latched/output following the rising edge of CLK.
HSYNC	29	I/O	Horizontal sync input/output. HSYNC is latched/output following the rising edge of CLK.
MASTER	12	I	Master/slave mode selection. A logical high for Master mode operation. A logical 0 for slave mode operation
CBSWAP	11	I	Cr and Cb pixel sequence configuration pin. A logic high swap the Cr and Cb sequence.
LUMA	10	I	Luma output selection pin. A logic high selects Y output. A logic low selects composite video output.
SLEEP	9	I	Power save mode. A logic high on this pin puts the chip into power-down mode. This pin is equal to reset pin. An external logic high pulse should input to the pin when power on.
MODEA	13	I	Mode configuration pin.
MODEB	14	I	Mode configuration pin.
CLK	15	I	27MHz crystal oscillator input. A crystal with 27MHz clock frequency can be connected between this pin and XTALO.
XTALO	16	O	Crystal oscillator output.
TEST	30	I	Test pin. These pins must be connected to DGND.
VREFIN	5	I	Voltage reference input. An external voltage reference must supply typical 1.235V to this pin. A 0.1µF ceramic capacitor must be used to de-couple this input to GND. The decoupling capacitor must be as closed as possible to minimize the length of the load. This pin may be connected directly to VREFOUT.
VREFONT	4	O	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive VREFIN pin directly.
FSADJ	1	-	Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground.
COMP	2	-	Compensation pin. A 0.1µF ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
VBIAS	6	-	DAC bias voltage. Potential normally 0.7V less than COMP.
VDD	27	-	Digital power pin
DGND	26	-	Digital ground pin
CVBSY	32	O	Composite/Luminance output. This is a high-impedance current source output. The output format can be selected by the PAL pin. The CVBSY can drive a 37.5 Ω load.
NO	7		-
VAA	3	-	Analog power pin
AGND	31,8	-	Analog ground pin

5.2. PIN Map

6. FUNCTIONAL DESCRIPTIONS

6.1. Mode Selection

Master mode is selected when MASTER = 1; slave mode is selected when MASTER = 0. Two pins, MODEA, MODEB, drive three different configuration registers. The most common operating modes can be selected with these pins while in master mode. In slave mode, the common operating modes are automatically determined from the timing of the incoming HSYNC* and VSYNC* signals.

Note:

The term "common operating mode" refers to North American NTSC and Western European PAL **Table 1** illustrates the multi-functionality of the mode pins during master and slave mode. To access the more exotic video formats, slave mode is preferred since the necessary registers are always accessible. If master mode is needed, the less common modes can still be programmed by first registering the modes as a slave, and then switching to a master. During power-up, the MODEA and MODEB pins configure the master registers (i.e. EFIELD, PAL625, are written. Also, during power-up, the slave registers are reset to zero, i.e., YCSWAP.

Table 1. Mode Selection

PIN Description		
The MASTER pin	**MODEA**	**MODEB**
0	YCSWAP	PALSA
1	EFIELD	PAL625

Table 2. Configuration Register Settings

Mode Register Name	Set to 0	Set to 1	Comments
EFIELD	The VSYNC* pin will output normal vertical synchronization signal.	The VSYNC pin will output field signal. Low at VSYNC pin for even field, high for odd field	This is only used at master mode.
PAL625	525-line operation will be select	The 625-line operation will be select	This is only used at master mode
YCSWAP	Do not swap Y and Cr/Cb	Swap Y and Cr/Cb sequence	-
PALSA	When PAL625 register is set to high, PAL-BDGHI mode is selected. When PAL625 register is set to low, NTSC mode is selected.	When PAL625 register is set to high, PAL-Nc mode is selected. When PAL625 register is set to low, PAL-M mode is selected.	-

6.2. Clock Timing

A clock signal with a frequency twice the luminance sampling rate must be present at the CLK pin. All setup and hold timing specifications are measured with respect to the rising edge of this signal.

6.3. Pixel Input Timing

6.3.1. Pixel sequence

Multiplexed Y, Cb, and Cr data is input through the DATA[7:0] inputs. By default, the input sequence for active video pixels

must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR-656. This pattern begins during the first CLK period after the falling edge of HSYNC* (regardless of the setting of SLAVE/MASTER mode). The order of Cb and Cr can be reversed by setting the CBSWAP pin. **Figure 1** illustrates the timing. If the pixel stream input to the SPCA717A is off by one CLK period, the SPCA717A can lock to the pixel stream by setting the YCSWAP register. This would solve the problem of having the Y and Cr/Cb pixels swapped.
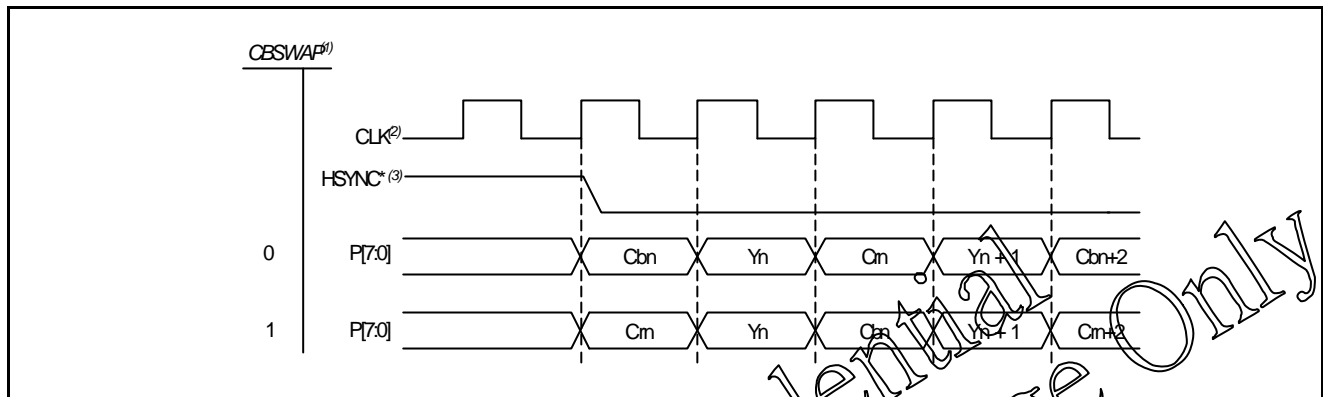
Figure 1. Pix Sequence

Note1: CBSWAP is pin 11.

Note2: Pixel transitions must occur observing setup and hold timing about the rising edge of CLK.

Note3: Pixel sequence will beging with Cbn at 4 x m clock periods following the falling edge of HSYNC*, when m is an integer.

6.4. Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR-624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, and the burst envelope are internally controlled. Video timing figures follow the text in this section.

6.4.1. Sync and burst timing

Table 3 lists the resolutions and clock rates for the various modes of operation.

Table 4 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked. The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync. The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level). The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level).

Table 3. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active pixels	Total Pixels	CLK Frequency (MHz)
NTSC/PAL-M CCIR601	720 x 240	858 x 262	27
PAL-B,D,G,H,I, Nc	720 x 288	864 x 313	27

Table 4. Horizontal Counter Values for Various Video Timings

Operation Mode	Front porch (a)	Horizontal Sync Width (b)	Start of Burst (c)	Duration of Burst (d)	Back porch (e)
NTSC CCIR601	20	63	72	34	127
PAL-B CCIR601	20	63	76	30	142

Note: The unit is the number of luminance pixel.

6.4.2. Master mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, and VSYNC* are output following the rising edge of CLK. The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line. The vertical counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation, it is reset to one, indicating the start of a new field. VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively.

6.4.3. Slave mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of CLOCK. The horizontal counter is incremented on the rising edge of CLOCK. Two clock cycles after falling edge of HSYNC*, the counter is reset to one, indicating the start of a new line. The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field. A falling edge of VSYNC* occurring within ±1/4 of a scan line from the falling edge of HSYNC* cycle time (line time) indicates the beginning of Field 1. A falling edge of VSYNC* occurring within ±1/4 scan line from the mid-point of the line indicates the beginning of Field 2.

The operating mode (NTSC/PAL) can be programmed with the MODEA and MODEB bits when the SETMODE (MASTER pin) bit is set high. Alternatively, when SETMODE is low, the mode is automatically detected in slave mode. For example, 525-line operation is assumed, 625-line operation is detected by the number of HSYNC* edges between VSYNC* edges. The frequency of operation (CCIR/601) for both PAL and NTSC is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz, ±1 count which is detected in between two successive falling edges of HSYNC*.

6.4.4. Burst blanking

For NTSC, color burst information is automatically disabled on scan lines 1-9 and 264-272, inclusive. (SMPTE line numbering convention.) For PAL-B, D, G, H, I , Nc color burst information is automatically disabled on scan lines 1-6, 310-318, and 623-625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1-5, 311-319, and 622-625, inclusive.

6.5. Vertical Blanking Intervals

For NTSC, scan lines 1-9 and 263-272, inclusive, are always blanked. There is no setup on scan lines 10-21 and 273-284 inclusive. All displayed lines in the vertical blanking interval (10-21 and 273-284 for interlaced NTSC; 7-13 and 320-335 for interlaced PAL-B, D, G, H, I) are forced to blank. For PAL-B, D, G, H, I, scan lines 1-6, 311-318, and 624-625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1-5, 311-319, and 624-625, inclusive, are always blanked.

6.6. Digital Processing

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter. The Y and filtered UV components are up-sampled to CLK frequency by a digital filter.

6.7. Subcarrier Generation

To maintain a synchronous sub-carrier relative to HSYNC*, the sub-carrier phase is reset every frame for NTSC and every 8 fields for PAL. The SCA phase is non-zero and depends upon the clock frequency and the video format.

For a perfect clock input, The burst frequency is 4.43361875 MHz for PAL-B, D, G, H, I, 3.57561149MHz for PAL-M, 3.58205625MHz for PAL-Nc (Argentina), 3.579545 MHz for NTSC interlaced.

6.8. Power-Down Mode

In power-down mode (SLEEP pin set to 1), the internal clock is stopped and also an internal reset is forced and the DACs are powered down. When returned low, the device starts from a reset state (horizontal and vertical counters = 0, which is the start of VSYNC in Field 1).
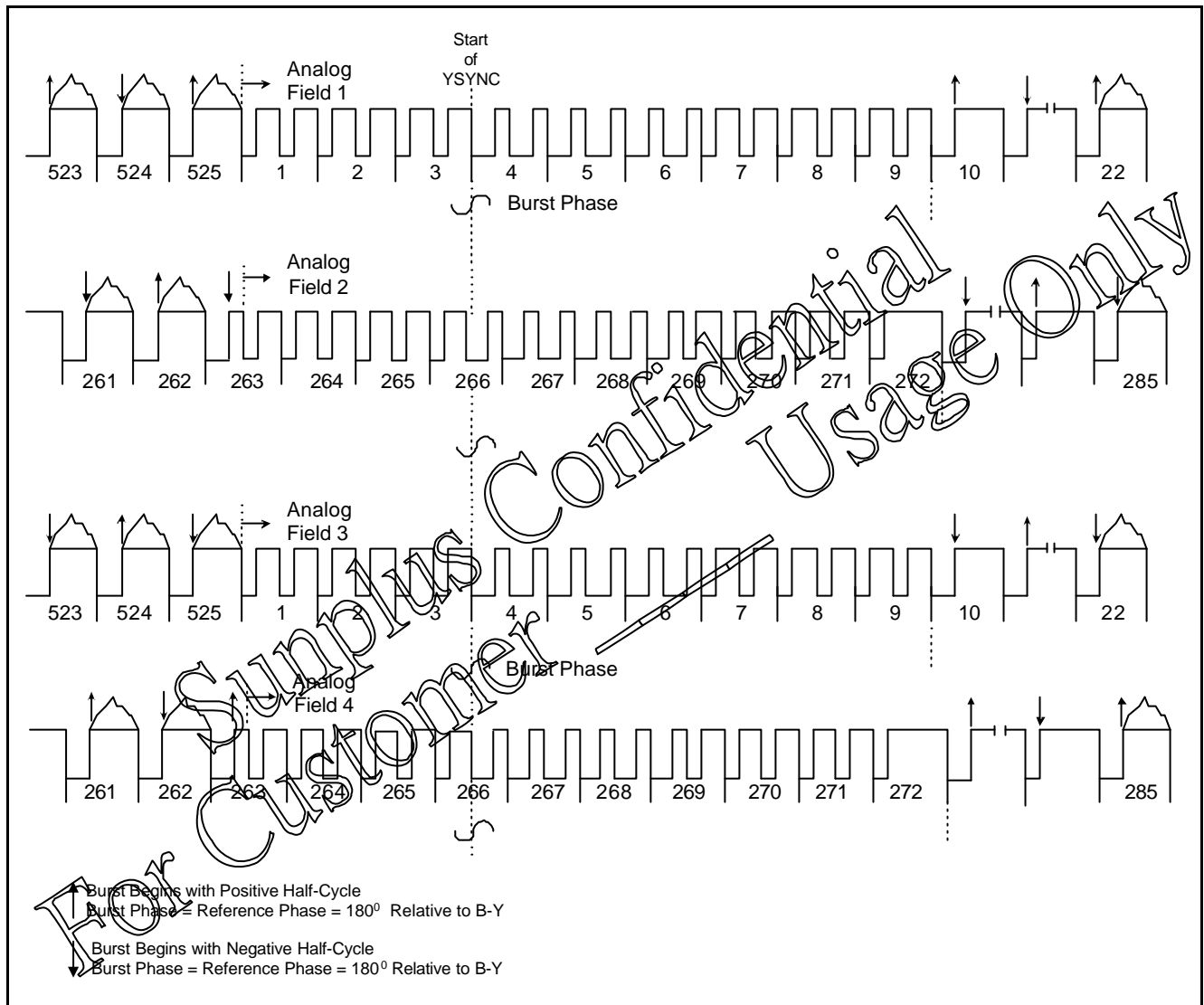
Figure 2. Interlaced 525-Line (NTSC) Video Timing

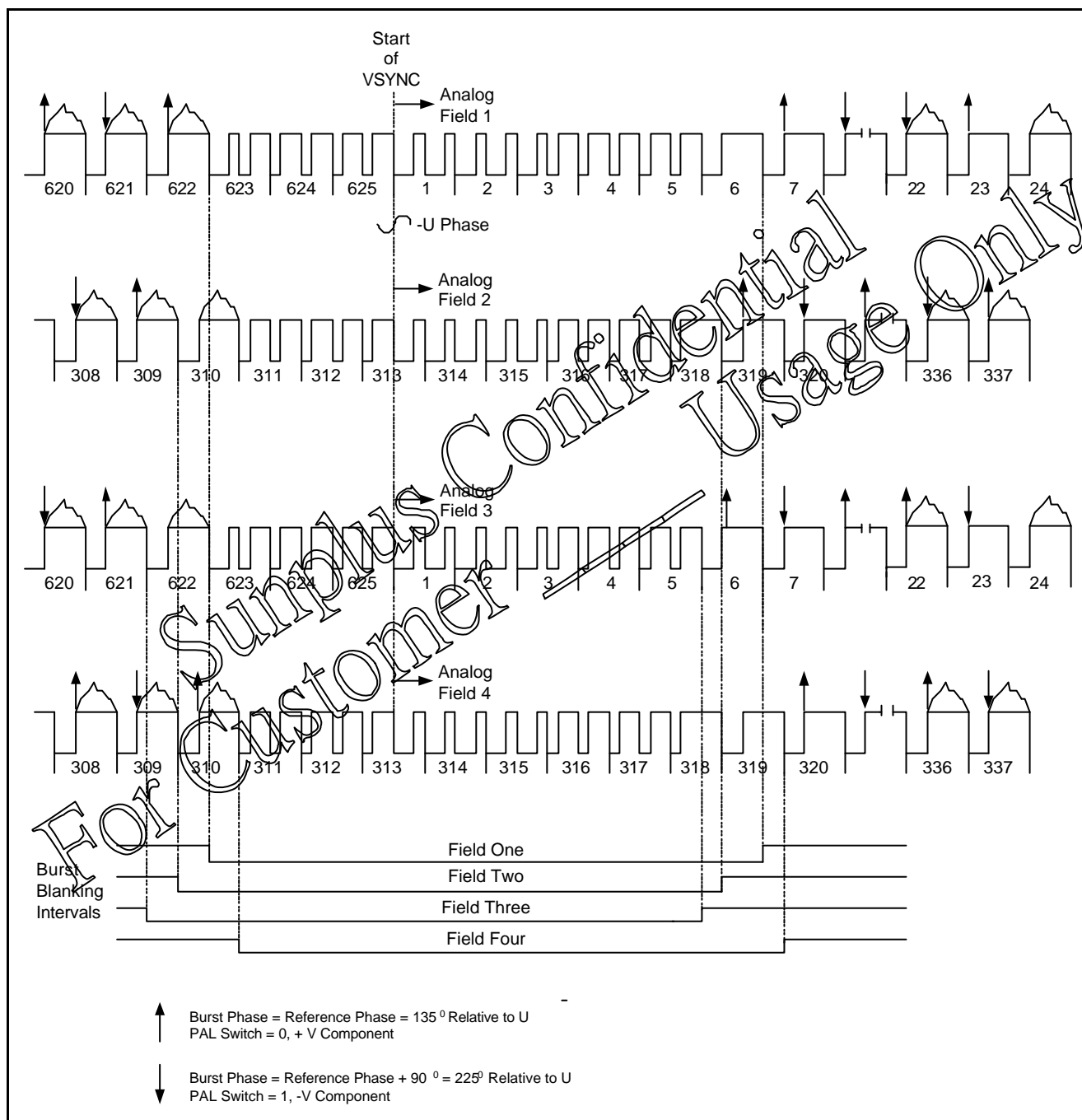**Note:** SMPTE line numbering convention rather than CCIR-624 is used.

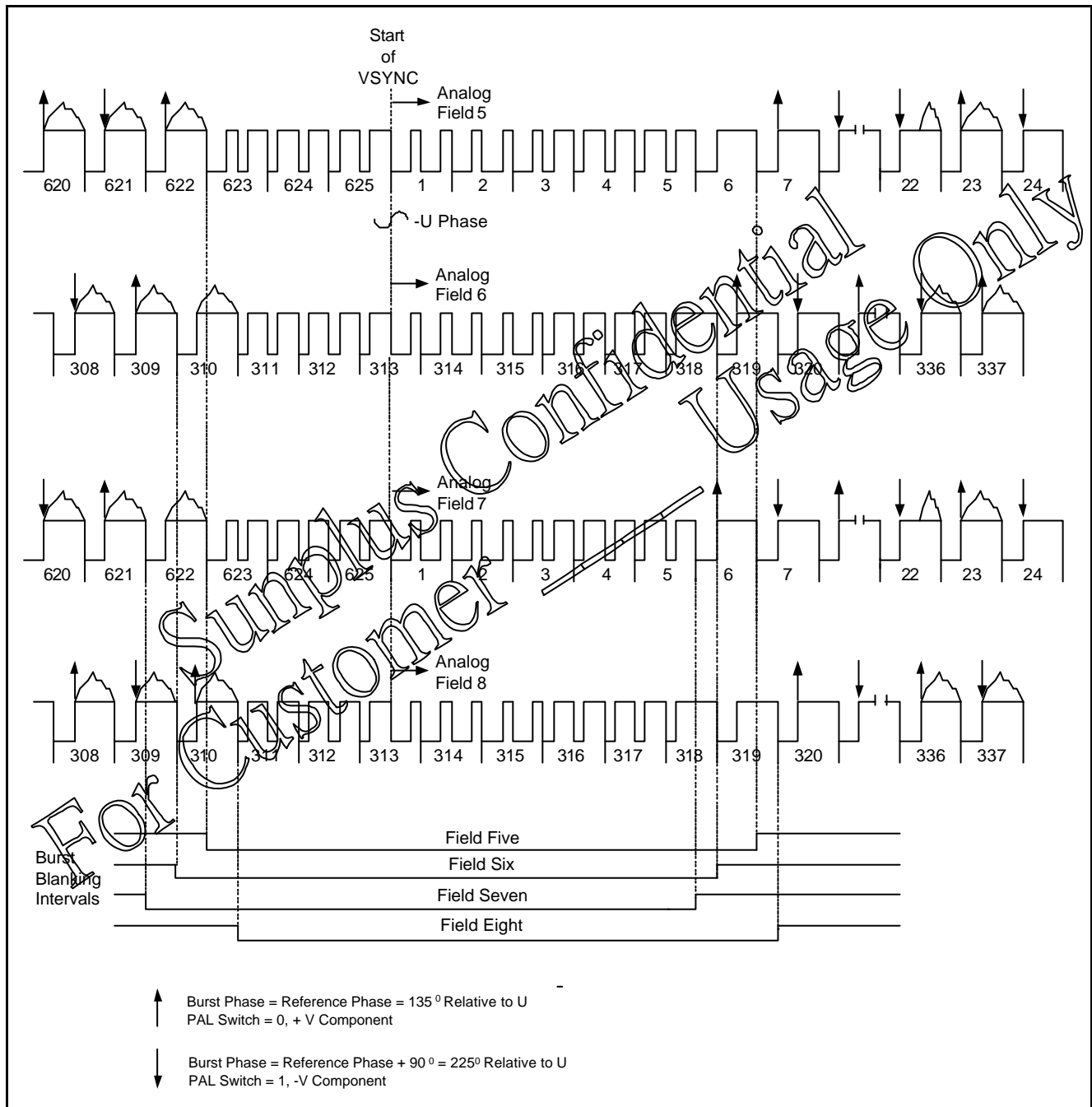**Figure 3a.** Interlaced 625-Line (PAL) Video Timing

Figure 3b. Interlaced 625-Line (PA L) Video Timing

6.9. Pixel Input Ranges And Colorspace Conversion

6.10. YC inputs (4:2:2 YCRCB)

Y has a nominal range of 16-235; Cb and Cr have a nominal range of 16-240, with 128 equal to zero. Y values of 0-15 and 236-255 are interpreted as 16 and 235. CrCb values of 1-15 and 241-254, are interpreted as 16 and 240.

6.11. DAC coding

White is represented by a 9-bit DAC code of 400. For PAL-B, D, G, H, I, Nc the standard blanking level is represented by a DAC code of 126. For NTSC, the standard blanking level is represented by a DAC code of 120.

6.12. Outputs

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Either tone composite video outputs or Y outputs are available (selectable by the LUMA pin). If the SLEEP pin is high, the DAC are essentially turned off and only the leakage current is present.

6.12.1. Composite and luminance (CVBS/Y analog output

When LUMA is a logical zero, digital composite video information drives the 9bit D/A converter that generates the CVBS output. When LUMA is a logical one, digital luminance information drives the DAC that generates the analog Y video output.

7.ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Rating

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply (Measured to ground)	VAA	-	-	4.5	V
Ambient Operating temperature	TA	-40	-	+125	°C
Voltage on Any Signal Pin	-	GND-0.5	-	VAA+0.5	V
Storage Temperature	TS	-65	-	+150	°C
Junction Temperature	TJ	-	-	+150	°C

Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latchup.

7.2. Recommended Operation Conditions

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply	V_{AA}	3	3.3	3.6	V
Ambient Operating temperature	TA	0	-	+70	°C
DAC Output Load	RL	-	37.5	-	Ω
External Voltage Reference	VREFIN	-	1.27	-	V

7.3. DC Characteristics

Characteristics	Symbol	Limit			Unit
		Min.	Tpy.	Max.	
Analog Power Operating Voltage	V_{AA}	3.0	3.3	3.6	V
Digital Power Operating Voltage	VDD	3.0	3.3	3.6	V
Operating Current	I_{OP}	-	90	300	mA
Power Down Mode Current	-	-	20	-	mA
Input High Voltage (Digital Input)	V_{IH}	2.0	-	V_{AA}+0.5	V
Input Low Voltage (Digital Input)	V_{IL}	GND-0.5	-	0.8	V
Output High I (V_{OH}=2.4V) (Digital Output)	I_{OH}	-	-8	-	mA
Output Sink I (V_{OL}=0.8V) (Digital Output)	I_{OL}	-	8	-	mA
VREFOUT Output Voltage	VREFOUT	-	1.27	-	V
VREFOUT Current	IREFOUT	-	10	-	uA

7.4. AC Characteristics
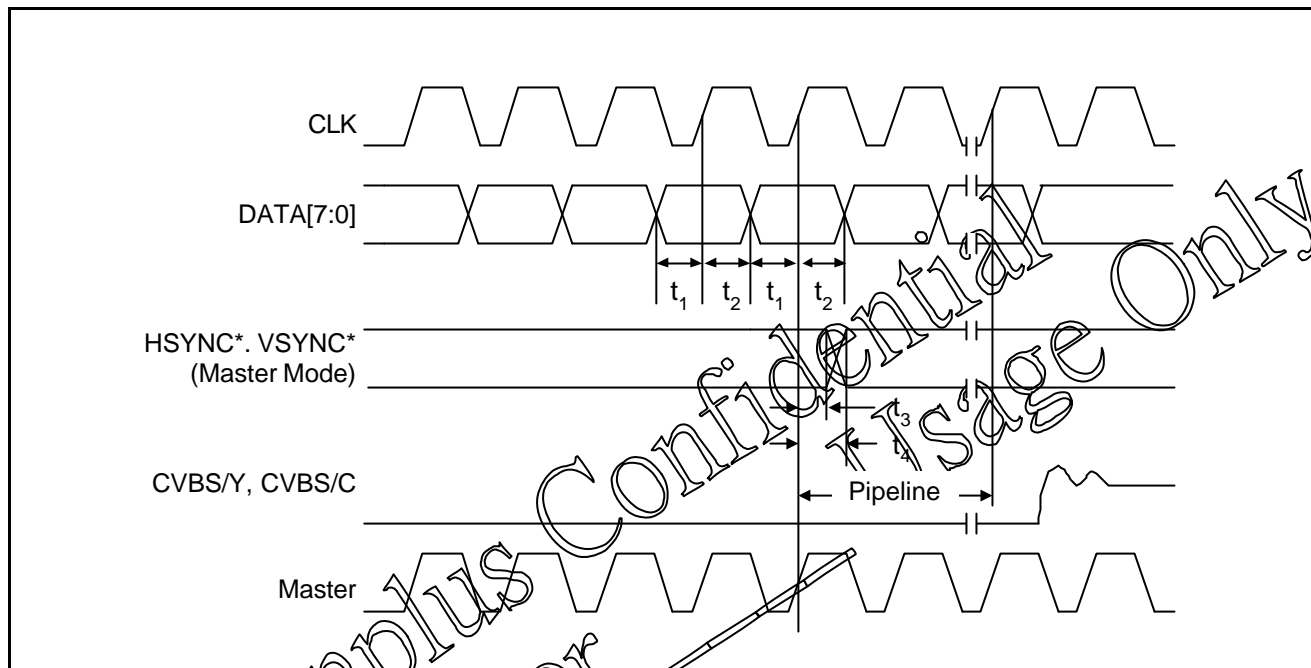
Description	Symbol	Min.	Typ.	Max.	Units
Pixel/Control Setup Time	t1	-	20	-	ns
Pixel/Control Hold Time	t2	-	15	-	ns
Control Output Hold Time	t3	-	7	-	ns
Control Output Delay Time	t4	-	10	-	ns
HSYNC* to Analog Output (Master Mode)	-	-	26	-	CLK Periods
CLK Frequency	-	24.54	27	29.5	MHZ
CLK Pulse Width Low Time	-	-	10	-	ns
CLK Pulse Width High Time	-	-	10	-	ns

8. APPLICATION CIRCUITS

8.1. PC Board Considerations

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing. A well-designed power distribution network is critical to eliminate digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

8.2. Component Placement

Components should be placed as close as possible to the associated pin. The optimum layout enables the SPCA717A to be located as close as possible to the power supply connector and the video output connector.

8.3. Power And Ground Planes

For optimum performance, a common digital and analog ground plane is recommended. Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SPCA717A power pins, VREF circuitry, and COMP decoupling. At least a 1/8-inch gap is required in between the digital power plane and the analog power plane. The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in **Figure 4, Table 6**. This bead should be located within 3 inches of the SPCA717A. The bead provides resistance to switching-currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.
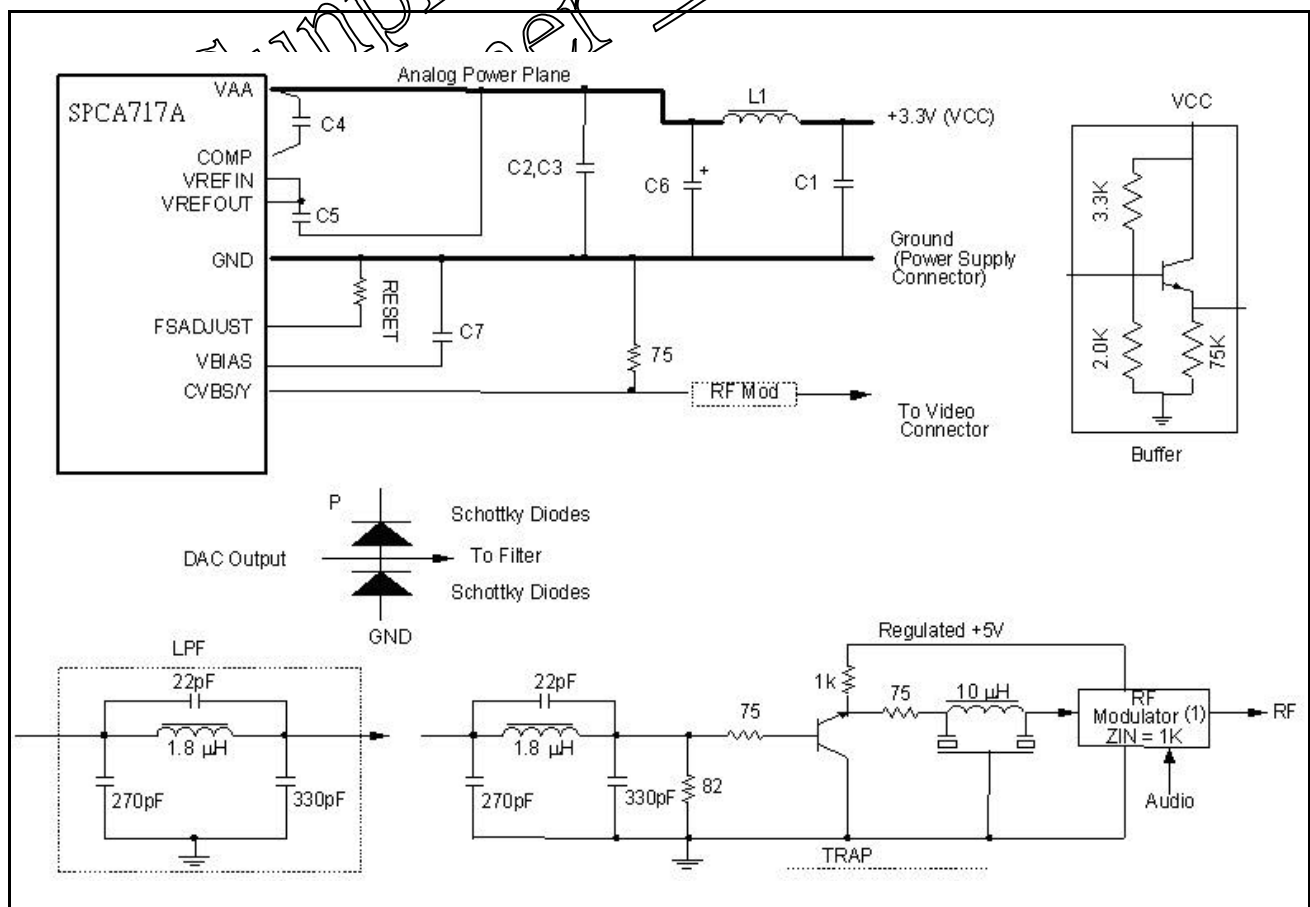

Figure 4. Typical Connection Diagram (Internal Voltage Reference)

Note1: Some modulators may require AC coupling capacitors (10μF).
Note2: Optional for chroma boost.
Note3: VREFIN must be connected to either VREFOUT or VBIAS.

Table 6. Typical Parts List (Internal Voltage Reference)

Locations	Description	Vendor Part Number
C1 - 5, C7	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
L2, L3	Ferrite Bead (z < 300Ω @ 5MHz)	ATC LCB0805, Taiyo Yuden BK2125LM182
RESET	470 or 560 Ω 1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
-	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT64-04 (Dual)

Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect SPCA717A performance.

9.PACKAGE/PAD LOCATIONS

9.1. Package Type: 32 pin LQFP
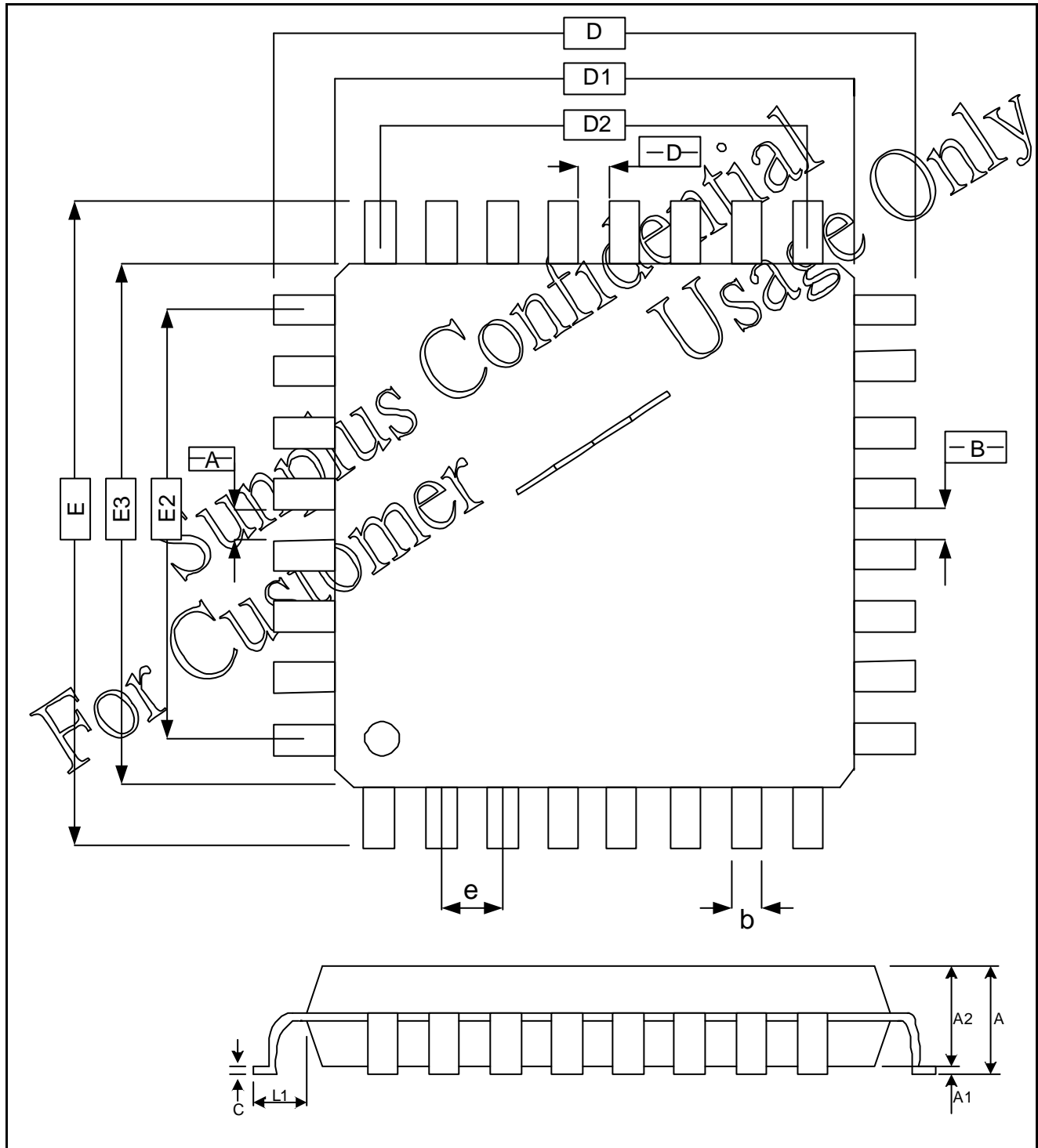
Note: Ambient temperature range: 0℃ - 70℃

9.2. Outline Dimensions

Symbol	MILLIMETER		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	9.00BSC.		
D1	7.00BSC.		
E	9.00BSC.		
E1	7.00BSC.		
R2	0.08	-	0.20
R1	0.08	-	-
	0°	3.5°	7°
1	0°	-	-
2	11°	12°	13°
3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
	1.00REF		
	0.20	-	-

10. DISCLAIMER

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Digital to Audio Converter

GENERAL DESCRIPTION

The SPCA713A is a low cost stereo digital to analog converter for consumer electronic applications such as MP3 player, Mini Disk, audio or video CD player, SVCD, DVD player, CD/DVD- ROM driver, MIDI applications, Karaoke system, and set-top box etc. The SPCA713A provides, not only the latest technology, but also the full commitment and technical support of Sunplus.

BLOCK DIAGRAM
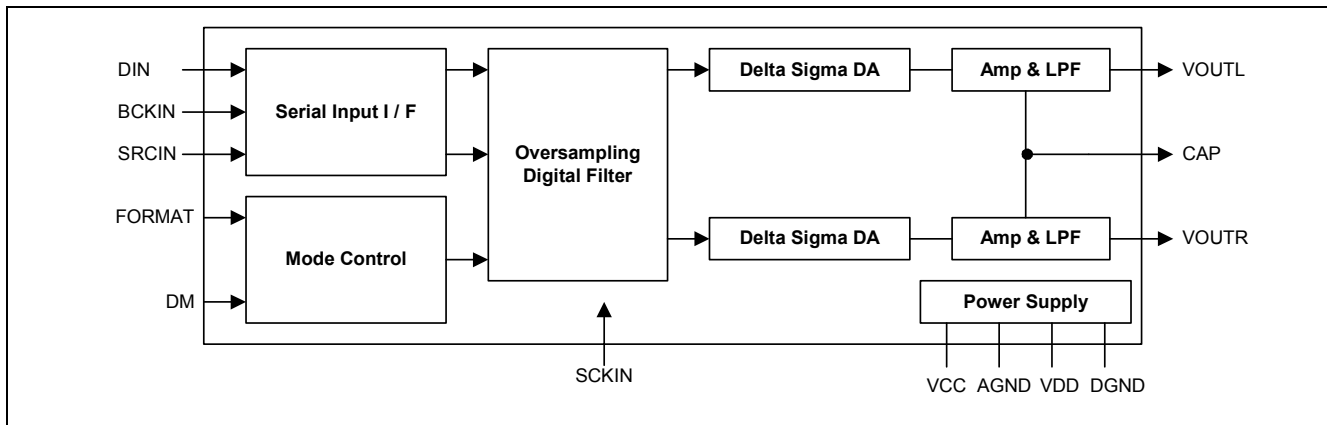
FEATURES

- High resolution:
    —16 Bit Normal/IIS Format Selectable
- 14 pin SOP package
- High performance:
    —THD+N: -90 dB
    —Dynamic Range: 96dB
    —S/N Ratio: 100db

- High integration:
    —Oversampling Digital Filter
    —High-Resolution Delta Sigma DAC
    —Analog Low Pass Filter
    —Output Amplifier
    —On-Chip Digital Filters for:
    —De-emphasis at 44.1kHz

FUNCTION DESCRIPTION

1. SYSTEM CLOCK

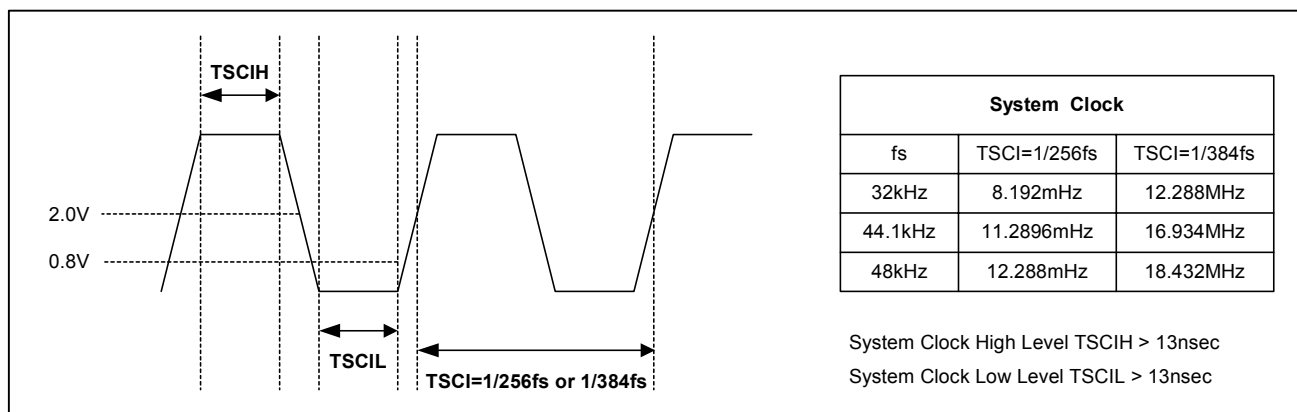The system clock is either 256fs or 384fs where fs is the standard audio frequency including 32Khz, 44.1Khz, and 48KhZ. The system clock is used to operate the digital filter and delta sigma modulator. The system clock is input through SCKIN (pin14).

System Clock		
fs	TSCI=1/256fs	TSCI=1/384fs
32kHz	8.192mHz	12.288MHz
44.1kHz	11.2896mHz	16.934MHz
48kHz	12.288mHz	18.432MHz

System Clock High Level TSCIH > 13nsec
System Clock Low Level TSCIL > 13nsec

2. SERIAL DIGITAL AUDIO DATA INPUT INTERFACE

Digital audio information is input to the SPCA713A via the DIN (pin2) for audio data input, the SRCIN (pin1) for sampling rate clock, and the BCKIN (pin3) for the bit clock. The SPCA713A can accept both normal and IIS data formats. The normal data format is MSB first, two's complement and right justified; on the other hand, the IIS data format, which is compatible with Philips serial data protocol, is left justified. The relationship of the three input signals is illustrated in the following figures:

Normal Data Format (right justified):

IIS Data format (Left Justified):
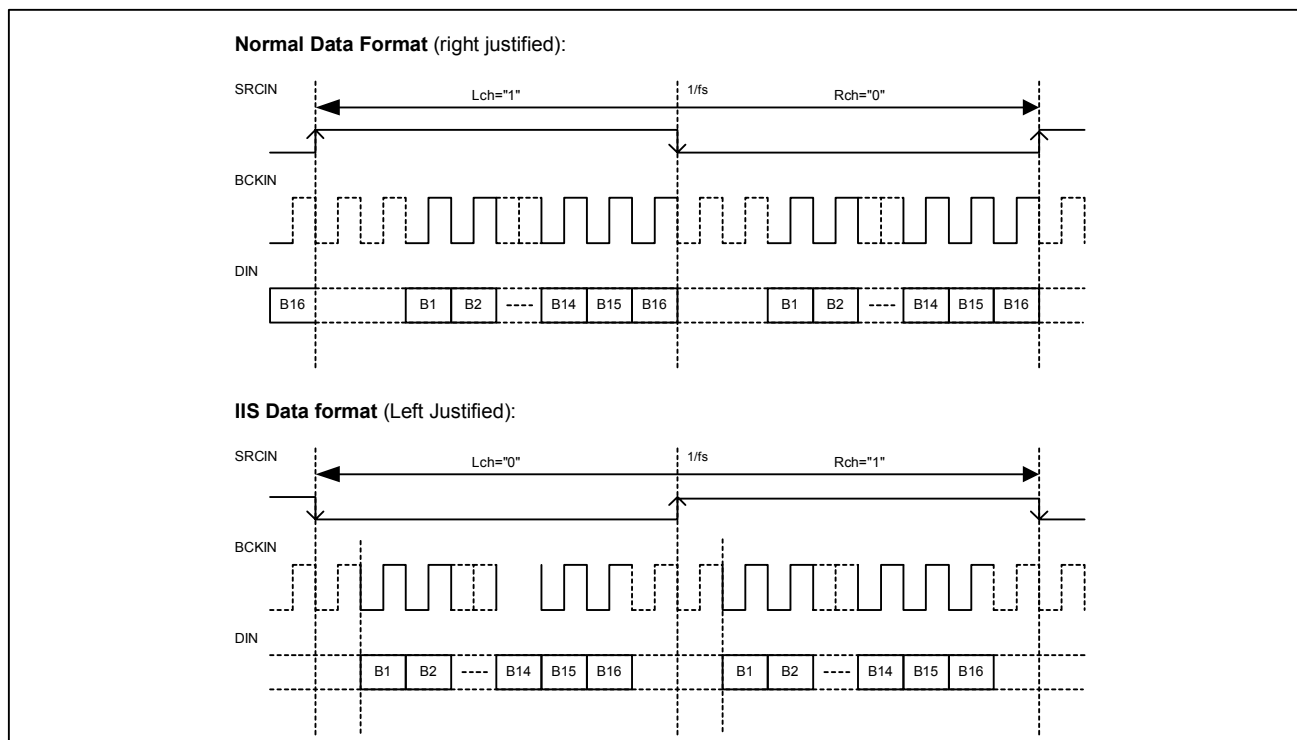
Note: Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

3. INTERNAL RESET

When the power supply voltage VCC reaches 2.2V, the internal reset function is initialized. The power-on reset initialization period is 1,024 SCKIN cycles during which the analog out puts are forced to VCC/2.

4. MODE CONTROL

The SPCA713A provides two control functions – Input Format Select and De-emphasis through FORMAT (pin 13) and DM (pin12). They are illustrated in following table:

Table1: Selectable Functions

Function	Control
Digital Audio input Format Selection	FORMAT (pin13) = "0" Normal format selected.
	FORMAT (pin13) = "1" IIS format selected
De-emphasis Control at 44.1kHz	DM (pin12) = "0" De-emphasis OFF
	DM (pin12) = "1" De-emphasis ON

PIN ASSIGNMENTS

Mnemonic	PIN NO.	I/O	Description
SRCIN	1	IN	Sample Rate Clock Input
DIN	2	IN	Audio Data Input
BCKIN	3	IN	Bit Clock Input for Audio Data
NC	4	-	No Connection
CAP	5	-	R-Channel & L-Channel Output Amp Common Node
VOUTR	6	OUT	R-Channel Output
GND	7	-	Ground
VCC	8	-	Power Supply
VOUTL	9	OUT	L-Channel Output
NC	10	-	No Connection
NC	11	-	No Connection
DM	12	IN	De-emphasis Control, "H": ON, "L": OFF
FORMAT	13	IN	Data Format Select, "H": IIS Format, "L": Normal Format.
SCKIN	14	IN	System Clock Input

PIN CONFIGURATION

1	SRCIN	SCKIN	14	
2	DIN	FORMAT	13	
3	BCKIN	DM	12	
4	NC	NC	11	
5	CAP	NC	10	
6	VOUTR	VOUTL	9	
7	GND	VCC	8	
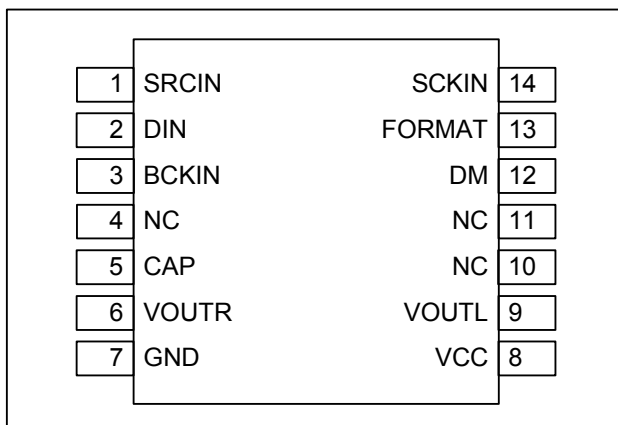
ABSOLUTE MAXIMUM RATING

Power Supply Voltage	+ 6.5V
+VCC to VDD Difference	+/- 0.1V
Input Logic Voltage	-0.3V to (VDD + 0.3V)
Power Dissipation	250mW
Operating Temperature Range	-25 C to +85 C
Storage Temperature	-55 C to +125 C

PACKAGE INFORMATION*

Model	Package	Package Drawing No.
SPCA713A	14 pin SOP	114-D

Note: See Package drawing at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

At 25°C, VCC=VDD=5V/3.3V, fs=44.1kHz, 16Bit input data, System Clock = 384/256fs

Parameter	Conditions	Min.	Type		Max.	Unit
Resolution			16			Bits
Sampling Frequency		16	44.1		96	kHz
System Clock Frequency			256/384fs			
Audio Data Format			Normal/IIS			
Data Bit Length			16			
Power Supply						
Voltage Range: VDD	VDD=5V	4.5	5		5.5	V
	VDD=3.3V	3.0	3.3		3.7	V
Supply Current: IDD	VDD=5V		13		18	mA
	VDD=3.3V		6		10	mA
Power Dissipation:	VDD=5V		65		90	mW
	VDD=3.3V		20		33	mW
Digital Input/Output						
Input Logic Level						
VIH	Pin14	60%				VDD
VIL					16%	VDD
VIH	Pin1,2,3,12,13	60%				VDD
VIL	--Schmitt Trigger				25%	VDD
Output Logic Level						
VOH		90%				VDD
VOL					10%	VDD
DC Accuracy						
Gain Error			+/- 1		+/- 5	%FSR
Gain Mismatch Ch to Ch			+/- 1		+/- 5	%FSR

| Analog Output | | | VDD | | | |
			5V	3.3V		
Voltage Range	Vout=0dB		1.1	0.7		Vrms
Center Voltage			2.5	1.65		V
Load Impedance	AC Load	10				KOhm
Frequency Response		0			20	KHz

| Dynamic Performance | | | VDD | | | |
			5V	3.3V		
THD+N at FS(0dB)	Fout=1kHz		.003	.0035	0.006	%
THD+N at –60dB	Fout=1kHz		1.8	2.0	5	%
Dynamic Range	EIAJ, A-weighted	90	96	94		dB
SNR	EIAJ, A-weighted	92	100	97		dB
Channel Separation	Fout=1kHz	90	97	95		dB

TIMING CHARACTERISTICS

At 25°C, VCC = VDD = 5V/3.3V, fs = 44.1kHz, 16Bit input data, System Clock = 384/256fs

Parameter	Symbol	Value	Unit
Data Input Timing			
DIN setup time	tds	>30	ns
DIN hold time	tdh	>30	ns
BCKIN high-level, low-level	Tbcwh, tbcwl	>50	ns
BCKIN pulse cycle time	tbcy	>100	ns
BCKIN rising edge to SRCIN	tbsr	>30	ns
SRCIN to BCKIN rising edge	tsrb	>30	ns

TIMING DIAGRAM

DATA INPUT TIMING
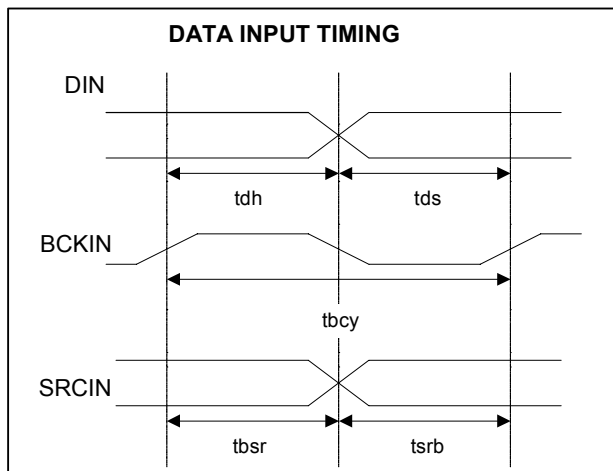
APPLICATION CIRCUIT NOTE
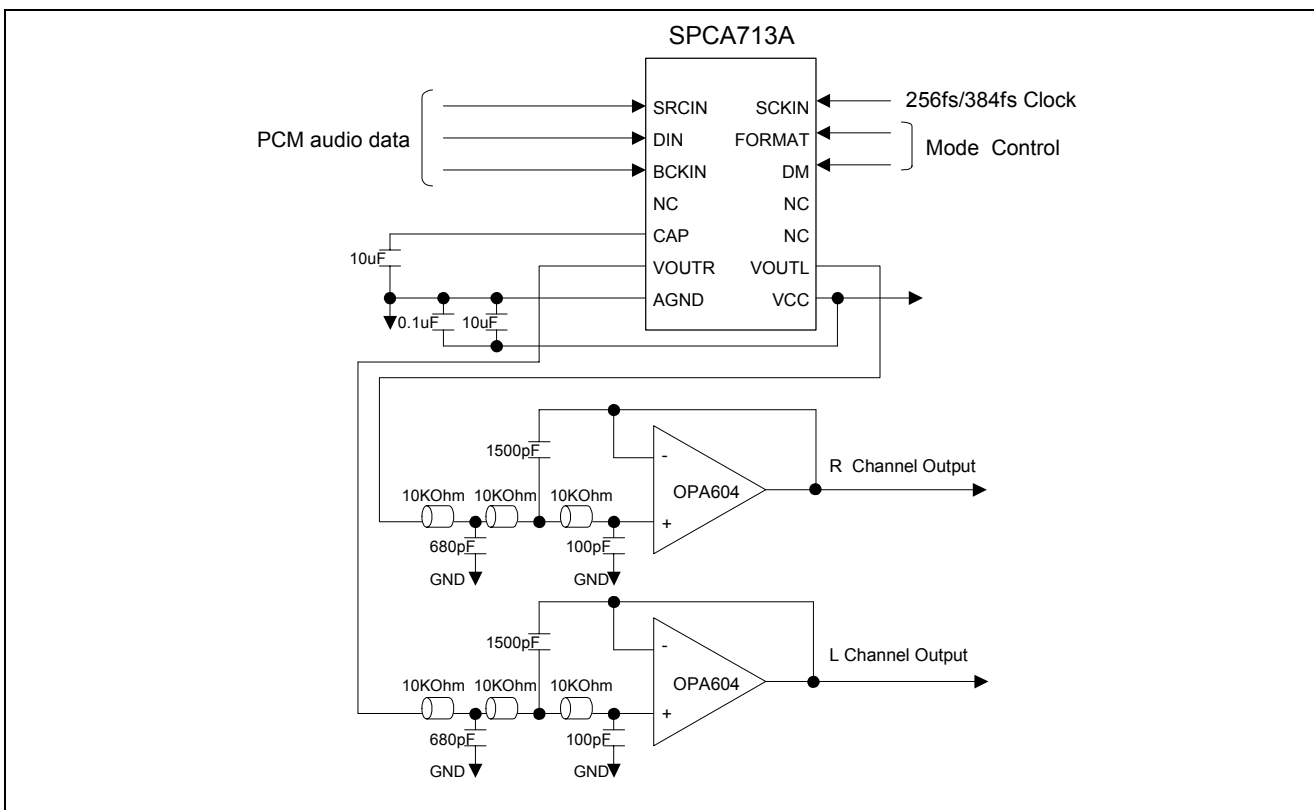
1. BYPASSING POWER SUPPLY

A 10uF tantalum capacitor can be used for bypassing the power supplies. The bypass capacitor should be connected as close as possible to the unit and a 0.1uF ceramic capacitor is recommended to connect in parallel with it.

2. OUTPUT FILTERING

The internal low pass filter is designed to have a 3dB band width at 100kHz. To limit out of band noise, an external 3rd order filter, as shown in the application circuit diagram, is recommended, especially when the chip is to drive a wide band amplifier.

PACKAGE DRAWING NO. 114-S

Model	Package	Package Drawing No.
SPCA713A	14 pin SOP	114-S

Package outline drawing is shown below:

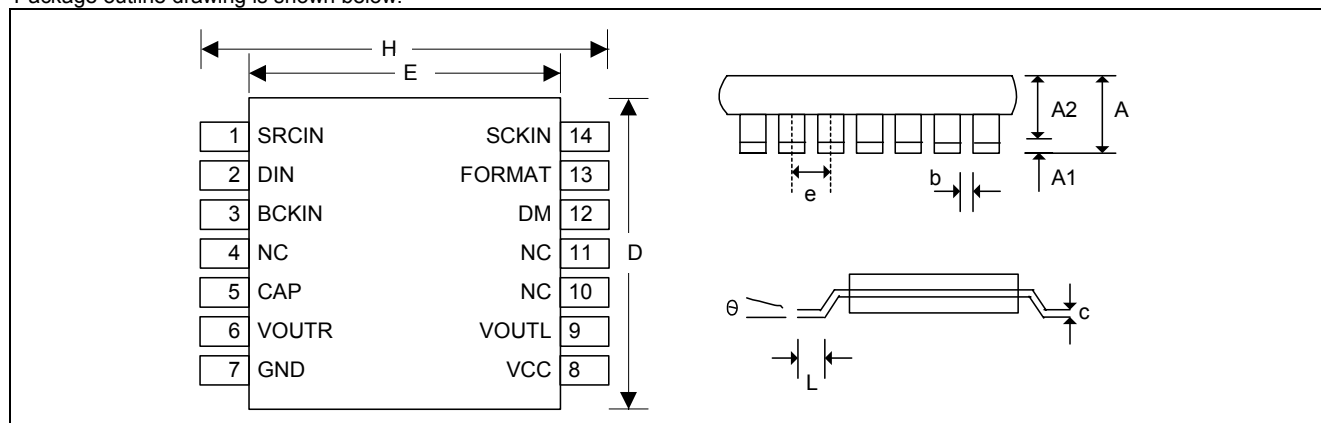| Symbols	Dimensions In Milimeters			Dimensions In Inches		
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
H	5.79	5.99	6.20	0.228	0.236	0.244
E	3.81	3.91	3.99	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
L	0.38	0.71	1.27	0.015	0.028	0.050
θ	0°		8°	0°		8°

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REVISION HISTORY

Date	Revision #	Description	Page
APR. 03, 2001	1.0	Original	7

11. REVISION HISTROY

Date	Revision #	Description	Page
NOV. 11, 2002	0.1	Original	21

IC

CD-ROM

BH3541F / BH3544F

BH3541F、BH3544F はデジタルソース向けのデュアルヘッドホンアンプです。BH3541F はゲイン 0dB、BH3544F はゲイン 6dB 固定で、外付けゲイン設定が不要です。BH3541F、BH3544F ともミュート機能を内蔵することによって電源 ON-OFF 時のボツ音防止対策が簡単に行えます。また、サーマルシャットダウン回路の内蔵により、短絡などによる IC 破壊を防止します。

BH3541F	0dB
BH3544F	6dB

●用途

CD-ROM、CD、MD、パソコン、ノートパソコン、カムコーダなどヘッドホン出力を有する機器

●特長

１）ミュート機能内蔵によって電源 ON-OFF 時のボツ音防止対策が可能。
２）サーマルシャットダウン回路（150°C）内蔵によって短絡による IC 破壊を防止。
３）SOP8pin の小型パッケージである。

●絶対最大定格 （Ta = 25°C）

Parameter	Symbol	Limits	Unit
	VMax	7.0	V
	Pd	450 ∗	mW
	Topr	−25 ~ +75	°C
	Tstg	−55 ~ +125	°C

∗Ta=25°C   1°C   4.5mW

●推奨動作条件 （Ta = 25°C）

Parameter	Symbol	Min.	Typ.	Max.	Unit
	Vcc	2.8	−	6.5	V

ROHM

IC

●ブロックダイアグラム

( ) BH3544

IC
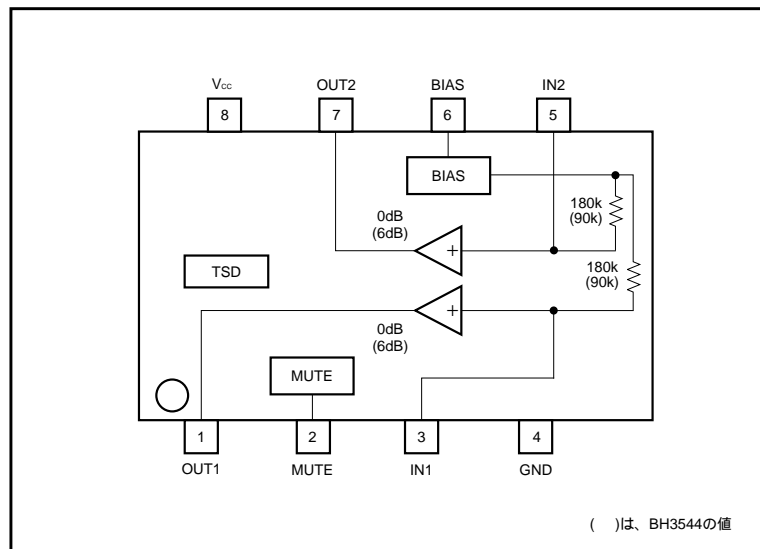
●各端子説明

Pin No.		I / O			
1	OUT1	O	2.1V		
7	OUT2	O	2.1V Vcc=5V		
2	MUTE	I	0.1V Open		ON OFF Lo Hi MUTE Lo Open
3	IN1	I	2.1V		
5	IN2	I	2.1V Vcc=5V		
6	BIAS	I / O	2.1V Vcc=5V		47μF
4	GND	I	–		
8	Vcc	I	–		

IC

● 電気的特性 （特に指定のない限り Ta = 25°C, Vcc = 5.0V, RL = 32Ω, f = 1kHz,
　　　　　　　BH3541F : VIN = 0dBV, BH3544F : VIN = −6dBV）

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
		IQ	4	7	10	mA	VIN=0Vrms
		VTM	0.3	0.7	1.6	V	−
	BH3541F	GVC	−2	0	2	dB	−
	BH3544F		4	6	8	dB	−
		GVC	−0.5	0	0.5	dB	−
		THD	−	0.02	0.1	%	BW=20~20kHz
1		PO1	25	31	−	mW	RL=32Ω, THD < 0.1%
2		PO2	50	62	−	mW	RL=16Ω, THD < 0.1%
		VNO	−	−93	−85	dBV	BW=20~20kHz, Rg=0Ω
		CS	82	90	−	dB	Rg=0Ω
		ATT	70	80	−	dB	Rg=0Ω
		RR	50	57	−	dB	fRR=100Hz, VRR=−20dBV

● 測定回路図

Fig.1

( )　BH3544

IC
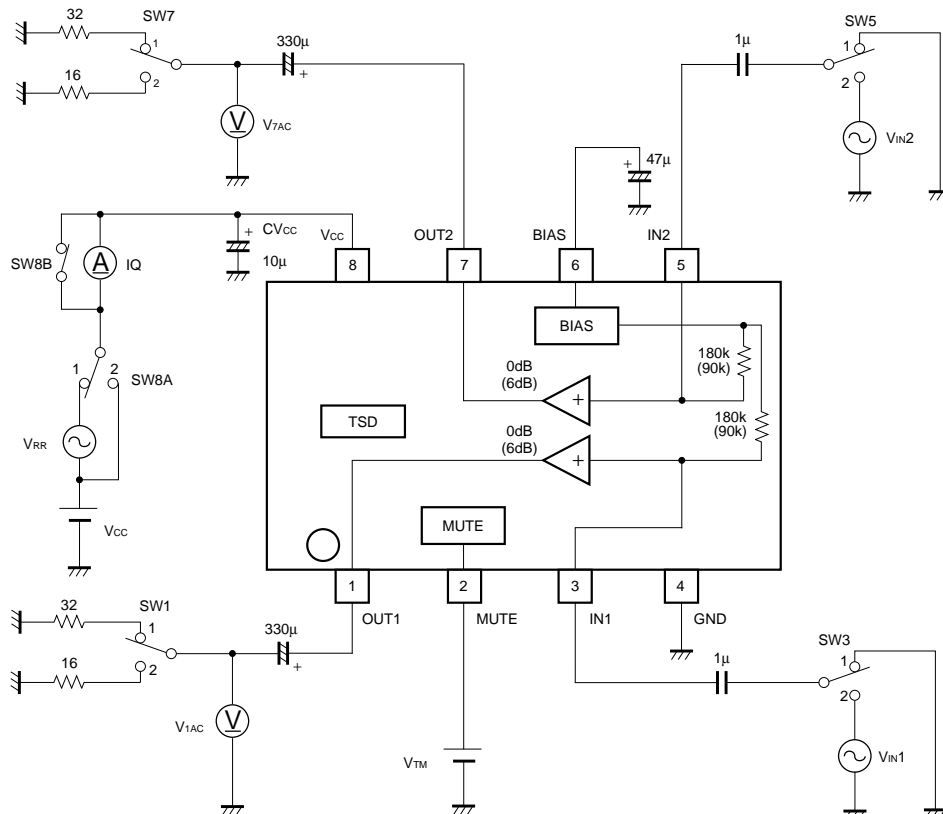
●測定条件表

	SW						Monitor	Conditions
	SW1	SW3	SW5	SW7	SW8A	SW8B		
I_Q	1	1	1	1	2	OFF	IQ	–
V_{TM}	–	–	–	–	–	–	–	–
G_{VC}	1	2	2	1	2	ON	V1AC, V2AC	f=1kHz, $V_{IN}1/2$=0dBV ($V_{IN}1/2$=−6dBV), VTM=1.6V
G_{VC}	–	–	–	–	–	–	–	GVC1−GVC2
THD	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, $V_{IN}1/2$=0dBV ($V_{IN}1/2$=−6dBV), VTM=1.6V
P_{O1}	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, $V_{IN}1/2$=0dBV ($V_{IN}1/2$=−6dBV), VTM=1.6V
P_{O2}	2	2	2	2	2	ON	V1AC, V2AC	fin=1kHz, $V_{IN}1/2$=0dBV ($V_{IN}1/2$=−6dBV), VTM=1.6V
V_{NO}	1	1	1	1	2	ON	V1AC, V2AC	–
CS	1 1	1 2	2 1	1 1	2 2	ON ON	V1AC, V2AC V1AC, V2AC	fin=1kHz, $V_{IN}2$=0dBV ($V_{IN}2$=−6dBV), VTM=1.6V fin=1kHz, $V_{IN}1$=0dBV ($V_{IN}1$=−6dBV), VTM=1.6V
ATT	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, $V_{IN}1/2$=0dBV ($V_{IN}1/2$=−6dBV), VTM=0.3VB
RR	1	1	1	1	1	ON	V1AC, V2AC	V_{RR}=−20dBV, f_{RR}=100Hz
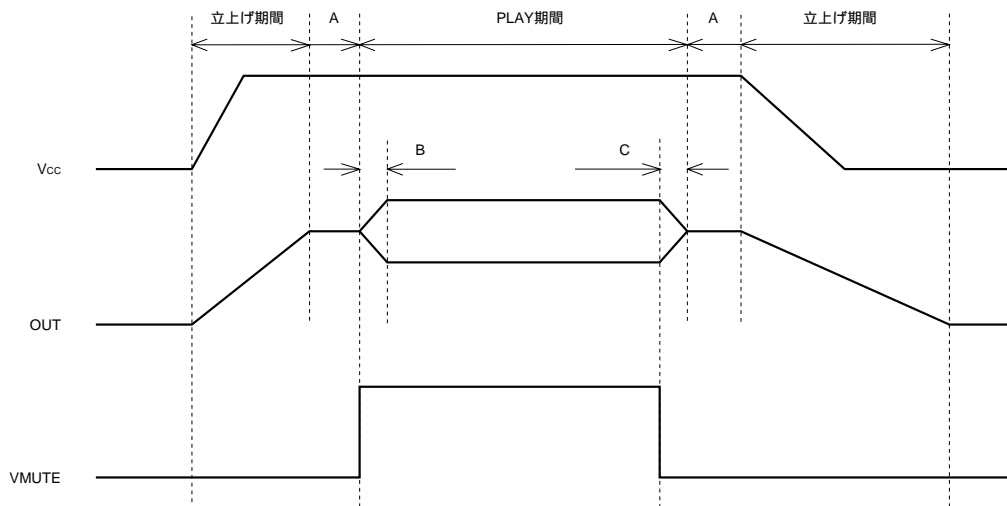
*( ) BH3544F

●動作説明

立上げタイミング

A		ON/OFF	V_{MUTE}=Lo
B		C2,R2	
C			

IC

●応用例
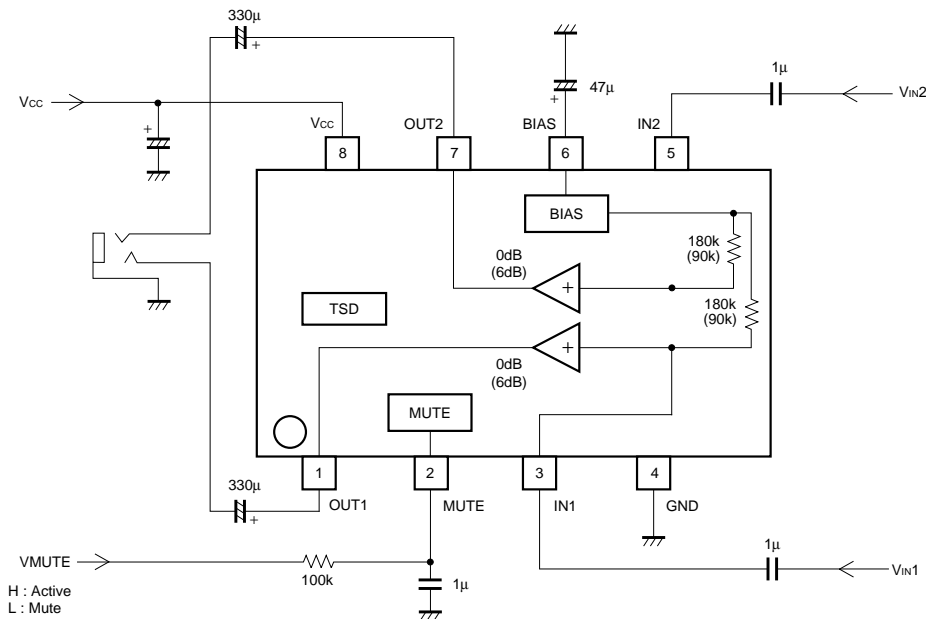
Fig.2

( ) BH3544

●外付け部品の説明

(1) 入力カップリングコンデンサ（C3、C5）
低域のカットオフ周波数により決定されます。本 IC の入力インピーダンスは 180kΩのため、下記の式から求められますが、バラツキ、温特等の考慮を必要とします。（積層セラミックコンデンサを推奨します。）

$$C3\ (C5) = 1 / (2\pi \times 180k\Omega \times f)$$

(2) バイアスコンデンサ（C6）
V_{CC} = 5V の時は 47μF、V_{CC} = 3V の時は 33μF を推奨します。容量値をあまり下げますと、電気的特性の悪化やボツ音の発生原因となりますので、変更の際は十分ご確認のうえ、決定してください。

(3) ミュート端子ボツ音対策（R2、C2）
GND に対してインピーダンス（190kΩ）を持っているため、R2 を大きくしすぎますと、ミュートが解除できないことがありますのでご注意願います。

(4) 出力カップリングコンデンサ（C1、C7）
低域のカットオフ周波数により決定されます。出力の負荷抵抗値を R_L として（出力に保護または、電流制限のために抵抗 R_X を入れると仮定する）、下記の式から求められます。

$$C1\ (C7) = 1 / (2\pi \times (R_L + R_X) \times f)$$

(5) 入力ゲイン調整抵抗（R3、R4）（BH3544F のみ）
外付け抵抗（R3、R4）により、入力ゲインの調整ができます。下記の式から求められるゲインに設定できます。

$$G_{VC} = 6 + 20\log (90k\Omega / (90k\Omega + R3))\ [dB]$$

●使用上の注意
応用例は推奨すべきものと確信しておりますが、ご使用にあたっては特性の確認を十分にお願いします。その他外付け回路定数を変更してご使用になる時は静特性のみならず、過渡特性も含め外付け部品及び当社 IC のバラツキ等を考慮して十分なマージンを見て決定してください。

IC

● 電気的特性曲線

Fig.3

QUIESCENT CURRENT : I$_Q$ (mA)
SUPPLY VOLTAGE : V$_{CC}$ (V)
Ta=25°C
R$_L$=32Ω
MUTE : OFF
MUTE : ON

Fig.4

BIAS DC VOLTAGE : V$_{BIAS}$ (V)
OUTPUT DC VOLTAGE : V$_O$ (V)
SUPPLY VOLTAGE : V$_{CC}$ (V)
Ta=25°C
R$_L$=32Ω

Fig.5

OUTPUT VOLTAGE : V$_{OUT}$ (dBV)
MUTE CONTROL VOLTAGE : VTM (V)
Ta=25°C
R$_L$=32Ω
V$_{CC}$=5V
V$_{IN}$=0dBV
f=1kHz

Fig.6

VOLTAGE GAIN : G$_{VC}$ (dB)
FREQUENCY : F (Hz)
BH3544F
BH3541F
Ta=25°C
R$_L$=32Ω
V$_{IN}$=0dBV
V$_{CC}$=5V

Fig.7   I

TOTAL HARMONIC DISTORTION : THD (%)
OUTPUT VOLTAGE : V$_O$ (dBV)
Ta=25°C
R$_L$=32Ω
V$_{CC}$=5V
f=10kHz
f=1kHz
f=100Hz

Fig.8   II

TOTAL HARMONIC DISTORTION : THD (%)
OUTPUT VOLTAGE : V$_O$ (dBV)
Ta=25°C
R$_L$=32Ω
V$_{CC}$=3V
f=10kHz
f=1kHz
f=100Hz

Fig.9   III

TOTAL HARMONIC DISTORTION : THD (%)
OUTPUT VOLTAGE : V$_O$ (dBV)
Ta=25°C
R$_L$=16Ω
V$_{CC}$=5V
f=10kHz
f=1kHz
f=100Hz

Fig.10   IV

TOTAL HARMONIC DISTORTION : THD (%)
OUTPUT VOLTAGE : V$_O$ (dBV)
Ta=25°C
R$_L$=16Ω
V$_{CC}$=3V
f=10kHz
f=1kHz
f=100Hz

Fig.11

CHANNEL SEPARATION : CS (dB)
FREQUENCY : f (Hz)
Ta=25°C
R$_L$=32Ω
Rg=0Ω
V$_{CC}$=5V

ROHM

IC

Fig.12

Fig.13

Fig.14

●外形寸法図 （Units : mm）

SOP8

265

2F15-3.pcb — Sat Dec 06 10:41:35 2003

| 5 | 4 | 3 | 2 | 1 |

RAM_A[0..11]

RAM_D[0..15]

ROM_A[0..17]

VM

R124
10K

ROM_D[0..7]

U2 (1MX16X4 SDRAM)

Signal	Pin	Pin	Signal
RAM_A0	23 A0	D0 2	RAM_D0
RAM_A1	24 A1	D1 4	RAM_D1
RAM_A2	25 A2	D2 5	RAM_D2
RAM_A3	26 A3	D3 7	RAM_D3
RAM_A4	29 A4	D4 8	RAM_D4
RAM_A5	30 A5	D5 10	RAM_D5
RAM_A6	31 A6	D6 11	RAM_D6
RAM_A7	32 A7	D7 13	RAM_D7
RAM_A8	33 A8	D8 42	RAM_D8
RAM_A9	34 A9	D9 44	RAM_D9
RAM_A10	22 A10	D10 45	RAM_D10
RAM_A11	35 A11	D11 47	RAM_D11
RAM_BA0	20 BA0	D12 48	RAM_D12
RAM_BA1	21 BA1	D13 50	RAM_D13
		D14 51	RAM_D14
		D15 53	RAM_D15
RAM_RAS0	19 CS#		
RAM_CAS	18 RAS#		
RAM_WE	17 CAS#	VCC 1	
RAM_DQM0	16 WE#	VCC 14	
	15 DQML	VCC 27	VM
	39 DQMU		
RAM_CLK	38 CLK	GND 28	
	36 NC	GND 41	
	40 NC	GND 54	
	37 CKE		
	43 VCCQ	VCCQ 3	
	49 VCCQ	VCCQ 9	
	52 GNDQ	GNDQ 6	
	46 GNDQ	GNDQ 12	

GND

VM

GND

U2
1MX16X4 SDRAM

268

U3 (SST39VF020 TSOP)

Signal	Pin	Pin	Signal
ROM_A0	20 A0	D0 21	ROM_D0
ROM_A1	19 A1	D1 22	ROM_D1
ROM_A2	18 A2	D2 23	ROM_D2
ROM_A3	17 A3	D3 25	ROM_D3
ROM_A4	16 A4	D4 26	ROM_D4
ROM_A5	15 A5	D5 27	ROM_D5
ROM_A6	14 A6	D6 28	ROM_D6
ROM_A7	13 A7	D7 29	ROM_D7
ROM_A8	3 A8		
ROM_A9	2 A9		
ROM_A10	31 A10	VCC 8	VM
ROM_A11	1 A11	GND 24	GND
ROM_A12	12 A12		
ROM_A13	4 A13		
ROM_A14	5 A14		
ROM_A15	11 A15		
ROM_A16	10 A16		
ROM_A17	6 A17		
R127 0Ω	9 NC		
	30 CE		
	32 /OE		
VM	7 /WE		

GND

R114 10K

U3
SST39VF020 TSOP

P_VDD3   VM

L2
FCM2012K-601B

C18
47uF/6.3V

GND

C19	C20	C21	C22
104	104	104	104

BBK

Title		
	<Title>	
Size A	Document Number <Doc>	Rev 0.1
Date:	Saturday, October 04, 2003	Sheet 2 of 8

AUD_XCK
AUD_LRCK
AUD_DATA
AUD_BLCK

ROUT

/MUTE
MOT_OFF

ROUT
LOUT

270

MIC_ATO

MIC_AIN

MIC_VM

MIC_GND

AUD_VCC3

CVBS

R_PHONE
L_PHONE

MIC_VDD

MIC_GND

MIC_IN
MIC_VM

U5
WM8714 SOP

U6
BH3544 SOP

BA4510*
U7A

MOT_START 4,7

D5
1N4148 SMD
1 2

D4
1N4148 SMD
2 1

K1
>||

GND

P_VDD3

R31
10K

SW2
SK??
3
2
1

GND

P_VDD3

C139 104
C137 104
C136 104

C138
104

C57
10uF/6.3V/1206

GND

R78 3.3K
R61 OPEN

C126
104

GND

U8
GR2003/SMD PCB

1	(RE2)	RE1	26
2	RE3	RD3	25
3	VSS	RD1	24
4	VDD3	RC3	23
5	CDD2	RC2	22
6	CDD1	RC1	21
7	DH2	(RC0)	20
8	DH1	RB2	19
9	(VDD)	RB1	18
10	XOUT1	RB0	17
11	XIN1	RA3	16
12	/RES	(RA2)	15
13	RA0	RA1	14

SCL 1,4

P_VDD3

GND

POW_DET 7

SDA 1,4

271

IR_IN 1

U10
AT138A

IR

R32 10Ω

VCC3

3
2
1

C58
104

C59
10uF/6.3V/1206

GND

KY0 KX0 KX2 KX1

KY2

FR/PRE
K3

VOL-
K2

FF/NEXT
K5

STOP/OFF
K4

VOL+
K6

软体同F9

7,8 CD_VC

MOT_FRDR 7
MOT_FFDR 7
MOT_TRDR 7
MOT_TFDR 7
MOT_SRDR 7
MOT_SFDR 7
MOT_LIM 7
MOT_MDP 7

8 RF_FE
8 RF_SE
8 RF_TE

C60 471
C61 273
C62 471

A_GND

R115 1K

D_GND
D_VDD3

L9 FCM2012K-601B
P_VDD3

C125 104
C64 104
C65 104
C66 104
C63 10uF/6.3V/1206

D_GND

P_VDD3

L10 FCM2012K-601B

7,8 CD_VC

PLL_VDD

C68 224

R34 33K

8 RF_DC
8 RF_AC

C69 104

A_GND

C67 10uF/6.3V/1206

272

R35 10K
R36 100K

C70 102
C71 103

A_GND

R37 10K

R38 3.3K
C73 473

R40 3.3K

R42 820K
C74 101

R41 470K

R44 1M
C75 104

A_GND

U11
CXD3068Q QFP

41 TE
42 CE
43 RFDC
44 ADIO
45 AVSS0
46 IGEN
47 AVDD0
48 ASYO
49 ASYI
50 RFAC
51 AVSS1
52 CLTV
53 FILO
54 FILI
55 PCO
56 AVDD1
57 BIAS
58 VCTL
59 V16M
60 VPCO

40 SE
39 FE
38 VC
37 TES1
36 TEST
35 DVSS1
34 FRDR
33 FFDR
32 TRDR
31 TFDR
30 SRDR
29 SFDR
28 DVDD1
27 FSTO
26 SSTP
25 MDP
24 LOCK
23 PWMI
22 FOK
21 DFCT

20 MIRR
19 COUT
18 DVSS0
17 WDCK
16 C4M
15 SCOR
14 C2PO
13 GFS
12 XPCK
11 XUGF
10 WFCK
9 ATSK
8 SCLK
7 SENS
6 CLOK
5 XLAT
4 DATA
3 MUTE
2 XRST
1 DVDD0

61 DVDD2
62 ASYE
63 MD2
64 DOUT
65 LRCK
66 PCMD
67 BCK
68 EMPH
69 XTSL
70 DVSS2
71 XTAI
72 XTAO
73 SOUT
74 SOCK
75 XOLT
76 SQSO
77 SQCK
78 SCSY
79 SBSO
80 EXCK

CD_SCOR 1
CD_C2PO 1

CD_SENS 1
CD_CLOK 1
CD_XLAT 1
CD_DDAT 1

CD_XRST 1

R39 10K

D_GND

AUD_DEM 4

CD_SQCK 1
CD_SQSO 1

R120 100Ω

R43 7.5K

x5 16.9344MHz

C76 22pF
C77 22pF

D_GND

1 CD_LRCK
1 CD_DATA
1 CD_BLCK

D14
1N4148 SMD

P_VDD3

L14
FCM2012K-601B

RF_VDD

C106
105

C121
47uF/6.3V

C103
47uF/6.3V

C104
104

C105
104

L15
FCM2012K-601B

R83
10Ω

Q10
3906

RF_VDD

A_GND

A_GND

RF_VDD

C107
47uF/6.3V

R84
1K

C108
100uF/6.3V

CN8
16P1.0mm SMD

C109 105

R86
1M

A_GND

U15

Pin	Signal		Pin	Signal
1	AGCVTH		20	VCC
2	LD		19	LD_ON
3	PD		18	AGCCONT
4	PD1		17	RFTC
5	PD2		16	RFI
6	VEE		15	RFO
7	F		14	RFM
8	E		13	FE
9	EI		12	FE_BIAS
10	VC		11	TE

CXA2550N SSOP

RF_LDON 1

RF_I
RF_O
RF_M

R85 68K
R87 68K
R88 180K
R89 180K

A_GND

RF_VDD

C110
100uF/6.3V

C111
104

R90 15K   RF_FE 6
R91 15K   RF_TE 6
R93 100K   RF_SE 6

R116
NC

A_GND

C112
100uF/6.3V

C113
104

R94
10K

CD_VC 6,7

A_GND

CD_VC

MOT_F+ 7
MOT_T- 7
MOT_T+ 7
MOT_F- 7

A_GND

R95
91Ω

274

A_GND

RF_VDD

R96
22K

Q11
3904

R97 3.3K   RF_SPEED 1

RF_M
RF_I
RF_O

R98
2.2K

R99
130Ω

C114 56pF

C115 68pF

CD_VC

R101
3.3K

R100
5.6K

C116
103

R102 1.8K   RF_DC 6

C117 152   RF_AC 6

RF LDON:	
low	CD-ROM
high	off

RF SPEED:	
low	2X
high	1X

BBK

Title
<Title>

Size
A

Document Number
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Rev
0.1

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