

A Novel Integrated Current Doubler Rectifier*

Peng Xu, Qiaoqiao Wu, Pit-Leong Wong and Fred C. Lee

Center for Power Electronics Systems
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061 USA

ABSTRACT

This paper presents an innovative current doubler rectifier, which integrates all the magnetic components into a single core and minimizes the number of high current windings. Compared to the conventional approach, the proposed integrated magnetic structure features reduced core loss, smaller core size, and reduced AC conduction losses, all while still reducing winding losses. The new rectification circuit can be applied to many topologies. An asymmetrical half-bridge converter was used as one attractive example to demonstrate the operation and performance of the proposed structure. A prototype featuring 400V input, 48V output, 200KHz switching frequency, and 1KW output power was also developed based on this topology.

I. INTRODUCTION

As an alternative rectification circuit, the current doubler rectifier has been proven to be promising for high current DC-DC converters [1-5]. The applications for this kind of converter include high-input Voltage Regulator Modules (VRMs), both load-end converters and front-end modules of Distributed Power Systems (DPS), and etc. Compared with the conventional center-tap rectifier, the current doubler rectifier simplifies the structure of the isolation transformer, and cuts the secondary winding conduction loss in half. The inherent disadvantage of this topology is in its use of three magnetic components thus increasing the cost and size of the system as well as causing termination power loss.

Several integrated magnetic solutions have been proposed to solve the above problems by integrating all the magnetic components into a single core [1,6]. Among them, the circuit shown in Fig.1 [6] is one of the most attractive topologies. A single conventional EE or EI core is used. An air gap can be placed in the center leg. However, this air gap should be minimized for better efficiency [6]. Unlike conventional magnetic integration focusing only on core integration, both core and winding integration are realized in this design. For high current applications, this winding integration is becoming more important because of lower termination loss and lower conduction loss. As a result, this topology allows for lower overall system cost and size, and higher efficiency. Other advantages include a simple

secondary winding layout for low voltage, high current applications, and reduced voltage stress of the rectifier diode by using different secondary winding turns.

However, this circuit suffers from a large leakage inductance problem because the primary and secondary windings are placed at the different core legs. In addition, the EE or EI cores used in this circuit requires an air gap on the two outer legs, and no air gap in the center leg. This kind of magnetic core is not a standard industry practice, thus adding an extra cost.

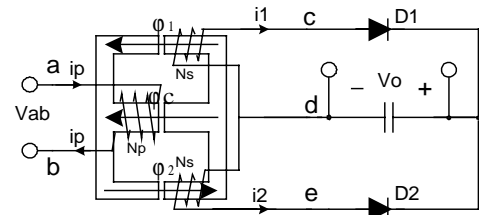


Fig. 1. Original Integrated current doubler rectifier [6]

This paper introduces a split primary winding technique to reduce the leakage inductance. By further changing the winding connection, a novel integrated current doubler rectifier is also proposed, as shown in Fig. 2. Standard EE or EI cores with an air gap only at the center leg can be used. No particular gapping process is needed, thus reducing the cost. While possessing all the advantages of the original circuit shown in Fig.1, the proposed circuit also features a higher efficiency due to reduced core loss, AC conduction loss, and switching loss. A detailed analysis of the circuit operation and comparison with the original circuit are given. Both simulation and experimental results are also provided.

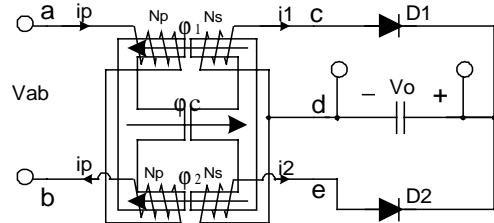


Fig. 2. Proposed integrated current doubler rectifier

* This work was supported primarily by the ERC Program of the National Science Foundation under Award Number EEC-9731677.

II. THE CONCEPT OF THE SPLIT PRIMARY WINDING AND ITS APPLICATION

Fig. 3(a) shows the magnetic structure used in the original circuit shown in Fig.1. Since the primary winding is placed at the center leg, and two secondary windings are mounted at two outer legs respectively, a lot of leakage flux goes through the air, thus causing large leakage inductance. Larger leakage inductance causes more circulation energy as well as detrimental parasitic ringings. As a result, an efficient power conversion can not be achieved.

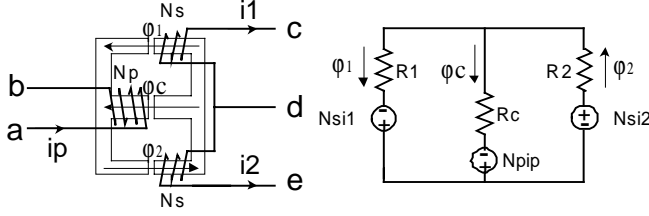


Fig. 3. Magnetic structure used in the original circuit:
(a) diagram, (b) magnetic reluctance circuit

This problem can be solved by using a split primary winding. As shown in Fig. 4(a), the primary winding is split and placed at the two outer legs. Since both the primary and secondary windings are wound on the same legs, tight couplings can be obtained. The interleaving winding technique can be used to minimize the leakage inductance, thus improving efficiency.

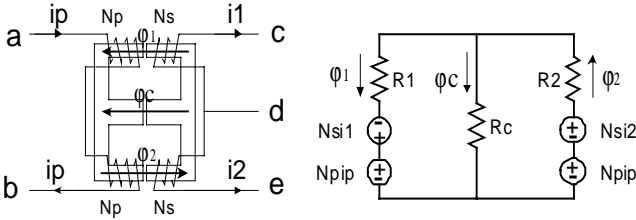


Fig. 4. Improved magnetic structure with a split primary winding:
(a) diagram, (b) magnetic reluctance circuit

The magnetic structure used in the original circuit can be replaced by the magnetic structure with a split primary winding, because they have the identical magnetic reluctance circuit, as shown in Fig. 3(b) and Fig. 4(b) respectively. Fig. 5 shows the original integrated current rectifier after using the split primary winding. Compared with the circuit shown in Fig. 1, the leakage inductance is minimized.

The operation of the circuit shown in Fig. 5 is the same as the operation of the original one. Their detailed operation and analysis can be found in [6]. Here, some results are selected and provided for the comparison in the next section.

Fig. 6 shows their typical waveforms in asymmetrical operation mode when the asymmetrical half bridge topology or the flyback-forward with active clamp topology is used for the primary circuit.

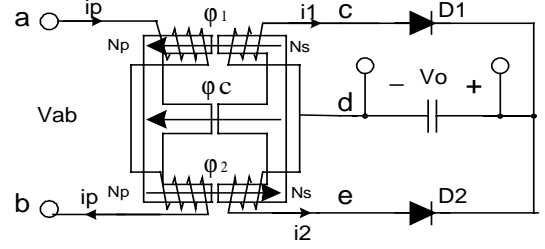


Fig. 5. Integrated current doubler rectifier with a split primary winding

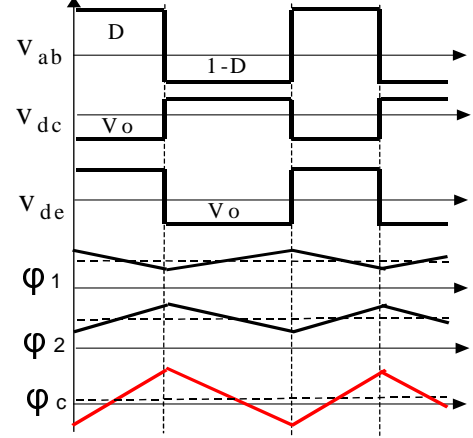


Fig. 6. Operation waveforms of the circuits shown in Fig. 1 and 5

From Fig. 6, we can see that flux ripples from two outer legs are added at the center leg, while their DC components are concealed over there. The following equation group gives the flux ripples in the three legs:

$$\begin{cases} |\Delta\Phi_1| = \frac{V_o T_s}{N_s} D \\ |\Delta\Phi_2| = \frac{V_o T_s}{N_s} (1-D) \\ |\Delta\Phi_c| = \frac{V_o T_s}{N_s} \end{cases} \quad (1)$$

Assuming that $R_1=R_2$, the output current ripple can be estimated to be:

$$\Delta i_o = \frac{V_o T_s}{N_s^2} (1-2D) R_1 \quad (2)$$

The primary current ripple can also be estimated to be:

$$\Delta i_p = \begin{cases} \frac{V_o T_s}{N_s^2} [(1-D)R_1 + R_c] , \text{ stage 1 } (0 \sim DT_s) \\ \frac{V_o T_s}{N_s^2} [-DR_1 - R_c] , \text{ stage 2 } (DT_s \sim T_s) \end{cases} \quad (3)$$

From Equ. (2) and (3), we can see that the air gap at the center leg should be minimized for higher efficiency, because the air gap increases the ripple current at the primary side.

III. A NOVEL INTEGRATED CURRENT DOUBLER RECTIFIER

In order to further improve the performance of the rectifier circuit, the winding connection of the circuit shown in Fig. 5 is changed. By doing so, a new integrated current doubler rectifier can be obtained, as shown in Fig. 2.

According to the voltage waveform across the primary winding ab , this circuit has two operation modes. One is the asymmetrical operation mode, when the asymmetrical half bridge topology or the flyback-forward with active clamp topology is used for the primary circuit. Another is the symmetrical operation mode, when the primary circuit is the conventional half bridge, full bridge or push-pull topology with symmetrical duty control. Here, the asymmetrical operation mode is selected for explaining the circuit operation.

A. Circuit Operation and Analysis

The steady state operation of the proposed rectifier circuit in the asymmetrical operation mode includes two basic stages, as shown in Fig. 7(a) and (b). Fig. 7(c) shows the corresponding magnetic reluctance circuits for these two stages. Fig. 8 shows the corresponding operation waveforms.

1) Stage 1 [0, DTs]

The voltage applied on the primary winding V_{ab} is positive. The induced voltage on the secondary winding cd is positive, thus forcing D1 to conduct and D2 to block. Winding cd conducts the full load current, and no current goes through the winding ed . During this period, the flux in the outer leg 1 decreases and the flux in the outer leg 2 increases. The magnetic reluctance for this stage shown in Fig. 7(c) gives the following flux equations:

$$\begin{cases} R_2 \phi_2 + R_c \phi_c = N_p i_p \\ R_1 \phi_1 + R_c \phi_c = N_s i_o - N_p i_p \end{cases} \quad (4)$$

2) Stage 2 [DTs, Ts]

The voltage applied on the primary winding V_{ab} is negative. The induced voltage on the secondary winding ed is positive, thus forcing D2 to conduct and D1 to block. Winding ed conducts the full load current, and no current goes through the winding cd . During this period, the flux in the outer leg 1 increases, and the flux in the outer leg 2 decreases. The magnetic reluctance for this stage shown in Fig. 7(c) gives the following flux equations:

$$\begin{cases} R_1 \phi_1 + R_c \phi_c = N_p i_p \\ R_2 \phi_2 + R_c \phi_c = N_s i_o + N_p i_p \end{cases} \quad (5)$$

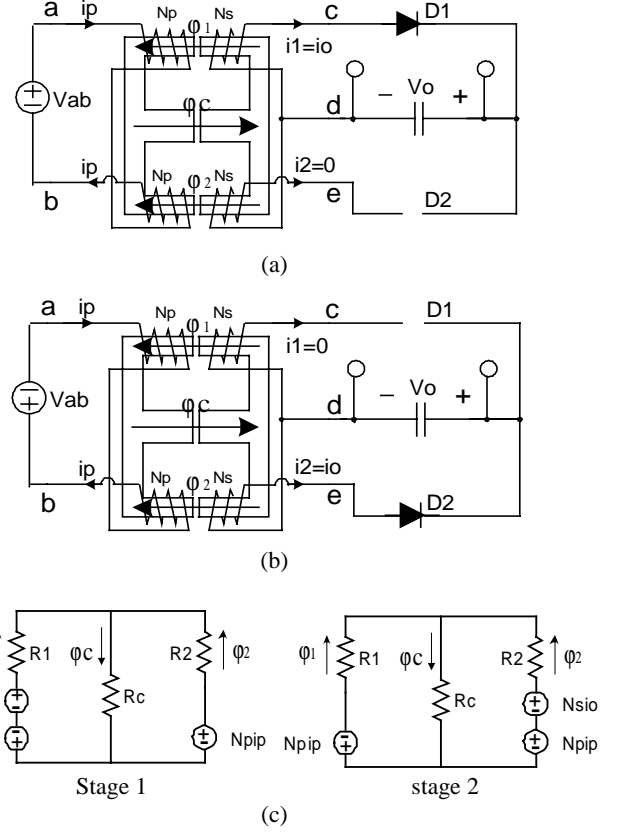


Fig. 7. Steady state operation of the new circuit: (a) stage 1, (b) stage 2, (c) magnetic reluctance circuits for two stages

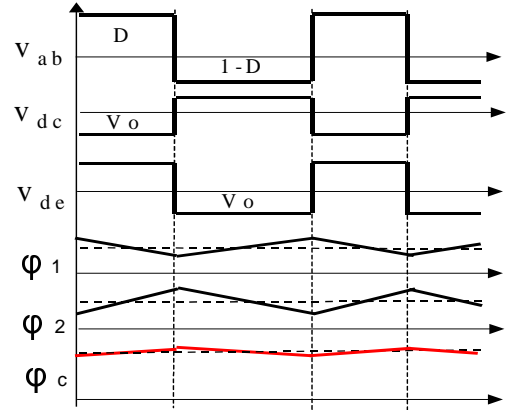


Fig. 8. Operation waveforms of the new circuit

From Fig. 8, we can see that flux ripples from two outer legs are concealed at the center leg, while their DC components are added over there. Therefore, the new circuit features lower core loss. The following equation group gives the flux ripples in three legs:

$$\begin{cases} |\Delta\phi_1| = \frac{V_o T_s}{N_s} D \\ |\Delta\phi_2| = \frac{V_o T_s}{N_s} (1-D) \\ |\Delta\phi_c| = \frac{V_o T_s}{N_s} |1-2D| \end{cases} \quad (6)$$

The output current ripple and the primary current ripple can be derived from Equ. (4), (5) and (6), as listed in the following, respectively.

$$\Delta i_o = \frac{V_o T_s}{N_s^2} (1-2D)(R_l + 2R_c) \quad (7)$$

$$\Delta i_p = \begin{cases} \frac{V_o T_s}{N_s^2} [(1-D)(R_l + 2R_c) - R_c] , \text{stage 1}(0 \sim DT_s) \\ \frac{V_o T_s}{N_s^2} [-D(R_l + 2R_c) + R_c] , \text{stage 2}(DT_s \sim T_s) \end{cases} \quad (8)$$

From Equ. (7) and (8), we can see that the air gap at the center leg reduces the ripple current at the primary side, thus improving efficiency.

B. Comparison with Original Integrated Current Doubler Rectifier

The new circuit should have all the advantages of the original circuit because of its simplified secondary side structure. These advantages include lower overall system cost and size, higher efficiency due to lower termination loss and lower conduction loss, a simple secondary winding layout for low voltage, high current applications, and reduced voltage stress of the rectifier diodes by using different secondary winding turns [6].

However, several significant advantages are realized in the new circuit, by the innovative use of a split primary winding with different connection. These advantages include the following.

1) Minimum leakage inductance

Using the split primary winding make the tight coupling possible between the primary and secondary windings. Therefore, The new circuit have a much smaller leakage inductance than the original circuit.

2) Lower cost

The magnetic core shown in Fig. 9(a) should be used for the original circuit to minimize the primary conduction losses. The magnetic core requires an air gap at two outer legs and no air gap in the center leg. This kind of core is not standard, needing a particular creation process thus increasing the cost.

However, In the new circuit, a standard core with an air gap only in the center leg, as shown in Fig. 9(b), can be used. No additional process is needed. Therefore, no extra cost is added.

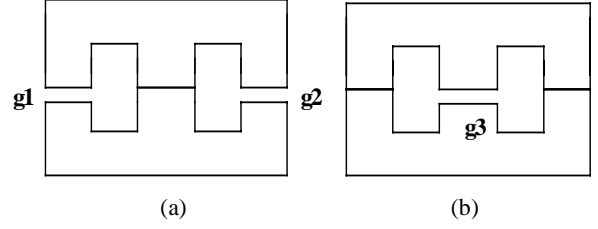


Fig. 9. Core structure: (a) for the original circuit, (b) for the new circuit

3) Lower core loss at the center leg

As we discussed before, flux ripples from two outer legs are concealed in the center leg in the new circuit, while flux ripples are added in the center leg for the original circuit. Fig. 10 shows the flux ripples at the center leg for both cases. Since most circuits are optimized at around 50% duty, the new circuit has a much lower core loss at the center leg than do the original circuit.

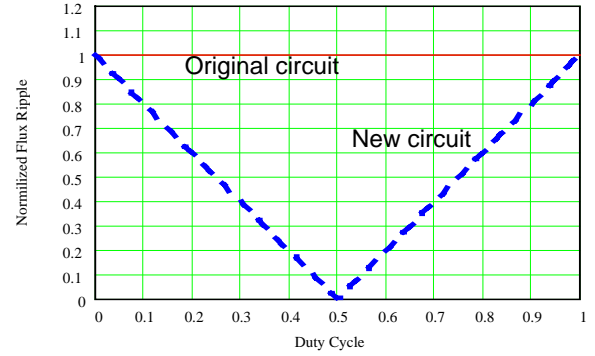


Fig. 10 Flux ripple at the center leg

4) Reduced primary current

From Equ. (2), (3), (7) and (8), we can easily see that the new circuit has a smaller primary current ripple than the original circuit under the same output current ripple assumption.

We can understand it by using the following equivalent electrical circuits of the magnetic structures, which are used in the original circuit and the new circuit respectively and correspond to the core structures shown in Fig. 9.

As shown in Fig. 11(a), the output current of the original circuit is the sum of two inductor currents. Since two inductor current ripples are concealed from each other, the inductor current ripple is much larger than the output current ripple in the original circuit. However, as shown in Fig. 11(b), the inductor current of the new circuit is always half of the output current. There is no ripple conceal effect. The inductor current ripple is half of the output current ripple. Since the primary current ripple reflects the inductor current ripple, under the same output current ripple assumption, the new circuit has a smaller primary current ripple than the original circuit.

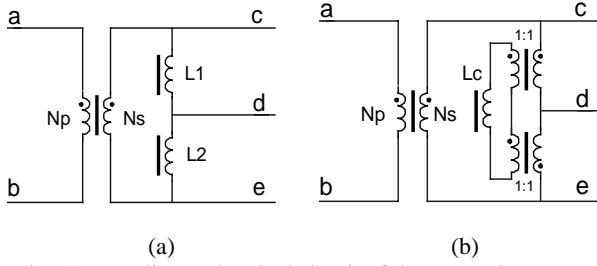


Fig. 11. Equivalent electrical circuit of the magnetic structure:
(a) in the original circuit, (b) in the new circuit

IV. DESIGN, SIMULATION AND EXPERIMENTAL RESULTS

Fig. 12 shows the simulation results for flux distribution. As shown in Fig. 12(b), the flux ripples of the two outer legs are concealed at the center leg in the new circuit.

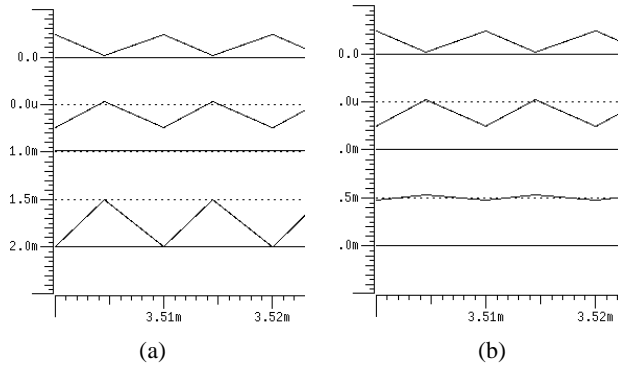


Fig. 12 Flux distribution (top-leg1, middle-leg2, bottom-center leg:
(a) in the original circuit, (b) in the new circuit

Fig. 13 and Table I show the three integrated magnetics design and their measured leakage inductance at the primary side. We can see that using the split primary winding significantly reduces the leakage inductance.

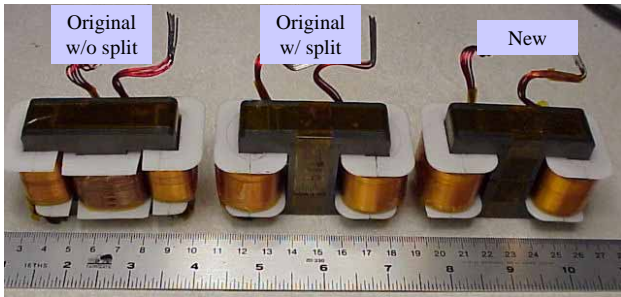


Fig. 13. Picture of three integrated magnetics

TABLE I Design parameters and leakage inductance

	Original w/o split	Original w/ split	New
Core structure	Fig. 9(a)	Fig. 9(a)	Fig. 9(b)
Winding structure	Fig. 1	Fig. 5	Fig. 2
Core size & material	PC40EE57/47		

Winding turns	Np=15, Ns=8		
Air gap thickness	42mil		
Leak inductance (uH)	33.8	3.2	3.3

Fig. 14 shows the experimental setup. “DUT” will be replaced by the integrated magnetics shown in Fig. 13. Switches Q1 and Q2 run at 200KHz, 50% duty.

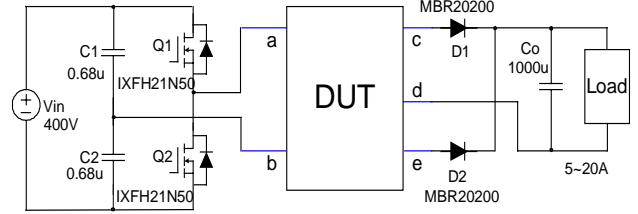


Fig. 14. Experimental setup

Fig. 15 shows the measured waveform of the primary current. As we can see, the primary current ripple is reduced in the new circuit. Therefore, the new circuit is expected to have higher efficiency due to lower conduction loss and switching loss at the primary side. Fig. 16 shows the measured efficiency. There is more than a 1% efficiency improvement at heavy load, and more than a 2% efficiency improvement at light load.

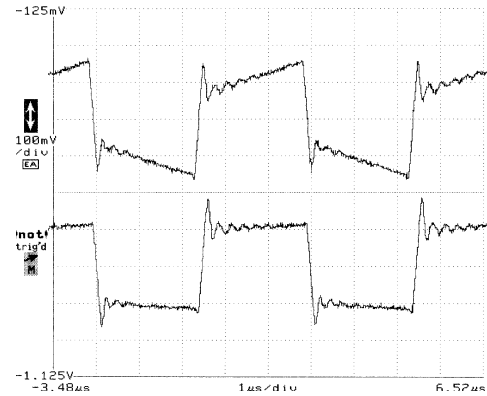


Fig. 14. the primary current waveform comparison (2.5A/div, top-the original circuit with a split winding, bottom-the new circuit)

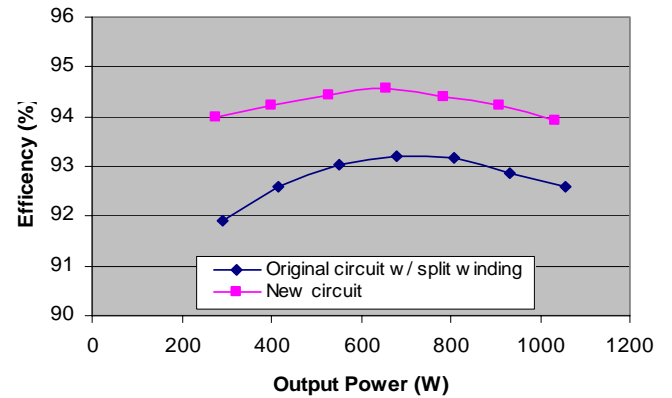


Fig. 15. Efficiency comparison

The new integrated current doubler rectifier was adopted for the following design:

Input voltage - 400V;
Output voltage - 48V;
Output power - 1kW; and
Switching frequency - 200KHz.

The primary power stage uses a half bridge topology with asymmetrical duty control because of its simple structure and ZVS soft-switching capability [5-7].

Fig. 16 shows the experimental waveforms. As we can see, the ZVS turn-on of primary switches is realized. Fig. 17 shows the measured efficiency, around 94% at full load. Fig. 18 shows the picture of the prototype.

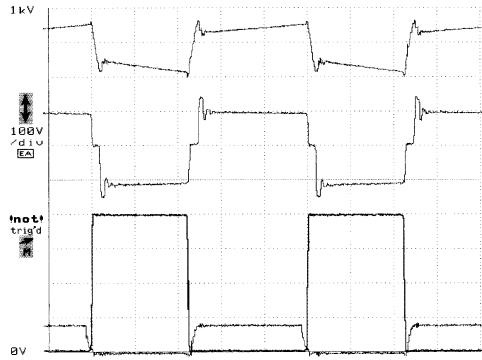


Fig.16. Experimental waveforms
Top: primary current, 5A/div
Middle: secondary voltage, 100v/div
Bottom: drain-to-source voltage, 100v/div;
Gate-to-source voltage, 20v/div

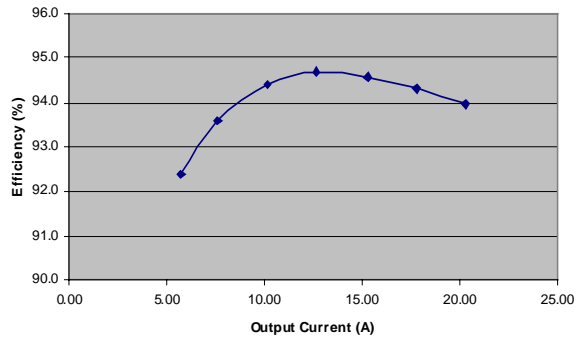


Fig17. Measured efficiency

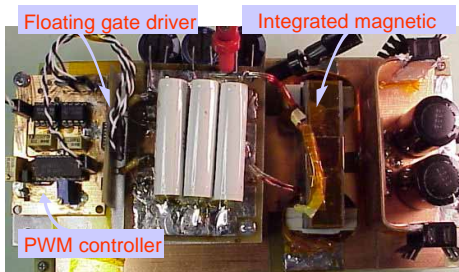


Fig. 18. Picture of prototype

VI. CONCLUSION

A novel integrated current doubler rectifier is proposed based on the split-winding concept. A detailed analysis of the circuit operation and comparison with the original circuit have been addressed. This new circuit features low cost and low power loss due to a single standard magnetic core, minimized secondary high current windings and their interconnections, reduced core loss, reduced primary current ripple and minimized leakage inductance. Both simulation and experimental verifications have been carried out. A design example featuring 400V input, 48V output, 200KHz switching frequency, and 1KW output power is also provided.

REFERENCES

- [1] C. Peng, M. Hannigan, O. Seiersen, "A new efficient high frequency rectifier circuit", *High Frequency Power Conversion Conference Proceedings*, pp. 236-243, June 1991.
- [2] K. O'Meara, "A new output rectifier configuration optimized for high frequency operation", *High Frequency Power Conversion Conference Proceedings*, pp. 219-225, June 1991.
- [3] L. Balogh, "The performance of the current doubler rectifier with synchronous rectification", *High Frequency Power Conversion Conference Proceedings*, pp. 216-225, May 1995.
- [4] N.H. Kutkut, D.M. Divan, and R.W. Gascoigne, "An improved full-bridge zero-voltage switching PWM converter using a two-inductor rectifier", *IEEE Tran. Ind. Appl.*, Vol. 31, No. 1, pp. 119-126, Jan./Feb. 1995.
- [5] L. Huber, M.M. Jovanovic, "Forward converter with current-doubler rectifier: analysis, design and evaluation results", *IEEE APEC'97*, pp. 605-611, 1997.
- [6] W. Chen, G. Hua, D. Sable, F. C. Lee, "Design of high efficiency, low profile, low voltage converter with integrated magnetics", *IEEE APEC'97*, pp. 911-917, 1997.
- [7] T. Ninomiya, N. Matsumoto, M. Nakahara, K. Harada, "Static and dynamic analysis of zero-voltage-switched half-bridge converter with PWM control", *IEEE PESC'91*, pp. 230-237, 1991.
- [8] P. Imbertson, N. Mohan, "New PWM converter circuits combining zero switching loss with low conduction loss", *IEEE International Telecommunication Energy Conference Proceedings*, pp. 179-185, 1991.