# Single-Wire Current-Share Paralleling of Current-Mode-Controlled DC Power Supplies

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***Abstract*—This paper presents a new single-wire autonomous current-share paralleling of current-mode-controlled dc power supplies. The proposed control scheme makes use of the nature of fast response of the inner current loop and the share bus injected signal to improve the response of the power supplies. It reduces the unbalance of current distribution during the transient state and avoids the fault alarm for the current limit. Through the theoretical derivation, the proposed control circuit can be designed by the three-loop control method. A design example of two 400-V/48-V 20-A parallel modules is set up and experimental recordings verify the performance of current sharing.**

***Index Terms*—Current-mode control, current sharing, single wire.**

## I. Introduction

IN RECENT years, due to the rapid advance of computer and communication, the power supplies must provide high current up to hundreds of amperes, and still have high efficiency and reliability. Under such requirements, multimodule paralleling is usually used and the load current is equally shared. In this way, the current stress of the switching devices is reduced and the efficiency and reliability [1] are improved. About the current-sharing control, a variety of schemes have been presented [2]–[10] over the years. The single-wire current-share method [7] is comparatively simple and, hence, favorable. The configuration is shown in Fig. 1. The share bus carries the average current signal reference for every module. No central control unit is required and only a few operational amplifiers or comparators [10] are added in the modules.

In practical applications, some unnecessary minor alarms occur as the load rapidly changes or one module fails and shuts down. The output currents of the converter modules are not equally distributed during the load transient. The protection circuit limits the output currents when they exceed the rated values and an alarm may be raised. These imbalances usually occur when the circuit components or output cables are not identical for every module [3]. To avoid the unfavorable situation, we try to use the current-mode control instead of the conventional voltage-mode control in the modules. The simplified circuit of conventional voltage mode is shown in Fig. 2(a). The current-sharing error signal is injected into the voltage loop to adjust the voltage command [2]–[5]. In current-mode control, the inner current loop, which has less phase shift, can have wider bandwidth without instability and, hence, improve transient response. It can be used to alleviate the unbalance problem during the transient. The current sensor is already used to sense the inductor current in current-mode control; it can be also used for current sharing.

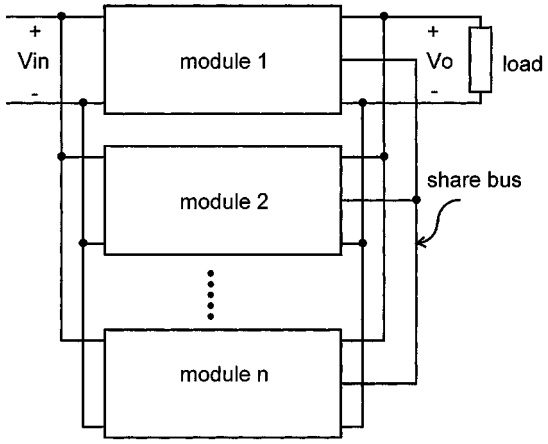


Fig. 1. Single-wire current sharing of paralleled converter modules.

The paralleled current-mode control has been investigated [11]–[14]. A simplified circuit of the paralleled current-mode control is shown in Fig. 2(b). Because the output current is proportional to the voltage error signal, the current command of every module is controlled by common voltage feedback. The common feedback circuit cannot be modularized, and the system may be shut down for the failure of the common part. The single-wire current sharing for current-mode control has been studied in the literature [5], [7], [15]. Commercialized control ICs, such as the UC3907, can also be used in current-mode-controlled modules [5], but the share bus carries the maximum current information of paralleled modules. Another method proposed by Small in 1988 [7] is shown in Fig. 2(c). The share bus carries the average current command signal, and the current-sharing error is injected into the reference voltage. The bandwidth of the current-sharing response is limited by the voltage loop. In this paper, a novel current-sharing control scheme is proposed. The simplified circuit is shown in Fig. 2(d). The share bus carries the average inductor current signal and the injected

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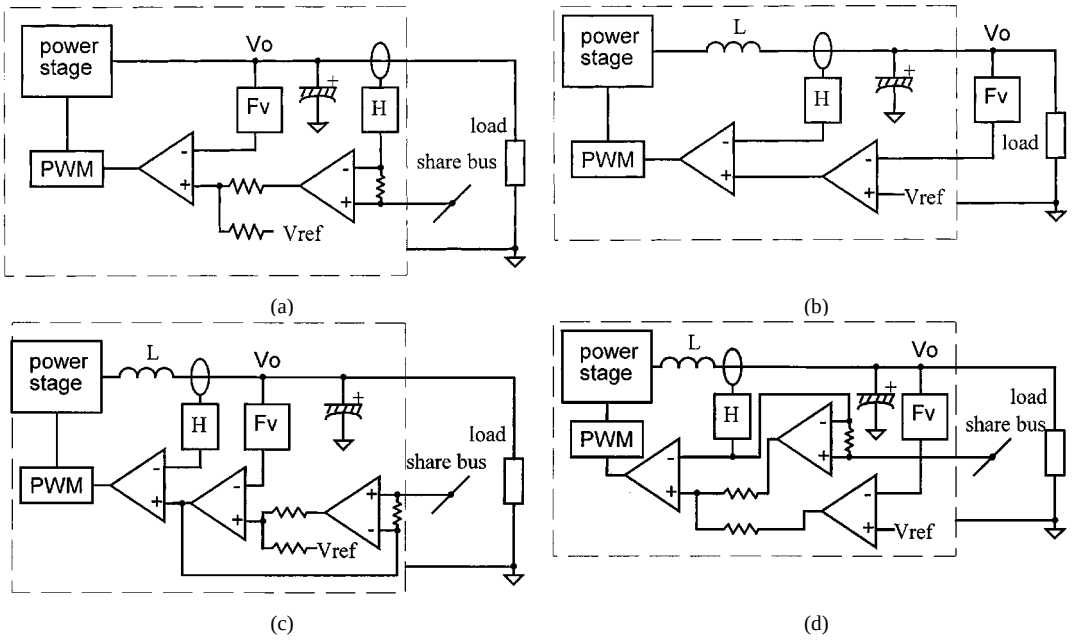


Fig. 2. Comparison among the current-sharing control schemes. (a) Conventional voltage mode. (b) Current mode with the common voltage feedback, (c) Current mode with the average current command share bus. (d) Proposed control scheme: current mode with the average inductor current-share bus.

point of current-sharing signal is on the inner current loop. Thus, the bandwidth of the current-sharing control is not limited by the voltage loop.

In the following, the new current-sharing circuit of current-mode controlled converters is described and analyzed. The design guidelines are listed and a design example of the average current-mode-controlled modules is implemented. Finally, the experimental results verify the performance of the circuit.

## II. Circuit Description

The circuit of a single module in the proposed control is depicted in Fig. 3. Three operational amplifiers form the control circuit. The functions of each portion are as follows.

1) *Share Bus:* It carries the instantaneous average current signal for the reference of the module current when paralleling. A share resistor $R_s$ of high accuracy is connected between the share bus and the output of the current sensor $H$. When the values of $R_s$ for every module are all the same, the output currents of the modules are the same. If they are proportional, the output currents are also proportional.
2) *Voltage Error Amplifier $U_v$:* The output voltage error signal is amplified as part of the current command. The current command is composed of the voltage error and the current-sharing error.
3) *Current-Sharing Amplifier $U_s$:* It amplifies the error signal between the share bus and the inductor current, and injects its signal into the current command.
4) *Current Amplifier $U_c$:* It amplifies the error signal between the inductor current and the current command, and sends the error to the modulator.
5) *Pulsewidth Modulator:* The analog control signal is converted into discrete control pulses.

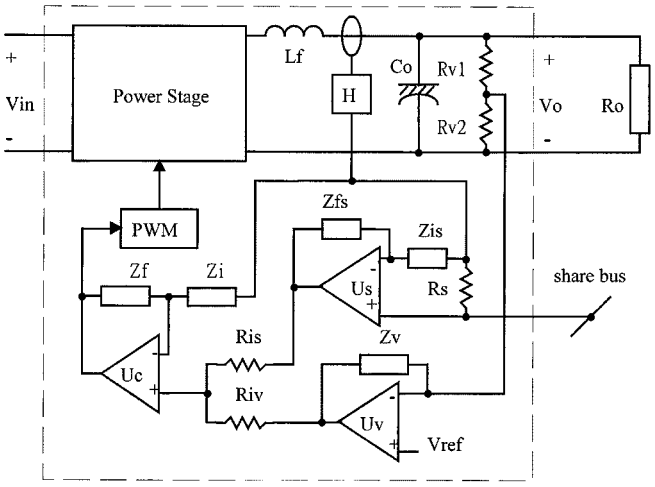


Fig. 3. Proposed control circuit for one current-mode-controlled module.

6) *Power Stage:* The power switches, switch drivers, and output filter components $L_f$ and $C_o$ are included.
7) *Current Sensor H:* Hall-effect sensors or other current-sensing devices may be used to sense the inductor current.

## III. Circuit Operations

In this section, the circuit operations of a single module and multimodule paralleling are presented.

### A. Single Module

The current signal of the module is equal to the share bus because the input impedance of the share amplifier is high enough and no current passes through $R_s$. Thus, the sharing error signal is zero and the control is the same as a standard two-loop control.

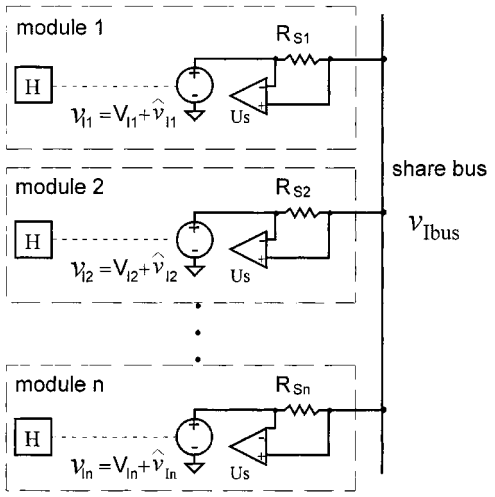


Fig. 4. Circuit between share bus and the share resistors.

### B. Multimodule Paralleling

For the same value of the share resistors $R_s$, the share bus carries average current signal reference. The share error signal is the difference between the share bus and the individual output current. This error is injected into the current command. By the pulsewidth modulation (PWM) control and power circuit, the average inductor current is adjusted. When the output current is lower than the share bus signal, the injected error tends to increase the inductor current to reduce the error. This negative feedback mechanism will reduce the error within the tolerance. At the steady state, the output current of every module is the same as the share bus indicated, and the purpose of the current sharing is achieved.

## IV. Analysis

There are three control loops in the presented circuit—the voltage loop, the sharing loop, and the current loop. A simplified circuit model for paralleled modules is set up and the control loop analysis is performed to derive the design rules of the proposed current-sharing controller.

The circuit between share resistors and the share bus is shown in Fig. 4. For $n$ paralleled modules, $v_{I1} \cdots v_{In}$ are the instantaneous voltage signals derived by the current sensors from the inductor currents and $v_{I\text{bus}}$ is the instantaneous voltage signal on the share bus. If the share resistors $R_{S1} \cdots R_{Sn}$ are equal, then

$$v_{I\text{bus}} = \frac{1}{n}(v_{I1} + v_{I2} + \cdots + v_{In}). \tag{1}$$

In small-signal analysis,

$$\hat{v}_{I\text{bus}} = \frac{1}{n}(\hat{v}_{I1} + \hat{v}_{I2} + \cdots + \hat{v}_{In}). \tag{2}$$

If the transfer function of the current sensor is $H$, then

$$\hat{v}_{I\text{bus}} = \frac{H}{n}(\hat{i}_{L1} + \hat{i}_{L2} + \cdots + \hat{i}_{Ln}) \tag{3}$$

where $\hat{i}_{L1}$, $\hat{i}_{L2}$, $\cdots$, $\hat{i}_{Ln}$ are the small-signal representations of the output inductor currents.

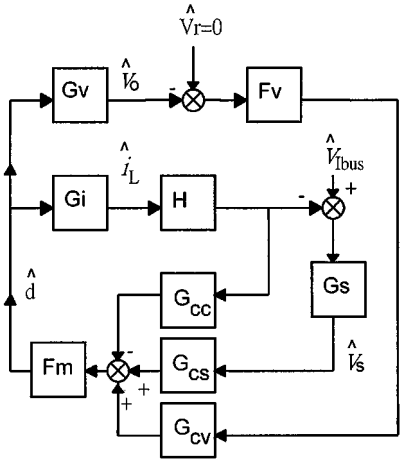


Fig. 5. Block diagram of the control circuits.

Neglecting the input voltage disturbance, the control block diagram for one of the paralleled module is shown in Fig. 5 where

| | |
|---|---|
| $F_v$ | voltage feedback transfer function; |
| $H$ | current to voltage signal transfer function; |
| $Fm$ | PWM modulator transfer function; |
| $G_v$ | duty cycle to output voltage transfer function; |
| $G_i$: | duty cycle to inductor current transfer function; |
| $Gs$ | transfer function of the current-sharing amplifier; |
| $G_{cc}$ | current amplifier transfer function for current loop; |
| $G_{cs}$ | current amplifier transfer function for sharing loop; |
| $G_{cv}$ | current amplifier transfer function for voltage loop. |

$\hat{v}_o$, $\hat{i}_L$, and $\hat{d}$ are the disturbances of output voltage, inductor current, and duty cycle, respectively. The reference voltage $V_r$ is constant and the small signal $\hat{v}_r = 0$.

In Fig. 5, if the module $n$ has a current-sharing disturbance, the injected current-sharing error signal into the controller$\hat{v}_S$ is

$$\hat{v}_S = G_S(\hat{v}_{I\text{bus}} - H\hat{i}_L). \tag{4}$$

Substitute (3) into (4) and $\hat{i}_L \equiv \hat{i}_{Ln}$,

$$\hat{v}_S = -\frac{n-1}{n} G_S H \hat{i}_{Ln} + G_S \frac{H}{n}(\hat{i}_{L1} + \hat{i}_{L2} + \cdots + \hat{i}_{Ln-1}). \tag{5}$$

The disturbances of the inductor currents of other modules do not form a local feedback loop in module $n$. The second term of (5) can be considered as an external disturbance to take into account the interactions among the modules. If the interactions could be neglected, the current-sharing error is

$$\hat{v}_S \cong -\frac{n-1}{n} G_S H \hat{i}_L. \tag{6}$$

The open-loop gains—the voltage loop $T_V$, the sharing loop $T_S$, and the current loop $T_I$ can be derived from Fig. 5

$$T_I = F_m G_{cc} H G_i \tag{7}$$

$$T_v = F_m G_{cv} F_v G_v \tag{8}$$

$$T_S = \frac{n-1}{n} F_m G_{CS} G_S H G_i. \tag{9}$$

When only one module is used, the loop gain of current sharing, $T_s = 0$. For an arbitrarily large number of modules paralleled,

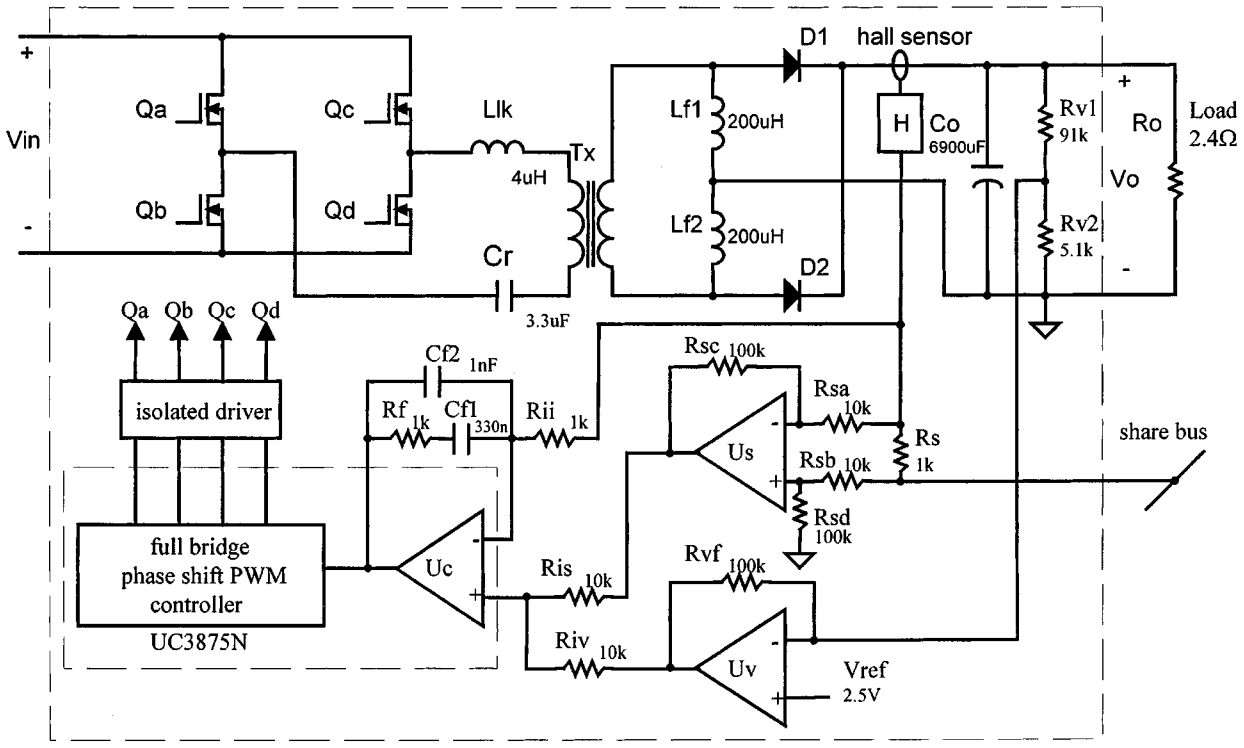


Fig. 6. Circuit diagram of the design example.

$T_s = F_m G_{cs} G_s H G_i$. Then, the three-loop control method [16] can be used to design the controller.

## V. Design Considerations

According to the analysis, the following design guidelines have been developed.

1) About the average current-mode control, the second pole of the error amplifier $U_c$ must be placed higher than half the switching frequency. The zero of $U_c$ must be placed at least one decade lower than half the switching frequency. The external ramp setting is similar to the voltage mode. Choose the gain of the error amplifier $U_c$ that makes proper damping on the resonant peak at half of the switching frequency [17], in accordance with Ridley's current-mode control model [18].
2) The design must be based on the multimodule condition, because the overall loop gain is higher than the single module case. To identify the stability, the closed-loop gains which include the overall loop gain $T_1$ and the outer loop gain $T_2$ are [16]

$$T_1 = T_I + T_S + T_V \tag{10}$$

$$T_2 = \frac{T_V}{1 + T_I + T_S}. \tag{11}$$

$T_1$ and $T_2$ can be experimentally measured or mathematically computed [6]. To design the controller to ensure the stability of $T_1$ and $T_2$, the rules are listed in the following.

a) To obtain the benefits of current-mode control, the crossover frequency of the current loop must be higher than that of the voltage loop. The high bandwidth of the current loop can improve the closed-loop response of the multiloop control [19]. It is better to design the current loop as high as possible for either the single module or multimodule case.
b) To avoid the dip [16] in the overall loop gains that can cause the system to be unstable, do not make the phases of the two loops in opposite directions when the two loops cross over. For example, the $|T_I| = |T_V|$ and $T_I(-90°)$ and $T_V(-270°)$ should not occur at the same frequency. The subtraction of the two loops will cause a dip that makes the system unstable.

3) To simplify the design, the control of current-sharing amplifier $U_s$ commonly uses proportional control [8]. The gain $G_s$ of the current-sharing amplifier must be as high as possible without instability. The accuracy of current sharing is determined by $G_s$ for proportional control.

## VI. Design Example

A design example of the proposed current-sharing control of paralleled dc power supplies is demonstrated in this section. The dc/dc converter is 400-V/48-V 20-A output. For average current-mode control, the full-bridge phase-shifted PWM zero-voltage-swtching (ZVS) topology is selected. The main transformer of the converter is not center tapped, but uses two independent inductors as a current doubler [20], [21]. Compared with the bridge rectifier, it wastes only one diode drop in the output path. In addition, the transformer secondary winding is rated one half the load current with no

center-tapped connection. It can improve the efficiency of the converter. The complete circuit of a single module is shown in Fig. 6, where $Q_a$, $Q_b$, $Q_c$, and $Q_d$ are the main switches of full-bridge converter controlled by commercial phase-shifted PWM IC UC3875N. The inductor $L_{lk}$ is designed for ZVS of the main switches. $C_r$ blocks the dc voltage to prevent the main transformer $T_x$ from saturation. The diodes $D_1$ and $D_2$ rectify the ac output. The bulk capacitor $C_o$ and two inductors, $L_{f1}$ and $L_{f2}$, are the output filter. A current sensor $H$ is put in the loop path of the two output inductors for feedback control of current mode and current sharing. The proposed control circuit is designed to sense the output voltage, inductor current, and share-bus voltage, and inject the control signal into the phase-shifted PWM controller UC3875N.

The circuit parameters are listed as follows:

| | |
|---|---|
| switching frequency | $f_s$100 kHz; |
| turn ratio of the main transformer | 18 : 6; |
| power MOSFET $Q_a$–$Q_d$ | 500 V/30 A; |
| output inductor filter $L_{f1}$, $L_{f2}$ | 200 $\mu$H; |
| fast-recovery diodes $D_1$, $D_2$ | 600 V/60A; |
| primary inductor $L_{lk}$ | 4 $\mu$H; |
| output capacitor $C_o$ | 6900 $\mu$F; |
| transfer ratio of the current sensor H | 4 V/100A. |

The output voltage of the current doubler is half of the transformer voltage output and the equivalent filter inductance is half as much as one of the two inductor filters. The turns ratio $m$ of the main transformer is $0.5 * (1/3) = 1/6$, and the output filter inductor $L_f = L_{f1}//L_{f2} = 100$ $\mu$H. The equivalent circuit is illustrated in Fig. 7. After the power stage parameters are determined, the controller and current-sharing network can then be designed.

The parameters and the transfer functions are listed as follows:

| | |
|---|---|
| $n$ | number of modules be paralleled, $n = 1$ to infinity; |
| $R_o$ | load resistance for a module. If $n = 2$ and the output voltage and current is 48 V/40 A, then the load current for every module is 20 A, and the load resistance $R_o = 2.4\ \Omega$; |
| $V_{\text{in}}$ | input voltage, $V_{\text{in}} = 400$ V; |
| $F_V$ | $= R_{Vf}/R_{V1} \cong 1$; |
| $Gs$ | $= 10$; |
| $F_m$ | $= 0.25$; |
| $L_{lk}$ | $= 4$ $\mu$H; |
| $m$ | equivalent transformer turns ratio $m = 1/6$; |
| $L_f$ | equivalent output filter inductor 100 $\mu$H; |
| $C_o$ | output filter capacitor 6900 $\mu$H; |
| $R_i$ | transfer ratio of the Hall sensor, $R_i = 0.04$ V/A. |

For modeling the current-mode control, the sampling gain of Ridley's model is inserted in the current-sensing network [18], so the transfer function of the current sensor is

$$H = R_i H_e(s) = R_i \left(1 + \frac{s}{\omega_s Q} + \frac{s^2}{\omega_s^2}\right). \tag{12}$$

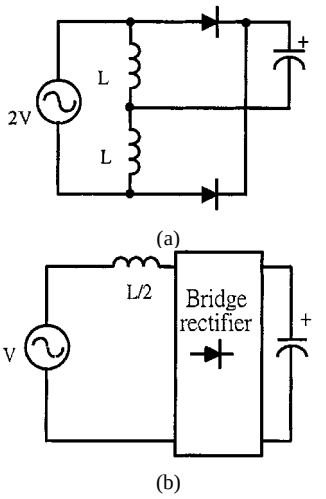


Fig. 7. The equivalent circuit of the current doubler. (a) Current doubler. (b) Equivalent circuit.

$H_e(s)$ is the sampling gain of the current-mode control, $Q = -2/\pi$, $\omega_s = 2\pi f_s$. The models of the phase-shifted PWM converter are [22]

$$G_V = \frac{mV_{\text{in}}Z_f}{Z_f + R_d}\left(\frac{1}{\Delta f}\right) \tag{13}$$

$$G_I = \frac{mV_{\text{in}}}{Z_f + R_d} \tag{14}$$

where

$$R_d = 4m^2 L_{lk} f_s \tag{15}$$

$$Z_f = \frac{R_O \Delta f}{1 + sR_O C_O} \tag{16}$$

$$\Delta f = s^2 L_f C_O + s\frac{L_f}{R_O} + 1. \tag{17}$$

The transfer functions of the current amplifier are

$$G_{CC} = \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)} \tag{18}$$

$$G_{CS} = \frac{R_{iv}}{R_{is} + R_{iv}}\left[1 + \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)}\right] \tag{19}$$

$$G_{CV} = \frac{R_{is}}{R_{is} + R_{iv}}\left[1 + \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)}\right] \tag{20}$$

where

$$\omega_z = \frac{1}{R_f C_{f1}} \tag{21}$$

$$\omega_p = \frac{C_{f1} + C_{f2}}{R_f C_{f1} C_{f2}} \tag{22}$$

$$\omega_t = \frac{1}{R_{ii} C_{f2}}. \tag{23}$$

Half of the switching frequency is 50 kHz. The second pole of the error amplifier is placed at 160 kHz and the zero is placed at 500 Hz. The gain of the error amplifier is set to make the bandwidth of the current loop high enough and the system stable. The gain of the current loop can be adjusted by changing the value of $R_{ii}$ in (23).

The following equation can help to find the approximate value of $R_{ii}$ [17]:

$$R_{ii} = \frac{\left(\frac{1}{2} + \frac{1}{\pi}\right) F_m V_{\text{in}} R_i}{(C_{f1} + C_{f2}) L_f f_s \omega_z}. \tag{24}$$

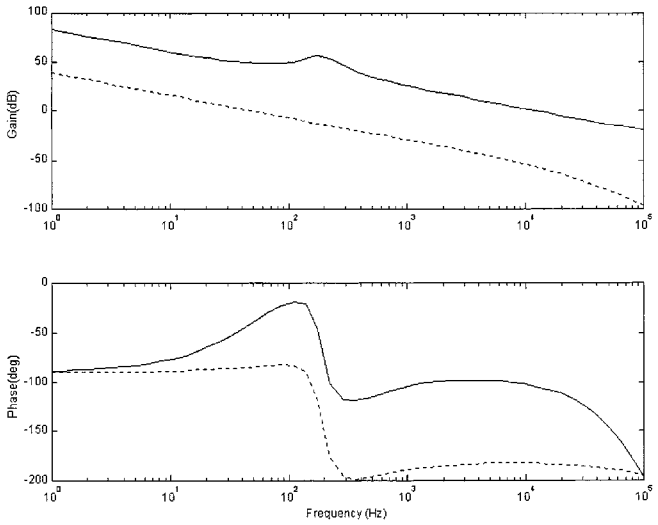


Fig. 8. Simulated closed-loop gains $T_1$ and $T_2$ for light load ($R_o = 480\ \Omega$) case. ($T_1$ ——, $T_2$ – – ––).

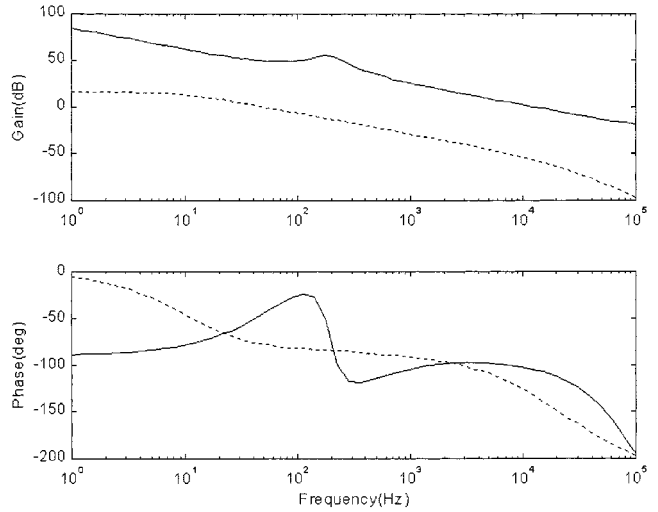


Fig. 9. Simulated closed-loop gains $T_1$ and $T_2$ for full load ($R_o = 2.4\ \Omega$) case. ($T_1$ ——, $T_2$ – – ––).

The voltage loop gain can be adjusted by $R_{is}$, $R_{iv}$, and $G_s$. For the circuit of Fig. 6, the small-signal models are built and simulated using MATLAB. The simulated closed-loop gains of light load ($R_o = 480\ \Omega$) condition are shown in Fig. 8. The simulated closed-loop gains for full load ($R_o = 2.4\ \Omega$) condition are shown in Fig. 9. All the closed-loop gains show that the power supply system is stable.

## VII. Experimental Results

Two 400-V/48-V 20-A output current dc/dc converter modules are implemented as shown in Fig. 6. To test the performance of the current-sharing circuit, an experiment of the total load changing from 0 to 20 A has been conducted. The transient response of the output currents and inductor currents for disconnected and connected share-bus conditions are shown in Fig. 10. In Fig. 10(a), without the current-sharing bus, the output current is not equally distributed because the inductor currents do not charge the output capacitors at the same time during the

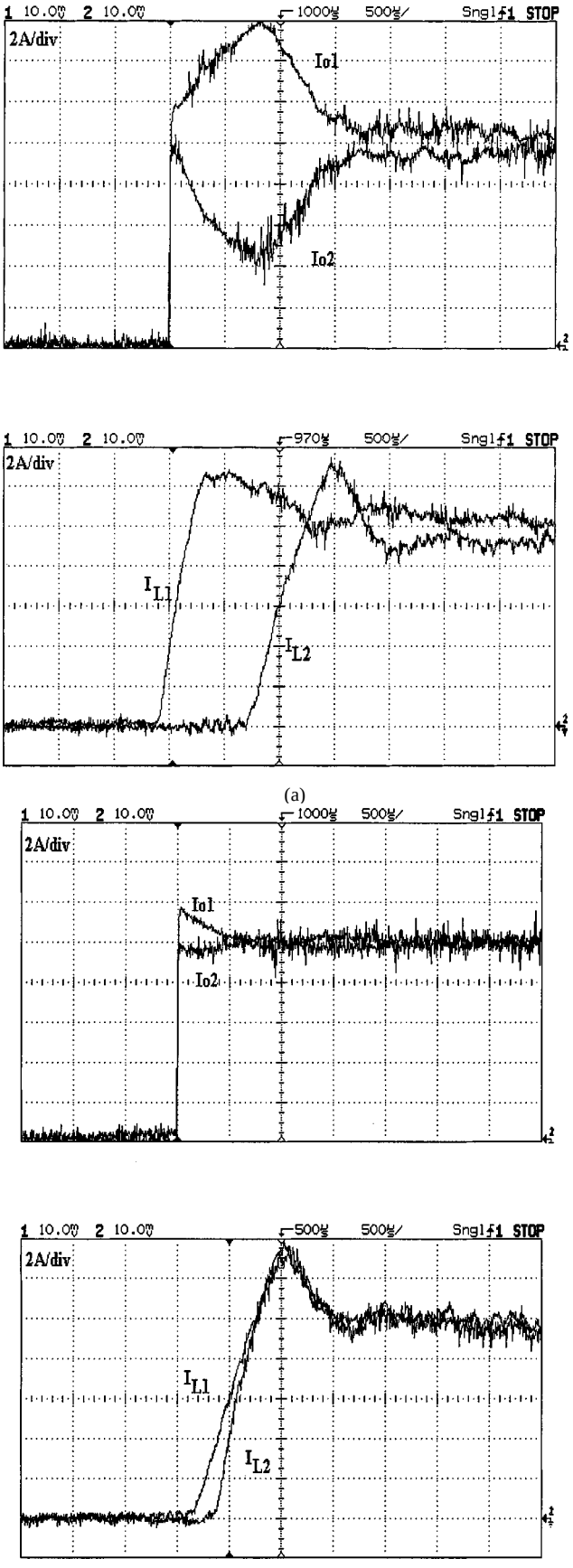


Fig. 10. Transient responses of the output and inductor currents. (a) Share bus disconnected. (b) Share bus connected.

TABLE I
CURRENT-SHARING TEST RECORDINGS

| nominal output current (A) | module 1 current (A) | module 2 current (A) | total current (A) | average current (A) | error current (A) | error rate (%) |
|---|---|---|---|---|---|---|
| 5 | 2.54 | 2.61 | 5.15 | 2.58 | 0.07 | 2.72 |
| 10 | 5.04 | 4.95 | 9.99 | 5.00 | 0.09 | 1.80 |
| 15 | 7.48 | 7.25 | 14.73 | 7.37 | 0.23 | 3.12 |
| 20 | 9.94 | 9.70 | 19.64 | 9.82 | 0.24 | 2.44 |
| 25 | 12.53 | 12.05 | 24.58 | 12.29 | 0.48 | 3.91 |
| 30 | 14.86 | 14.29 | 29.15 | 14.58 | 0.57 | 3.91 |
| 35 | 17.76 | 17.11 | 34.87 | 17.44 | 0.65 | 3.73 |
| 40 | 19.87 | 19.45 | 39.32 | 19.66 | 0.42 | 2.14 |

load transient. This imbalance is usually measured when the output inductors or capacitors or cable resistances are not exactly identical. In Fig. 10(b), the share bus forces the output inductor currents to charge the output capacitors almost simultaneously. The output currents of the two modules are very close. The overcurrent condition is, thus, avoided. At the steady state, the output current is equal to the inductor current. The current sharing is always controlled by the proposed circuit in transient or steady state. The steady-state test for current-sharing accuracy is recorded in Table I.

## VIII. CONCLUSIONS

The proposed single-wire current sharing of current-mode-controlled power supplies has the high-speed response to reduce the unbalance of the current distribution during the transient state and avoids the minor alarm of the current limit. The current sensor is used for feedback control and current sharing so that the cost is not higher than the voltage-mode control. It can be used in all modularized converters and the design of the modules can follow the multiloop control method. Compared with the conventional voltage-mode-control current sharing, the performance of the proposed current-mode power supply system is much improved.

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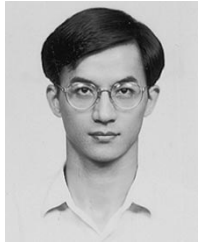

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